Design Example Report

Title	***40 W Dual Output Power Supply Using InnoSwitch3-CE INN3168C-H101***
Specification	90 VAC – 265 VAC Input; 5 V, 3 A and 50 V, 0.5 A Dual Output
Application	LED Monitor
Author	Applications Engineering Department
Document Number	DER-571
Date	October 3, 2017
Revision	1.0

Summary and Features

- InnoSwitch3-CE - industry first AC/DC ICs with isolated, safety rated integrated feedback
- All the benefits of secondary-side control with the simplicity of primary-side regulation
    - Insensitive to transformer variation
    - Extremely fast transient response independent of load timing
- Primary sensed output overvoltage protection (OVP) eliminates optocoupler for fault protection
- Accurate thermal protection with hysteretic shutdown
- Input voltage monitor with accurate brown-in / brown-out and overvoltage protection

Power Integrations

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing 5 V, 3 A and 50 V, 0.5 A dual output embedded power supply utilizing INN3168C-H101 from the InnoSwitch3-CE family of ICs.

This design shows the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

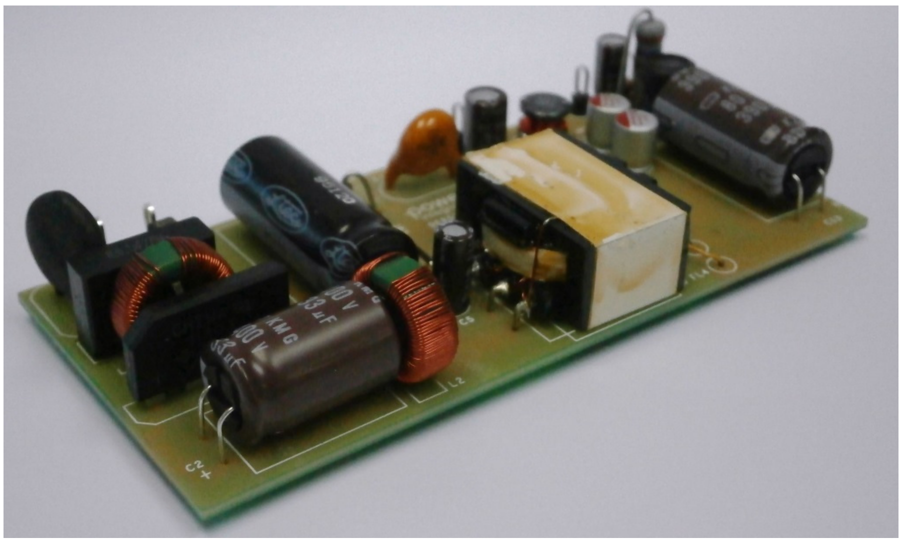

Figure 1 – Populated Circuit Board.
Length (106.7 mm) x Width (50.8 mm) x Height (21.5 mm).

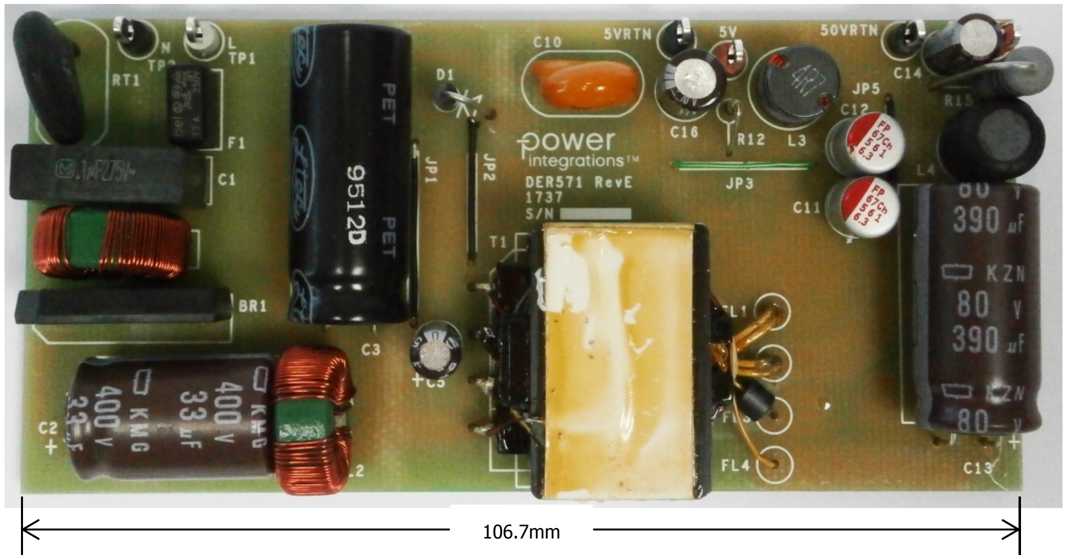

Figure 2 – Populated Circuit Board, Top View.

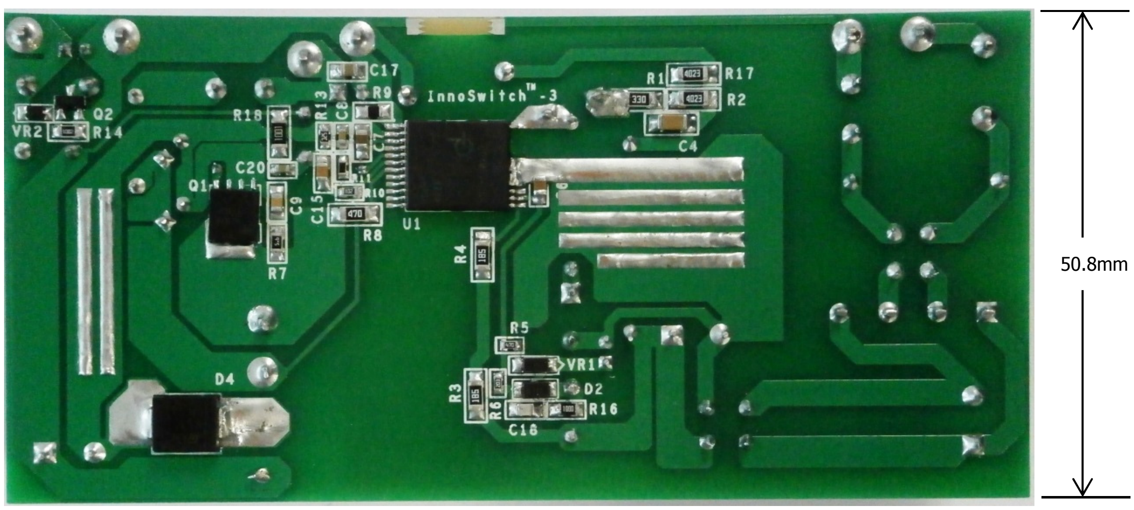

Figure 3 – Populated Circuit Board, Bottom View.

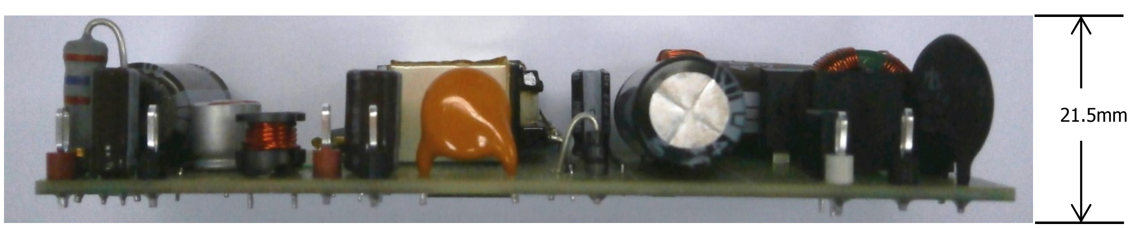

Figure 4 – Populated Circuit Board, Side View.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage 1	V_{OUT1}	4.75	5	5.25	V	
Output Ripple Voltage 1	$V_{RIPPLE1}$			50	mV	20 MHz Bandwidth.
Output Current 1	I_{OUT1}	0.01		3.0	A	
Output Voltage 2	V_{OUT2}	40	50	65	V	
Output Ripple Voltage 2	$V_{RIPPLE2}$			200	mV	20 MHz Bandwidth.
Output Current 2	I_{OUT2}	0		0.5	A	
Total Output Power						
Continuous Output Power	P_{OUT}		40		W	
Efficiency						
Average	η		89		%	Measured at 115 / 230 VAC, P_{OUT} 25 ºC.
No Load Input Power				30	mW	
Light Load Input Power				100	mW	With 10 mA Load on 5 V at 230 VAC and No-load on 50 V.
Thermals						
All components				90	ºC	Measured at 90 / 265 VAC, Room Temperature.
Environmental						
Conducted EMI		Meets CISPR22B /EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
ESD		±16.5		90	kV	Contact
		±8			kV	Air Discharge. No Degradation in Performance.
Surge		1			kV	
Common Mode Ring Wave		6			kV	
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level.

3 Schematic

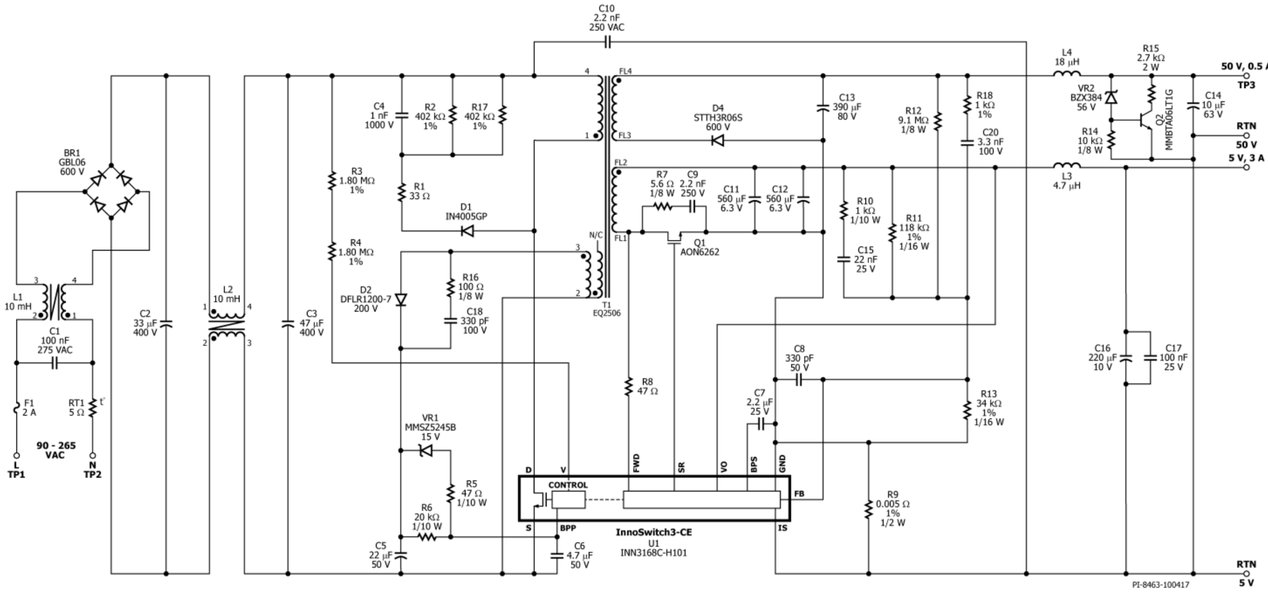

Figure 5 – Schematic.

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4 Circuit Description

4.1 Input EMI Filter and Rectifier

Fuse F1 isolates the circuit and provides protection from component failure while RT1 limits the inrush current when input voltage is applied in the circuit.

Common mode chokes L1 and L2 together with C1, C2, and C3 provides attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the input capacitors C2 and C3.

4.2 InnoSwitch3-CE Primary

One side of the transformer primary is connected to the rectified DC bus; the other is connected to the integrated 650 V power MOSFET inside the INN3168C IC (U1).

A low cost RCD clamp formed by D1, R1, R2, R17 and C4 limits the peak Drain voltage due to the effects of transformer leakage reactance and output trace inductance.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C6, when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D2 and capacitor C5, and fed in the BPP pin via a current limiting resistor R6. The primary side overvoltage protection is obtained using Zener diode VR1. RC snubber circuit R16 and C18 reduced the voltage ringing across D2 therefore helps in reducing EMI. In the event of overvoltage at output, the increased voltage at the output of the bias winding cause the Zener diode VR1 to conduct and triggers the OVP protection in the primary side controller of the INN3168C IC. Resistors R3 and R4 provide line voltage sensing and provide a current to U1, which is proportional to the DC voltage across capacitor C3. At approximately 100 V DC, the current through these resistors exceeds the line under-voltage threshold, which results in enabling of U1. At approximately 450 V DC, the current through these resistors exceeds the line over-voltage threshold, which results in disabling of U1.

4.3 InnoSwitch3-CE Secondary

The secondary side of the INN3168C provides reference of the output voltage feedback, output current sensing and drive to MOSFET’s providing synchronous rectification.

Output rectification for the 5 V output is provided by SR FET Q1. Very low ESR capacitors, C11 and C12, provide filtering, and inductor L3 and capacitor C16 form a second stage filter that significantly attenuates the high frequency ripple and noise at the 5 V output. Output rectification for the 50 V output is provided by D4. Very low ESR capacitor C13 provide filtering, and inductor L4 and capacitor C14 form a second stage filter that significantly attenuates the high frequency ripple and noise at the 50 V output. Capacitor C17 reduces the radiation EMI noise.

Zener diode VR2, R14, R15 and Q2 acts as voltage clamping circuit to limit the no-load voltage across 50 V when full load is applied on 5 V output.

RC snubber networks comprising R7 and C9 for Q1 damp high frequency ringing across SRFET, which results from leakage inductance of the transformer windings and the secondary trace inductances.

The gate of Q1 is turned on based on the winding voltage sensed via R8 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold ($V_{SR(TH)}$). Secondary-side control of the primary-side MOSFET ensure that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin. The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into the VO pin and charges the decoupling capacitor C7 via an internal regulator. The unit enters auto-restart when the sensed output voltage is lower than 3 V.

Resistor R11, R12 and R13 form a voltage divider network that senses the output voltage from both outputs for better cross-regulation. The INN3168C IC has an internal reference of 1.265 V. Feed forward RC networks comprising capacitors C15, C20 and resistors R10, R18 reduce the output ripple voltage. Capacitor C8 provides decoupling from high frequency noise affecting power supply operation. Total output current is sensed by R9 with a threshold of approximately 35 mV to reduce losses. Once the current sense threshold across these resistors is exceeded, the device adjusts the number of switch pulses to maintain a fixed output current.

4.4 Design Key Points

4.4.1 Low Standby Power

Low standby power across wide range input voltage is achieved using bias winding that supplies the minimum current needed in the primary bypass pin during no load condition. The value of resistor R6 is adjusted in a manner that the current drawn from C5 towards the BPP pin is sufficient enough during no-load condition so that the InnoSwitch3-CE IC won’t draw current from the Drain pin or the bulk voltage.

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4.4.2 Average Efficiency of More Than 89% at Nominal Input Line

High average efficiency is achieved with the InnoSwitch3-CE IC by having variable frequency QR controller + CCM operation. InnoSwitch3-CE ICs feature a means to allow switching when the voltage across the primary switch is near its minimum voltage when the converter operates in critical (CRM) or discontinuous conduction mode (DCM). This mode of operation is automatically detected in CRM and DCM and disabled once the when the converter operates in continuous-conduction mode (CCM).

Transformer design is optimized to have peak flux density near 3700 Gauss by adjusting the switching frequency to 60 kHz and therefore reducing the switching losses on all the switching devices when compared in operating at higher switching frequencies. Bobbin winding area is also optimized is such a way that the wire gauge used from primary, bias, shield, and secondary winding covers the whole bobbin area to reduce the winding loss.

4.4.3 Cross Regulation

DER-571 has shared regulation for 5 V and 50 V output rail. Resistor R11 and R12 shares current towards R13 or the FB pin that helps regulate the output voltages. Values of R11 and R12 are optimized with priority on maintaining tight regulation on 5 V output rail based on specification.

A good turns ratio in the transformer design for two output voltages also helps maintain good cross regulation. Since 5 V and 50 V have a ratio of 1:10, secondary turns used in the design is 2 turns for 5 V and 20 turns for 50 V and the two secondary windings are wounded close to each other.

Low leakage inductance (<10 μH) is maintained in the transformer construction design to reduce high no-load output voltage when the other output voltage rail is at full load. Also, lower VOR and lower KP helps reduce the high no-load output voltage. For, 50 V output rail, active pre-load is connected to limit its no-load output voltage (during full load at 5 V) to less than 65 V.

5 PCB Layout

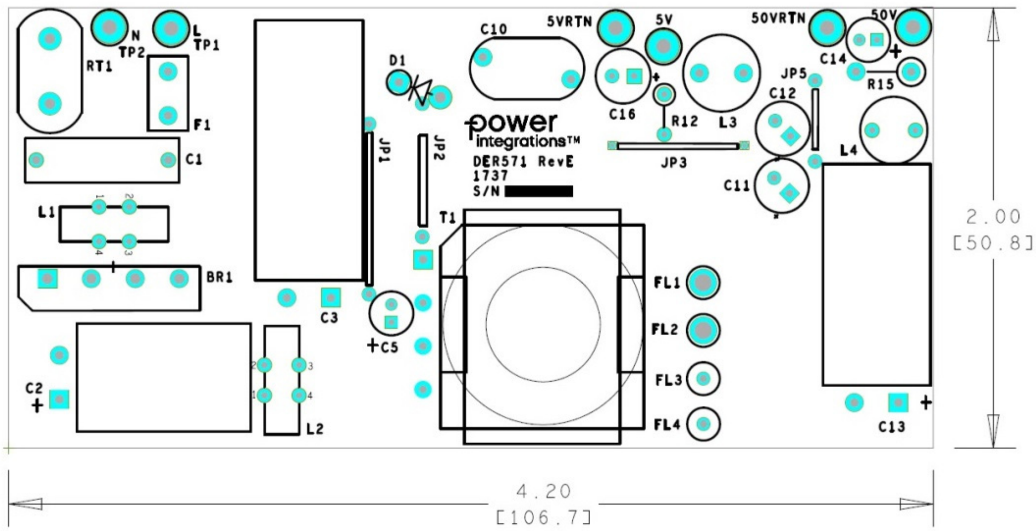

Figure 6 – Top Side.

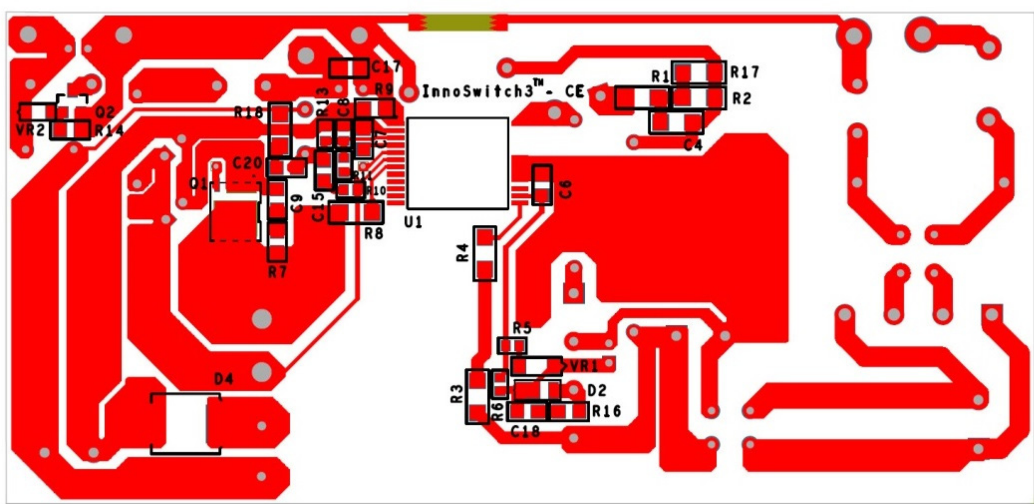

Figure 7 – Bottom Side.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	DIODE BRIDGE 600V 4A GB	GBL06	Genesic Semi
2	1	C1	100 nF, 275 VAC, Film, X2	ECQ-U2A104ML	Panasonic
3	1	C2	33 µF, 400 V, Electrolytic, (12.5 x 20)	KMG401ELL330MK20S	Nippon Chemi-Con
4	1	C3	47 µF, 400 V, Electrolytic, (12.5 x 30)	TYB2CM470J300	Ltec
5	1	C4	1 nF, 1000 V, Ceramic, X7R, 1206	CC1206KKX7RCBB102	Yageo
6	1	C5	22 µF, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
7	1	C6	4.7 µF, 50 V, Ceramic, X5R, 0805	CL21A475KBQNNNE	Samsung
8	1	C7	2.2 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
9	1	C8	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
10	1	C9	2.2 nF, 250 V, Ceramic, X7R, 0805	C2012X7R2E222K085AA	TDK
11	1	C10	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
12	1	C11	560 µF, 6.3 V, Al Organic Polymer, Gen. Purpose, 20%	RS80J561MDN1JT	Nichicon
13	1	C12	560 uF, 6.3 V, Al Organic Polymer, Gen. Purpose, 20%	RS80J561MDN1JT	Nichicon
14	1	C13	390 µF, 80 V, Electrolytic, Low ESR, (12.5 x 26.5)	EKZN800ELL391MK25S	United Chemi-Con
15	1	C14	10 µF, 63 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG630ELL100ME11D	Nippon Chemi-Con
16	1	C15	22 nF, 25 V, Ceramic, X7R, 0805	C0805C223K3RACTU	Kemet
17	1	C16	220 µF, 10 V, Electrolytic, Very Low ESR, 130 mΩ, (6.3 x 11)	EKZE100ELL221MF11D	Nippon Chemi-Con
18	1	C17	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX
19	1	C18	330 pF, 100 V, Ceroamic, COG, 0805	C0805C331K1RACTU	Kemet
20	1	C20	3.3 nF 100 V, Ceramic, X7R, 0603	C0805C332K1RACTU	Kemet
21	1	D1	600 V, 1 A, Rectifier, Glass Passivated, 2 us, DO-41	1N4005GP	Vishay
22	1	D2	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
23	1	D4	600 V, 3 A, SMC, DO-214AB	STTH3R06S	ST Micro
24	1	F1	2 A, 250 V, Slow, Long Time Lag, RST	RST 2	Belfuse
25	1	L1	10 mH, ±10%,Toroidal Common Mode Choke, custom, Wound on Toroid Core: PI 32-00275-00	32-00358-00	Power Integrations
26	1	L2	10 mH, ±10%,Toroidal Common Mode Choke, custom, Wound on Toroid Core: PI 32-00275-00	32-00358-00	Power Integrations
27	1	L3	4.7 µH, 4.2 A	RFB0807-4R7L	Coilcraft
28	1	L4	18 µH, 1.6 A, 9 x 12 mm H	AIUR-03-180K	Abracon
29	1	Q1	60 V, 40A N-Channel, DFN5X6	AON6262	Alpha & Omega Semi
30	1	Q2	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1G	On Semi
31	1	R1	RES, 33 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ330V	Panasonic
32	1	R2	RES, 402 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF4023V	Panasonic
33	1	R3	RES, 1.80 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
34	1	R4	RES, 1.80 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
35	1	R5	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
36	1	R6	RES, 20 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ203V	Panasonic
37	1	R7	RES, 5.6 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ5R6V	Panasonic
38	1	R8	RES, 47 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ470V	Panasonic
39	1	R9	RES, 0.005 Ω, 0.5 W, 1%, 0805	PMR10EZPFU5L00	Rohm
40	1	R10	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
41	1	R11	RES, 118 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1183V	Panasonic
42	1	R12	RES, 9.1 MΩ, 5%, 1/8 W, Carbon Film	CF18JT9M10	Stackpole
43	1	R13	RES, 34 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3402V	Panasonic
44	1	R14	RES, 10 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
45	1	R15	RES, 2.7 kΩ, 5%, 2 W, Metal Oxide Film	ERG-2SJ272	Panasonic
46	1	R16	RES, 100 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ101V	Panasonic

47	1	R17	RES, 402 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF4023V	Panasonic
48	1	R18	RES, 1.0 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1001V	Panasonic
49	1	RT1	NTC Thermistor, 5 Ω, 5 A	MF72-005D13	Cantherm
50	1	T1	Bobbin, EQ2506, 4 pins, 4pri, 0sec	EQ-2506	Shen Zhen Xin Yu Jia Tech
51	1	U1	InnoSwitch-3EP, InSOP24D	INN3168C-H101	Power Integrations
52	1	VR1	DIODE ZENER 15 V 500 mW SOD123	MMSZ5245B-TP	Diodes, Inc.
53	1	VR2	56 V, 2%, 300 mW, SOD323	BZX384-B56,115	NXP Semi

Miscellaneous Parts

Item	Qty	Ref Des	Description	Mfg	Mfg Part Number
1	1	50V	Test Point, ORG, THRU-HOLE MOUNT	Keystone	5013
2	1	50VRTN	Test Point, BLK, THRU-HOLE MOUNT	Keystone	5011
3	1	5V	Test Point, RED, THRU-HOLE MOUNT	Keystone	5010
4	1	5VRTN	Test Point, BLK, THRU-HOLE MOUNT	Keystone	5011
5	1	JP1	Wire Jumper, Insulated, TFE, #22 AWG, 1.0 in	Alpha	C2004-12-02
6	1	JP2	Wire Jumper, Non insulated, #22 AWG, 1.2 in	Alpha	298
7	1	JP3	Wire Jumper, Insulated, TFE, #22 AWG, 0.6 in	Alpha	C2004-12-02
8	1	JP4	Wire Jumper, Insulated, TFE, #22 AWG, 0.7 in	Alpha	C2004-12-02
9	1	TP1	Test Point, RED, THRU-HOLE MOUNT	Keystone	5010
10	1	TP2	Test Point, WHT, THRU-HOLE MOUNT	Keystone	5012

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7 Flyback Transformer (T1) Specifications

7.1 Electrical Diagram

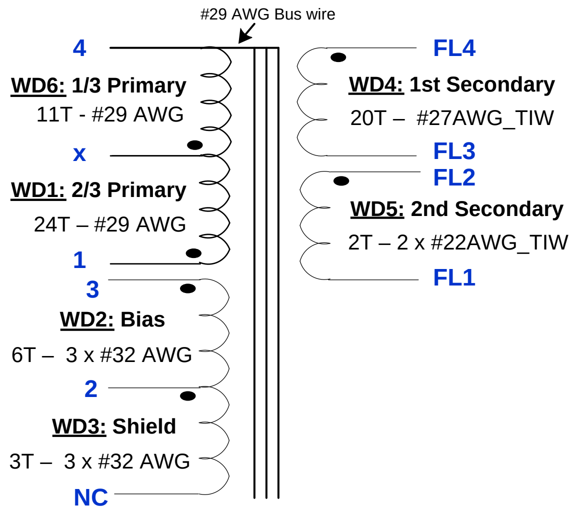

Figure 8 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, across pin 1 and pin 4, with all other windings open.	635.9 μH
Tolerance	Tolerance of Primary Inductance.	±7%
Leakage Inductance	Between pin 1 and 4, with all secondary fly leads FL1-FL4 shorted and pin 2 and 3 shorted.	10 μH (Max.)

7.3 Material List

Item	Description
[1]	Core: EQ27, Shen Zhen Xin Yu Tech Ltd.
[2]	Bobbin: EQ2506-V-4 pins (4/0); Shen Zhen Xin Yu Tech Ltd., PI#: 25-01095-00.
[3]	Magnet Wire: #29 AWG, Double Coated.
[4]	Magnet Wire: #32 AWG, Double Coated.
[5]	Magnet Wire: #22 AWG, Triple Insulated Wire.
[6]	Magnet Wire: #27 AWG, Triple Insulated Wire.
[7]	Barrier Tape: 3M 1298 Polyester Film, 1 mil Thickness, 4.5 mm Wide.
[8]	Bead: 210 Ω, 25 MHz, 3.5 x 3.25, PI#: 30-00117-00
[9]	Barrier Tape: 3M 1298 Polyester Film, 1 mil Thickness, 15 mm Wide.
[10]	Epoxy: Devcon, 5 minute, MF#: 14270; or Equivalent.
[11]	Varnish: Dolph BC-359.

7.4 Transformer Build Diagram

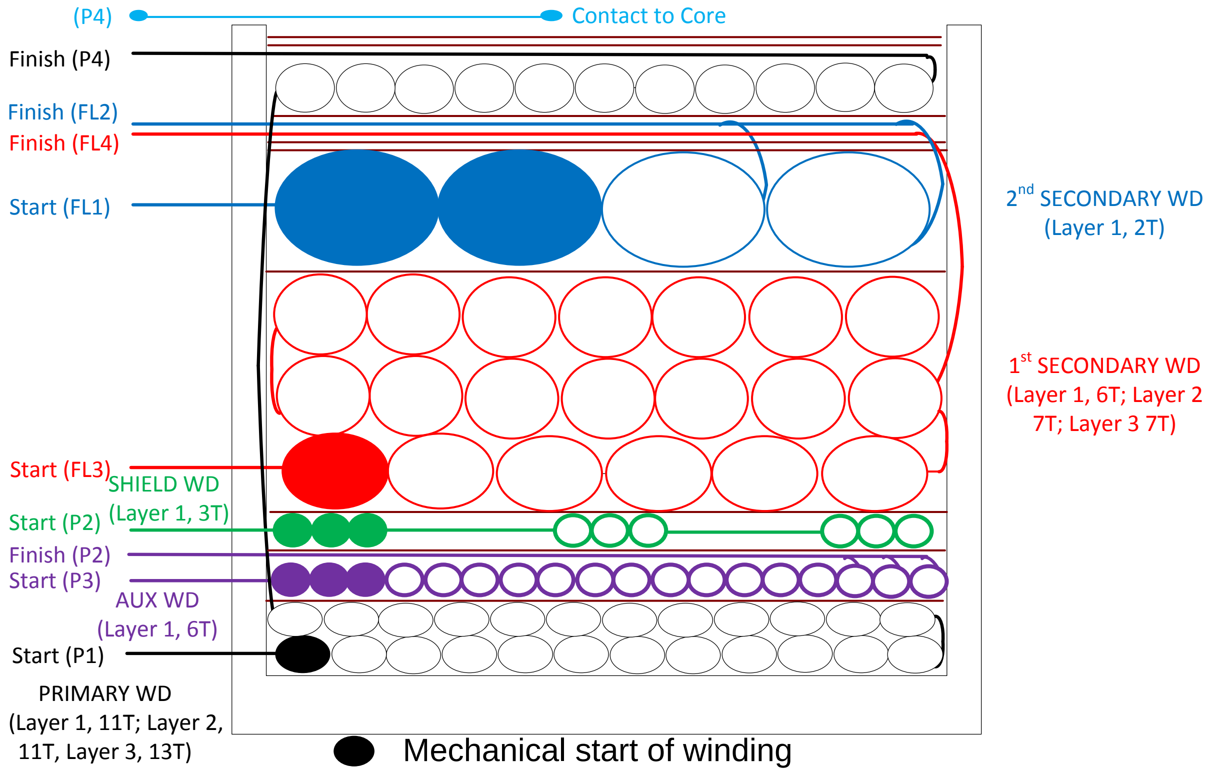

Figure 9 – Transformer Build Diagram.

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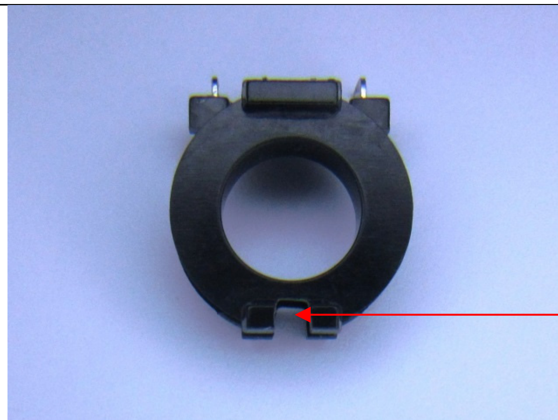
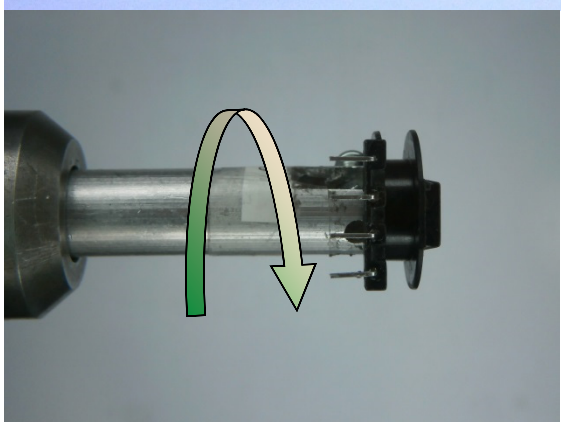
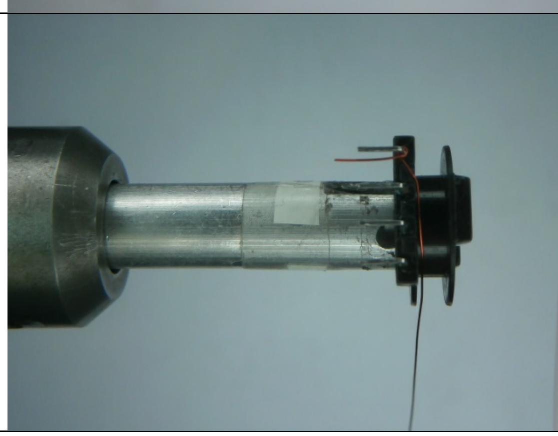
7.5 Flyback Transformer Construction

Winding Preparation	Make 2 slots ~ 3 mm width x 3.5 mm depth on the secondary flanges of the bobbin Item [2]. Then place the bobbin on the mandrel with the pin side on the left side. Winding direction is clockwise direction.
WD1 **2/3 Primary**	Start at pin 1, wind 24 turns of wire Item [3] in 2 layers with tight tension, and on the last turn leave ~1 meter of wire for WD6.
Insulation	Place 1 layer of tape Item [7] to secure this winding.
WD2 **Bias**	Start at pin 3, wind 6 trifilar turns of wire Item [4] in 1 layer.
Insulation	Place 1 layer of tape Item [7] for insulation. Bring the WD2 last turn back to pin 2 after insulation tape.
WD3 **Shield**	Start at pin 2, wind 3 trifilar turns of wire Item [4] in 1 layer and evenly distributed. Cut the end of the wire during insulation process.
Insulation	Place 1 layer of tape Item [7] for insulation.
WD4 **1st Secondary**	Use 1 wire Item [6], start the winding on the left slot in floating condition. This will be marked as FL3 as indicated in the PCB board. Wind 20 turns in COUNTER – CLOCKWISE direction and place the last turn on the right slot in floating condition. Note that the last turn is for FL4 PCB location.
Insulation	Place 1 layer of tape Item [7] to secure this winding.
WD5 **2nd Secondary**	Use 2 wire Item [5], start the winding on the left slot in floating condition. This will be marked as FL1 as indicated in the PCB board. Wind 2 turns in COUNTER – CLOCKWISE direction and place the last turn on the right slot in floating condition. Note that the last turn is for FL2 PCB location.
Insulation	Place 2 layers of tape Item [7] for insulation. After that, bend FL4 and FL1 and secure it with 1 layers of tape Item [7].
WD6 **1/3 Primary**	Continue winding 11 turns of wire left from WD1in 1 layer with tight tension and finish at pin 4.
Insulation	Place 1 layer of tape Item [7] for insulation. Bring WD6 last turn back to pin 4 after insulation tape.
Finish Assembly	Gap core halves to get 660 μH inductance. Connected bus wire Item [3] to pin 4, lean on upper portion of the core, and secure all together with tape. Insert bead Item [8] onto the wire FL3 and place 1 drop of epoxy Item [10] to keep not moving. Varnish Item [11].

7.6 Winding Illustrations

Winding Preparation	 	Make 2 slots ~ 3 mm width x 3.5 mm depth on the secondary flanges of the bobbin Item [2]. Then place the bobbin on the mandrel with the pin side on the left side. Winding direction is clockwise direction.
WD1 **2/3 Primary**		Start at pin 1, wind 24 turns of wire Item [3] in 2 layers with tight tension, and the last turn leave ~ 1 meter of wire for WD6.

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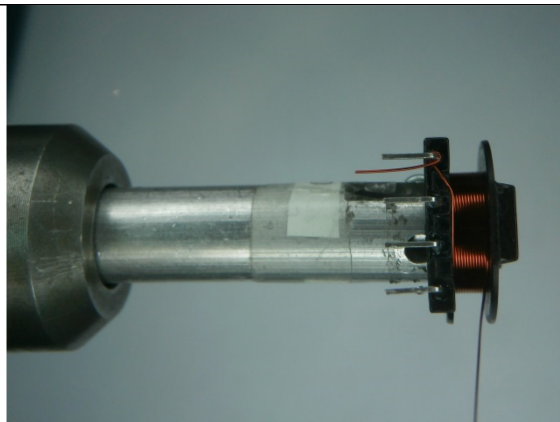
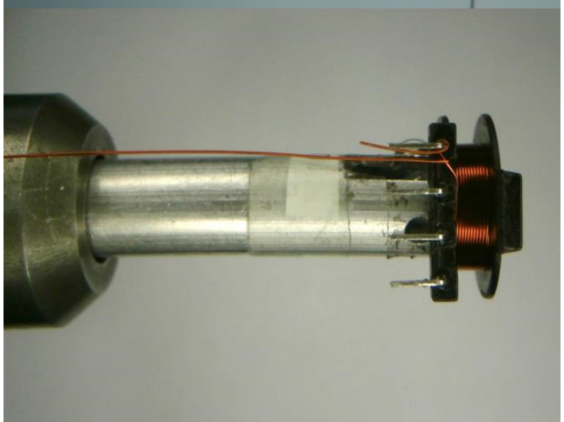
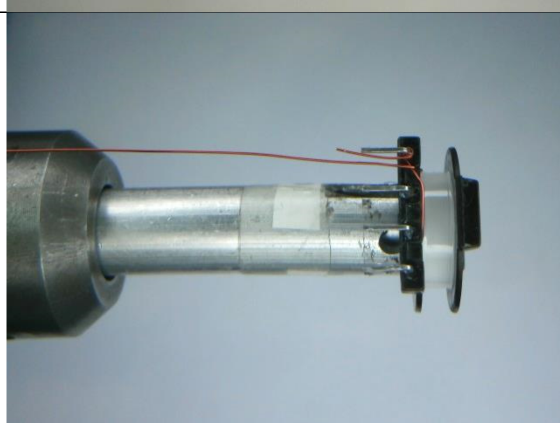
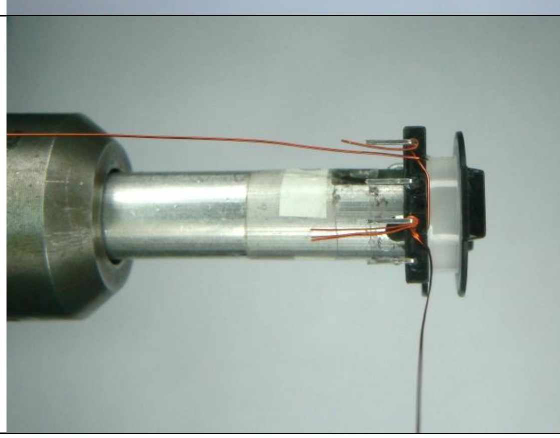
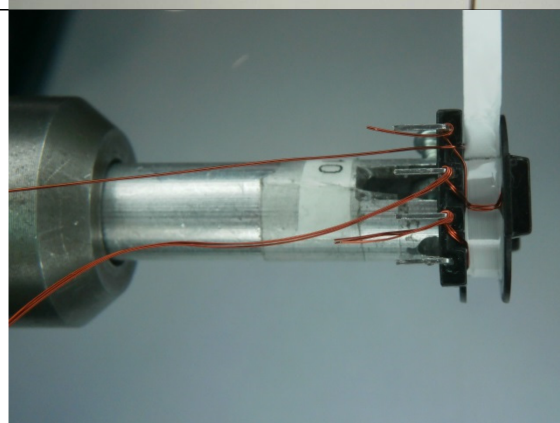
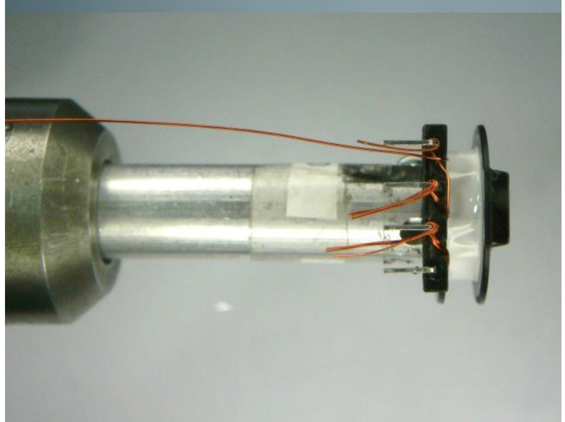
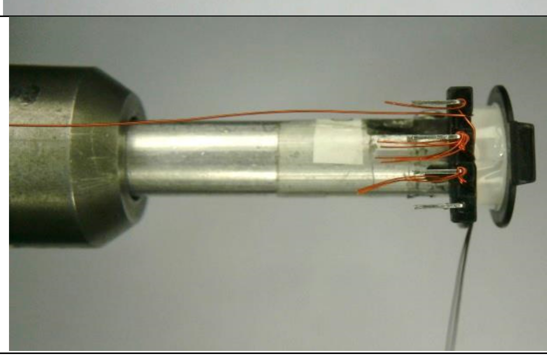
<table>
<tr><td></td><td>
</td><td></td></tr>
<tr><td>Insulation</td><td></td><td>Place 1 layer of tape Item [7] for insulation.</td></tr>
<tr><td>WD2
Bias</td><td></td><td>Start at pin 3, wind 6 trifilar turns of wire Item [4] in 1 layer.</td></tr>
</table>

		
Insulation	 	Place 1 layer of tape Item [7] for insulation. Bring the WD2 last turn back to pin 2 after insulation tape.
WD3 **Shield**		Start at pin 2, wind 3 trifilar turns of wire Item [4] in 1 layer and evenly distributed. Cut the end of the wire during insulation process.

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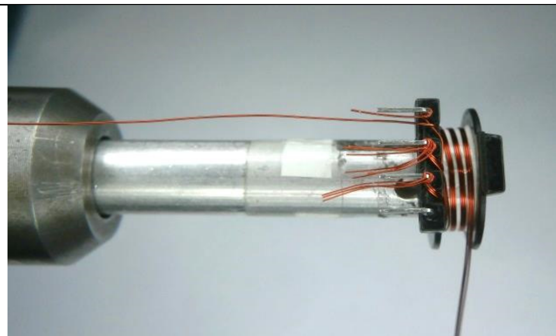
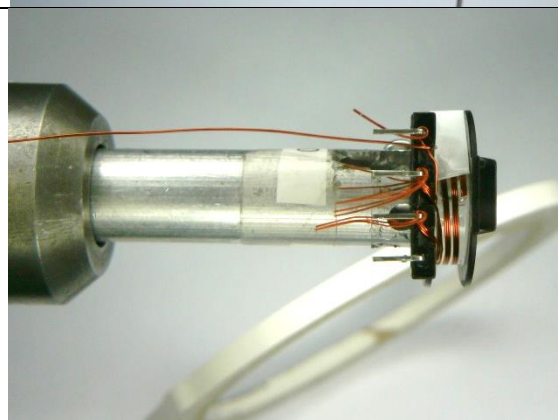
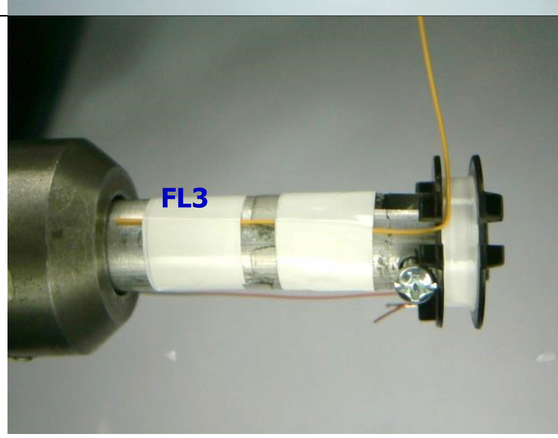
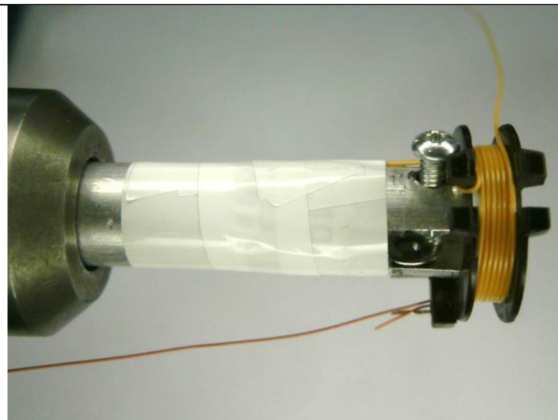
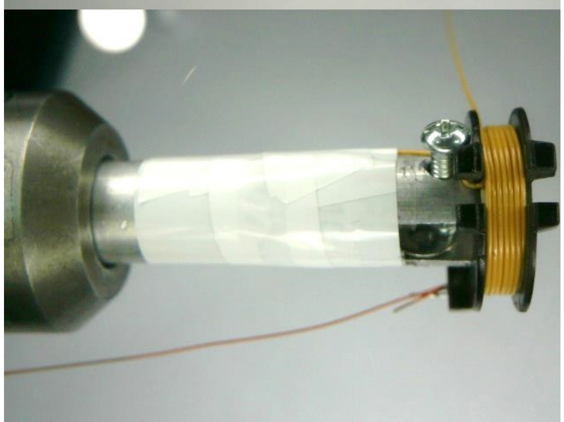
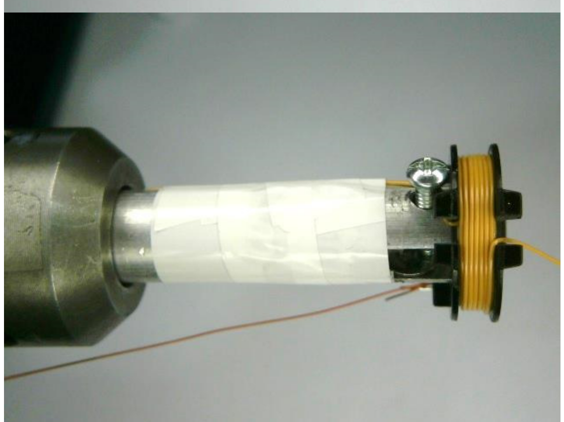
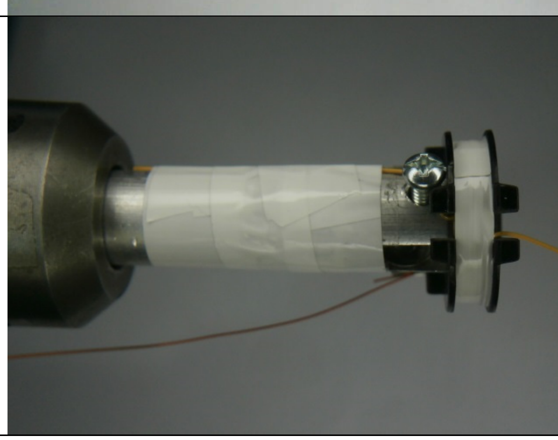
		
Insulation	 	Place 1 layer of tape Item [7] for insulation.
WD4 **1st Secondary**	 o	Use 1 wire Item [6], start the winding on the left slot in floating condition. This will be marked as FL3 as indicated in the PCB board. Wind 20 turns in COUNTER – CLOCKWISE direction and place the last turn on the right slot in floating condition. Note that the last turn is for FL4 PCB location.

	  	
Insulation		Place 1 layer of tape Item [7] to secure this winding.

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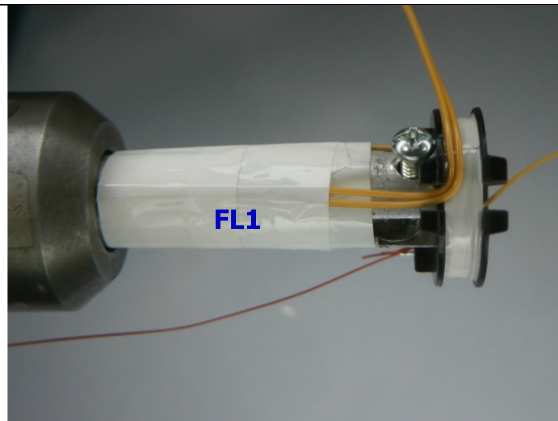
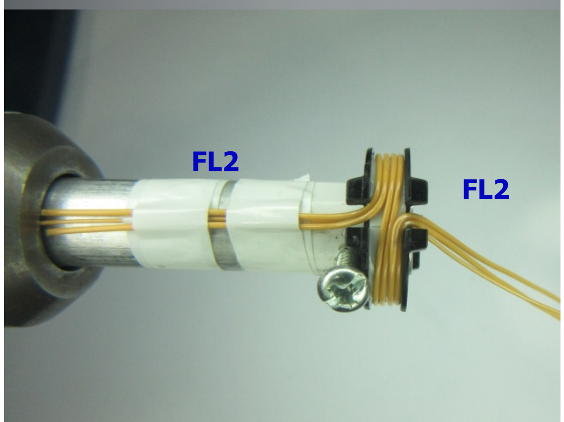
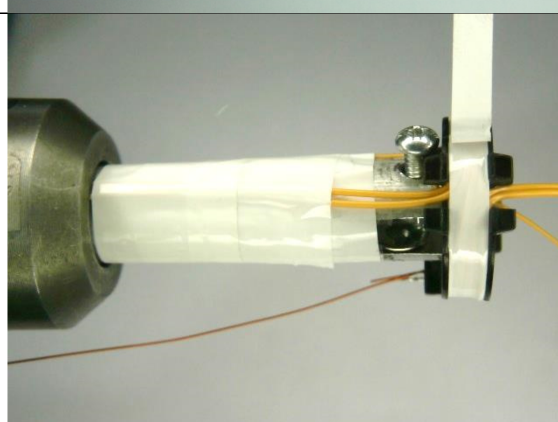
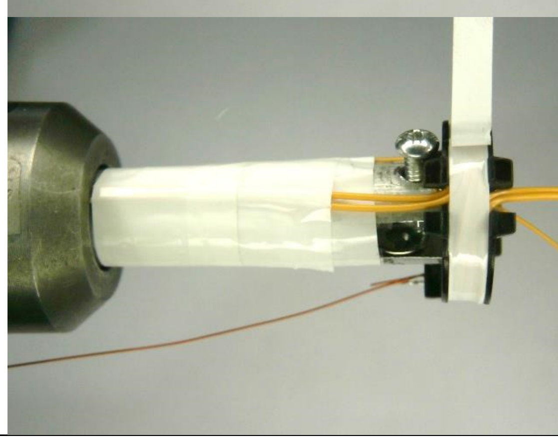
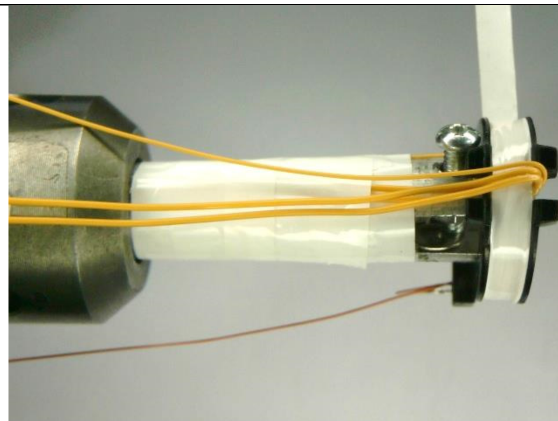
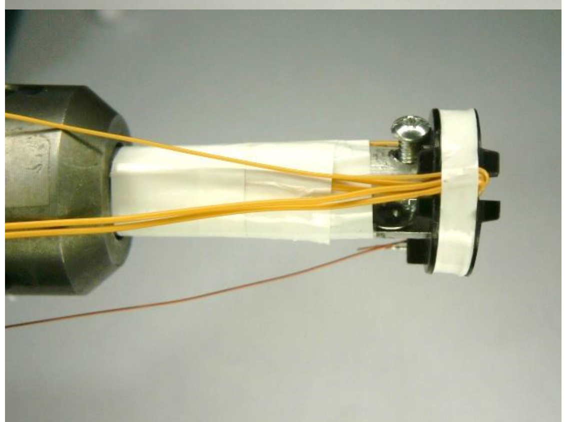
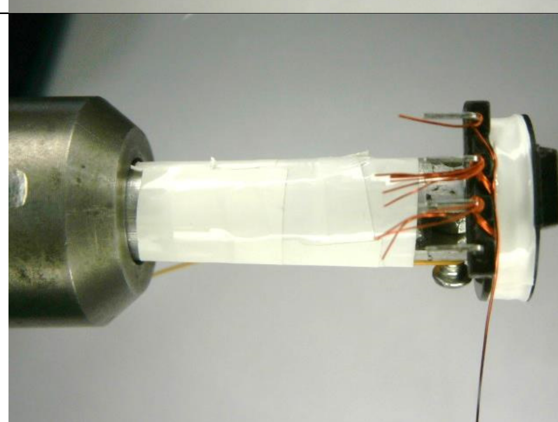
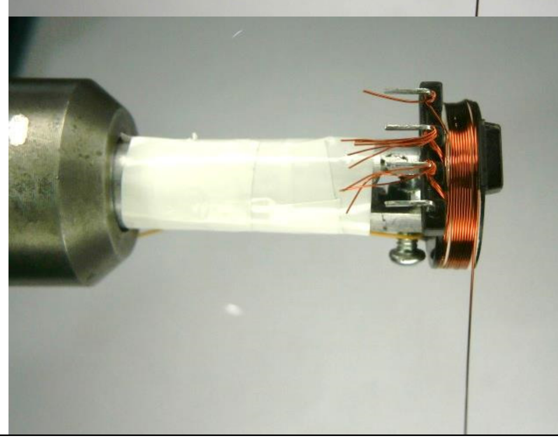
<table>
<tr>
<td>WD5
2nd Secondary</td>
<td>


</td>
<td>Use 2 wire Item [5], start the winding on the left slot in floating condition. This will be marked as FL1 as indicated in the PCB board. Wind 2 turns in COUNTER – CLOCKWISE direction and place the last turn on the right slot in floating condition. Note that the last turn is for FL2 PCB location.</td>
</tr>
<tr>
<td>Insulation</td>
<td>
</td>
<td>Place 2 layers of tape Item [7] for insulation. After that, bend FL4 and FL1 and secure it with 1 layers of tape Item [7].</td>
</tr>
</table>

	 	
WD6 **1/3 Primary**	 	Continue winding 11 turns of wire left from WD1in 1 layer with tight tension and finish at pin 4.

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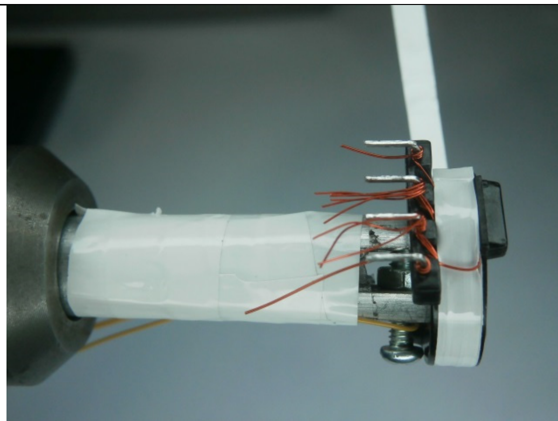
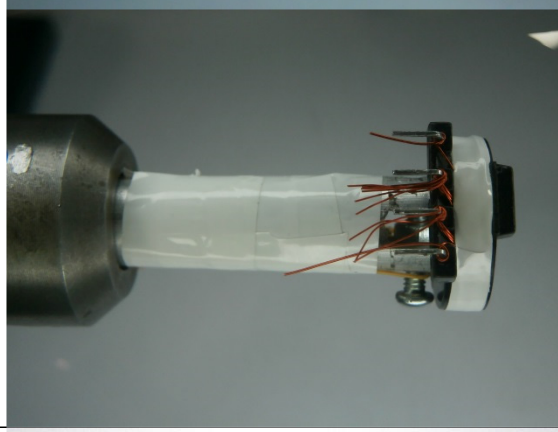
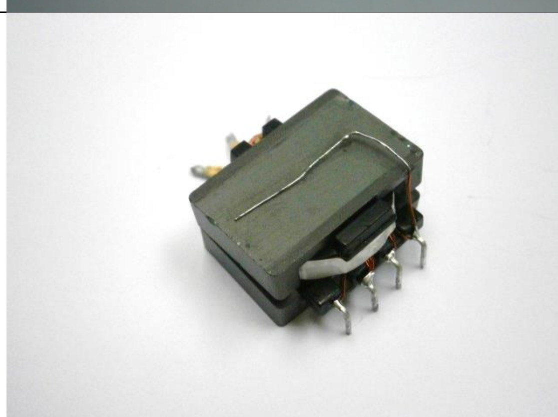
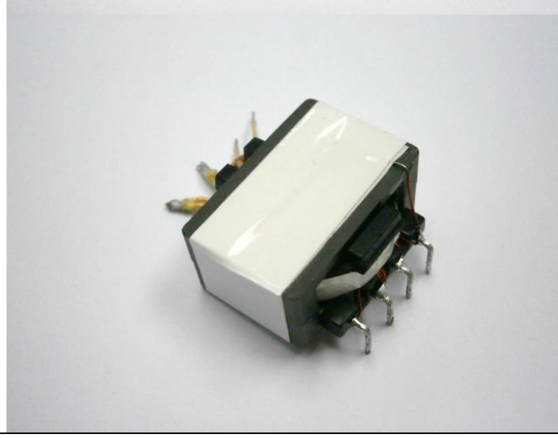
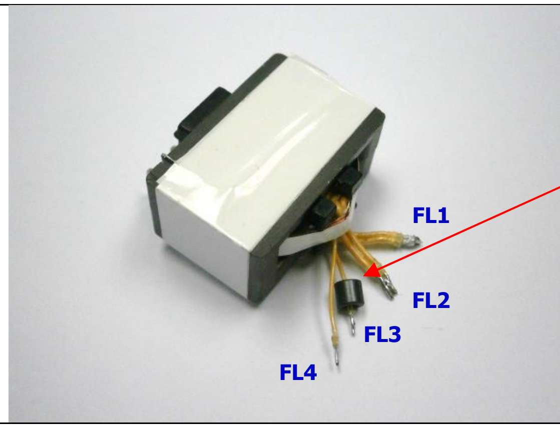
Insulation	 	Place 1 layer of tape Item [7] for insulation. Bring WD6 last turn back to pin 4 after insulation tape.
Finish Assembly	 	Gap core halves to get 660 μH inductance. Connected bus wire Item [3] to pin 4, lean on upper portion of the core, and secure all together with tape Item [9].

		Insert bead Item [8] onto the wire FL4 and place 1 drop of epoxy Item [10] to keep not moving. Varnish Item [11].

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8 Transformer Design Spreadsheet

1	**ACDC_InnoSwitch3-CE_Flyback_083017; Rev.1.0; Copyright Power Integrations 2017**	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**InnoSwitch3 CE Flyback Design Spreadsheet**
2	**APPLICATION VARIABLES**					
3	VIN_MIN	90		90	V	Minimum AC input voltage
4	VIN_MAX	265		265	V	Maximum AC input voltage
5	VIN_RANGE			UNIVERSAL		Range of AC input voltage
6	LINEFREQ			60	Hz	AC Input voltage frequency
7	CAP_INPUT	80.0		80.0	uF	Input capacitor
8	VOUT	50.00		50.00	V	Output voltage at the board
9	PERCENT_CDC	0%		0%		Percentage (of output voltage) cable drop compensation desired at full load
10	IOUT	0.80		0.80	A	Output current
11	POUT			40.00	W	Output power
12	EFFICIENCY	0.89		0.89		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.50		Z-factor estimate
14	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
15						
16						
17						
18	**PRIMARY CONTROLLER SELECTION**					
19	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
20	DEVICE_GENERIC	INN31X8		INN31X8		Generic device code
21	DEVICE_CODE			INN3168C		Actual device code
22	POUT_MAX			55	W	Power capability of the device based on thermal performance
23	RDSON_100DEG			1.53	Ω	Primary MOSFET on time drain resistance at 100 degC
24	ILIMIT_MIN			1.68	A	Minimum current limit of the primary MOSFET
25	ILIMIT_TYP			1.85	A	Typical current limit of the primary MOSFET
26	ILIMIT_MAX			2.02	A	Maximum current limit of the primary MOSFET
27	VDRAIN_BREAKDOWN			650	V	Device breakdown voltage
28	VDRAIN_ON_MOSFET			0.69	V	Primary MOSFET on time drain voltage
29	VDRAIN_OFF_MOSFET			530.4	V	Peak drain voltage on the primary MOSFET during turn-off
30						
31						
32						
33	**WORST CASE ELECTRICAL PARAMETERS**					
34	FSWITCHING_MAX	60000		60000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
35	VOR	87.0		87.0	V	Seconday voltage reflected to the primary when the primary MOSFET turns off
36	VMIN			95.02	V	Valley of the rectified minimum AC input voltage at full power
37	KP			0.79		Measure of continuous/discontinuous mode of operation
38	MODE_OPERATION			CCM		Mode of operation
39	DUTYCYCLE			0.480		Primary MOSFET duty cycle
40	TIME_ON			11.61	us	Primary MOSFET on-time
41	TIME_OFF			8.67	us	Primary MOSFET off-time

42	LPRIMARY_MIN			591.3	uH	Minimum primary inductance
43	LPRIMARY_TYP			635.9	uH	Typical primary inductance
44	LPRIMARY_TOL	7.0		7.0	%	Primary inductance tolerance
45	LPRIMARY_MAX			680.4	uH	Maximum primary inductance
46						
47	**PRIMARY CURRENT**					
48	IPEAK_PRIMARY			1.78	A	Primary MOSFET peak currrent
49	IPEDESTAL_PRIMARY			0.33	A	Primary MOSFET current pedestal
50	IAVG_PRIMARY			0.45	A	Primary MOSFET average current
51	IRIPPLE_PRIMARY			1.69	A	Primary MOSFET ripple current
52	IRMS_PRIMARY			0.73	A	Primary MOSFET RMS current
53						
54	**SECONDARY CURRENT**					
55	IPEAK_SECONDARY			3.12	A	Secondary winding peak current
56	IPEDESTAL_SECONDARY			0.57	A	Secondary winding current pedestal
57	IRMS_SECONDARY			1.46	A	Secondary winding RMS current
58						
59						
60						
61	**TRANSFORMER CONSTRUCTION PARAMETERS**					
62	CORE SELECTION					
63	CORE	Custom		Custom		Core selection
64	CORE CODE	EQ27		EQ27		Core code
65	AE	108.00		108.00	mm^2	Core cross sectional area
66	LE	36.30		36.30	mm	Core magnetic path length
67	AL	3000		3000	nH/turns^2	Ungapped core effective inductance
68	VE	3920.4		3920.4	mm^3	Core volume
69	BOBBIN	EQ27		EQ27		Bobbin
70	AW	95.00		95.00	mm^2	Window area of the bobbin
71	BW	10.00		10.00	mm	Bobbin width
72	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
73						
74	**PRIMARY WINDING**					
75	NPRIMARY			35		Primary turns
76	BPEAK			3716	Gauss	Peak flux density
77	BMAX			3138	Gauss	Maximum flux density
78	BAC			1237	Gauss	AC flux density
79	ALG			519	nH/turns^2	Typical gapped core effective inductance
80	LG			0.216	mm	Core gap length
81	LAYERS_PRIMARY	3		3		Number of primary layers
82	AWG_PRIMARY	29	Info	29	AWG	Overwriting the primary AWG may not guarantee the required number of layers as calculated by the spreadsheet
83	OD_PRIMARY_INSULATED			0.337	mm	Primary winding wire outer diameter with insulation
84	OD_PRIMARY_BARE			0.286	mm	Primary winding wire outer diameter without insulation
85	CMA_PRIMARY		Warning	173	Cmil/A	The primary winding wire CMA is less than 200 mil^2/Amperes: Increase the primary layers or wire thickness
86						
87	**SECONDARY WINDING**					
88	NSECONDARY	20		20		Secondary turns
89	AWG_SECONDARY			25	AWG	Secondary winding wire AWG
90	OD_SECONDARY_INSULATED			0.760	mm	Secondary winding wire outer diameter with insulation
91	OD_SECONDARY_BARE			0.455	mm	Secondary winding wire outer diameter without insulation
92	CMA_SECONDARY			240	Cmil/A	Secondary winding wire CMA

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93						
94	**BIAS WINDING**					
95	NBIAS			6		Bias turns
96						
97						
98						
99	**PRIMARY COMPONENTS SELECTION**					
100	**Line undervoltage**					
101	BROWN-IN REQURED	62.0		62.0	V	Required AC RMS line voltage brown-in threshold
102	RLS			3.64	MΩ	Connect two 1.82 MOhm resistors to the V-pin for the required UV/OV threshold
103	BROWN-IN ACTUAL			62.1	V	Actual AC RMS brown-in threshold
104	BROWN-OUT ACTUAL			57.0	V	Actual AC RMS brown-out threshold
105						
106	**Line overvoltage**					
107	OVERVOLTAGE_LINE			273.3	V	Actual AC RMS line over-voltage threshold
108						
109	**Bias diode**					
110	VBIAS			12.0	V	Rectified bias voltage
111	VF_BIAS			0.70	V	Bias winding diode forward drop
112	VREVERSE_BIASDIODE			76.01	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
113	CBIAS			22	uF	Bias winding rectification capacitor
114	CBPP			4.70	uF	BPP pin capacitor
115						
116						
117						
118	**SECONDARY COMPONENTS**					
119	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
120	RFB_LOWER			2.61	kΩ	Lower feedback resistor
121	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
122						
123						
124						
125	**MULTIPLE OUTPUT PARAMETERS**					
126	**OUTPUT 1**					
127	VOUT1			50.00	V	Output 1 voltage
128	IOUT1	0.50		0.50	A	Output 1 current
129	POUT1			25.00	W	Output 1 power
130	IRMS_SECONDARY1			0.83	A	Root mean squared value of the secondary current for output 1
131	IRIPPLE_CAP_OUTPUT 1			0.67	A	Current ripple on the secondary waveform for output 1
132	AWG_SECONDARY1			27	AWG	Wire size for output 1
133	OD_SECONDARY1_INSULATED			0.666	mm	Secondary winding wire outer diameter with insulation for output 1
134	OD_SECONDARY1_BARE			0.361	mm	Secondary winding wire outer diameter without insulation for output 1
135	CM_SECONDARY1			167	Cmils	Bare conductor effective area in circular mils for output 1
136	NSECONDARY1			20		Number of turns for output 1
137	VREVERSE_RECTIFIER 1			263.35	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
138	SRFET1	Auto		AON7254		SRFET selection for output 1
139	VF_SRFET1			0.033	V	SRFET on-time drain voltage for output 1
140	VBREAKDOWN_SRFET 1			150	V	SRFET breakdown voltage for output 1
141	RDSON_SRFET1			66.0	mΩ	SRFET on-time drain resistance at 25degC

						and VGS=4.4V for output 1
142						
143	**OUTPUT 2**					
144	VOUT2	5.00		5.00	V	Output 2 voltage
145	IOUT2	3.00		3.00	A	Output 2 current
146	POUT2			15.00	W	Output 2 power
147	IRMS_SECONDARY2			5.01	A	Root mean squared value of the secondary current for output 2
148	IRIPPLE_CAP_OUTPUT2			4.01	A	Current ripple on the secondary waveform for output 2
149	AWG_SECONDARY2			20	AWG	Wire size for output 2
150	OD_SECONDARY2_INSULATED			1.118	mm	Secondary winding wire outer diameter with insulation for output 2
151	OD_SECONDARY2_BARE			0.812	mm	Secondary winding wire outer diameter without insulation for output 2
152	CM_SECONDARY2			1001	Cmils	Bare conductor effective area in circular mils for output 2
153	NSECONDARY2			2		Number of turns for output 2
154	VREVERSE_RECTIFIER2			26.34	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 2
155	SRFET2	Auto		AO4484		SRFET selection for output 2
156	VF_SRFET2			0.038	V	SRFET on-time drain voltage for output 2
157	VBREAKDOWN_SRFET2			40	V	SRFET breakdown voltage for output 2
158	RDSON_SRFET2			12.5	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 2
159						
160	**OUTPUT 3**					
161	VOUT3			0.00	V	Output 3 voltage
162	IOUT3			0.00	A	Output 3 current
163	POUT3			0.00	W	Output 3 power
164	IRMS_SECONDARY3			0.00	A	Root mean squared value of the secondary current for output 3
165	IRIPPLE_CAP_OUTPUT3			0.00	A	Current ripple on the secondary waveform for output 3
166	AWG_SECONDARY3			0	AWG	Wire size for output 3
167	OD_SECONDARY3_INSULATED			0.000	mm	Secondary winding wire outer diameter with insulation for output 3
168	OD_SECONDARY3_BARE			0.000	mm	Secondary winding wire outer diameter without insulation for output 3
169	CM_SECONDARY3			0	Cmils	Bare conductor effective area in circular mils for output 3
170	NSECONDARY3			0		Number of turns for output 3
171	VREVERSE_RECTIFIER3			0.00	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 3
172	SRFET3	Auto		NA		SRFET selection for output 3
173	VF_SRFET3			NA	V	SRFET on-time drain voltage for output 3
174	VBREAKDOWN_SRFET3			NA	V	SRFET breakdown voltage for output 3
175	RDSON_SRFET3			NA	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 3
176						
177	PO_TOTAL			40.00	W	Total power of all outputs
178	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2
179						
180						
181						
182	**TOLERANCE ANALYSIS**					
183	CORNER_VAC			90	V	Input AC RMS voltage corner to be evaluated

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184	CORNER_ILIMIT	TYP		1.85	A	Current limit corner to be evaluated
185	CORNER_LPRIMARY	TYP		635.9	uH	Primary inductance corner to be evaluated
186	MODE_OPERATION			CCM		Mode of operation
187	KP			0.873		Measure of continuous/discontinuous mode of operation
188	FSWITCHING			48925	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
189	DUTYCYCLE			0.480		Steady state duty cycle
190	TIME_ON			9.81	us	Primary MOSFET on-time
191	TIME_OFF			10.63	us	Primary MOSFET off-time
192	IPEAK_PRIMARY			1.67	A	Primary MOSFET peak currrent
193	IPEDESTAL_PRIMARY			0.21	A	Primary MOSFET current pedestal
194	IAVERAGE_PRIMARY			0.45	A	Primary MOSFET average current
195	IRIPPLE_PRIMARY			1.45	A	Primary MOSFET ripple current
196	IRMS_PRIMARY			0.71	A	Primary MOSFET RMS current
197	CMA_PRIMARY			178	Cmil/A	Primary winding wire CMA
198	BPEAK			3185	Gauss	Peak fux density
199	BMAX			2802	Gauss	Maximum flux density

NOTE:
Line 82 – Actual winding construction has 3 layers.
Line 85 – Efficiency was met even using thinner wire gauge the transformer temperature is still within specifications.
Line 138 – Actual part used is STTH3R06S since there's no available logic FET with V_{GS} 6 V and V_{DS} of 600 V rating available.
Line 155 – Actual part used is AON6262 since V_{DS} during 265 VAC Full load condition is around 51 V.

9 10 mH (L1 and L2) Common Mode Choke Specification

9.1 Electrical Diagram

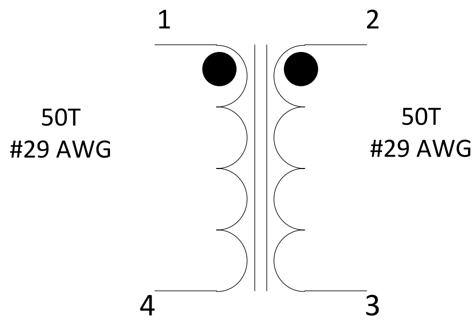


Figure 10 – Inductor Electrical Diagram.

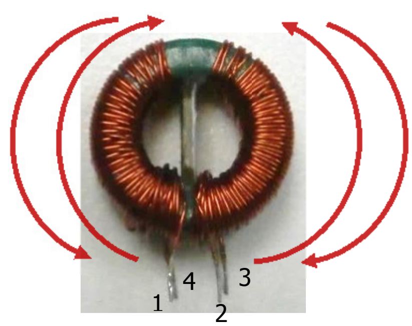
9.2 Electrical Specifications

Inductance	Pins 1-4 and pins 2-3 measured at 100 kHz, 0.4 V_{RMS}.	10.0 mH ±25%
Core effective Inductance		5110 nH/N^2
Primary Leakage Inductance	Pins 1-4, with 2-3 shorted.	100 µH

9.3 Material List

Item	Description
[1]	Toroid: FERRITE INDUCTOR TOROID T14.9 x 6.5 x 8. Manufacturing Part number: T14*8*5.5C-JL10 (PI p/n 32-00358-00)
	Divider -- Fish Paper, Insulating Cotton Rag, 0.010" thick, PI #: 66-00042-00. Cut to size 8.5 mm x 5.3 mm (L x W).
[2]	Magnet Wire: #29 AWG Heavy Nyleze

9.4 Illustrations



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10 Performance Data

All measurements were performed at room temperature.

10.1 Full Load Efficiency vs. Line

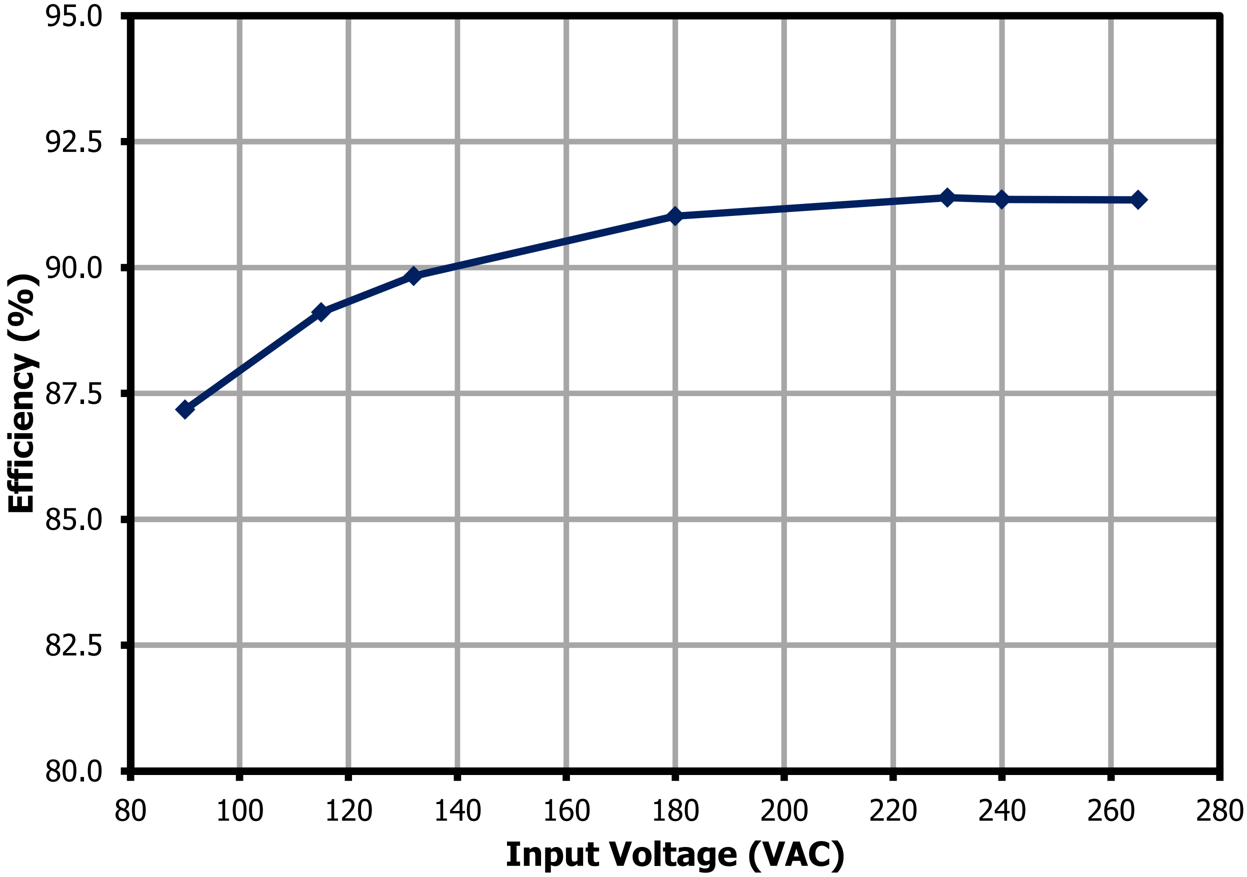

Figure 11 – Full Load Efficiency vs. Line Voltage at 25 ºC.

10.2 Average Efficiency

Loading condition: 25%, 50%, 75%, 100%

V_{IN}	P_{IN}	5 V Output		50 V Output		P_{OUT}	η	Average
		V_{OUT}	I_{OUT}	V_{OUT}	I_{OUT}			
(VAC)	(W)	(V)	(A)	(V)	(A)	(W)	(%)	η (%)
90	45.98	4.96	3.00	50.28	0.50	39.90	86.98	88.40
	33.89	4.98	2.25	50.19	0.38	30.01	88.52	
	22.45	5.02	1.50	50.28	0.25	20.09	88.04	
	11.15	5.05	0.75	50.26	0.13	10.07	90.07	
115	45.44	5.01	3.00	50.74	0.50	40.37	88.84	89.79
	33.46	4.99	2.25	50.32	0.38	30.08	89.89	
	22.23	5.02	1.50	50.37	0.25	20.11	89.56	
	11.06	5.05	0.75	50.28	0.13	10.05	90.84	
230	44.10	4.98	3.00	50.46	0.50	40.16	91.06	91.22
	33.07	5.02	2.25	50.58	0.37	30.23	91.42	
	22.03	5.04	1.50	50.52	0.25	20.16	91.30	
	11.03	5.05	0.75	50.25	0.13	10.05	91.13	
264	44.17	5.00	3.00	50.63	0.50	40.28	91.20	91.19
	33.09	5.02	2.25	50.63	0.38	30.27	91.47	
	22.07	5.05	1.50	50.57	0.25	20.19	91.38	
	11.08	5.05	0.75	50.27	0.13	10.05	90.70	

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10.3 Line Regulation at Full Load

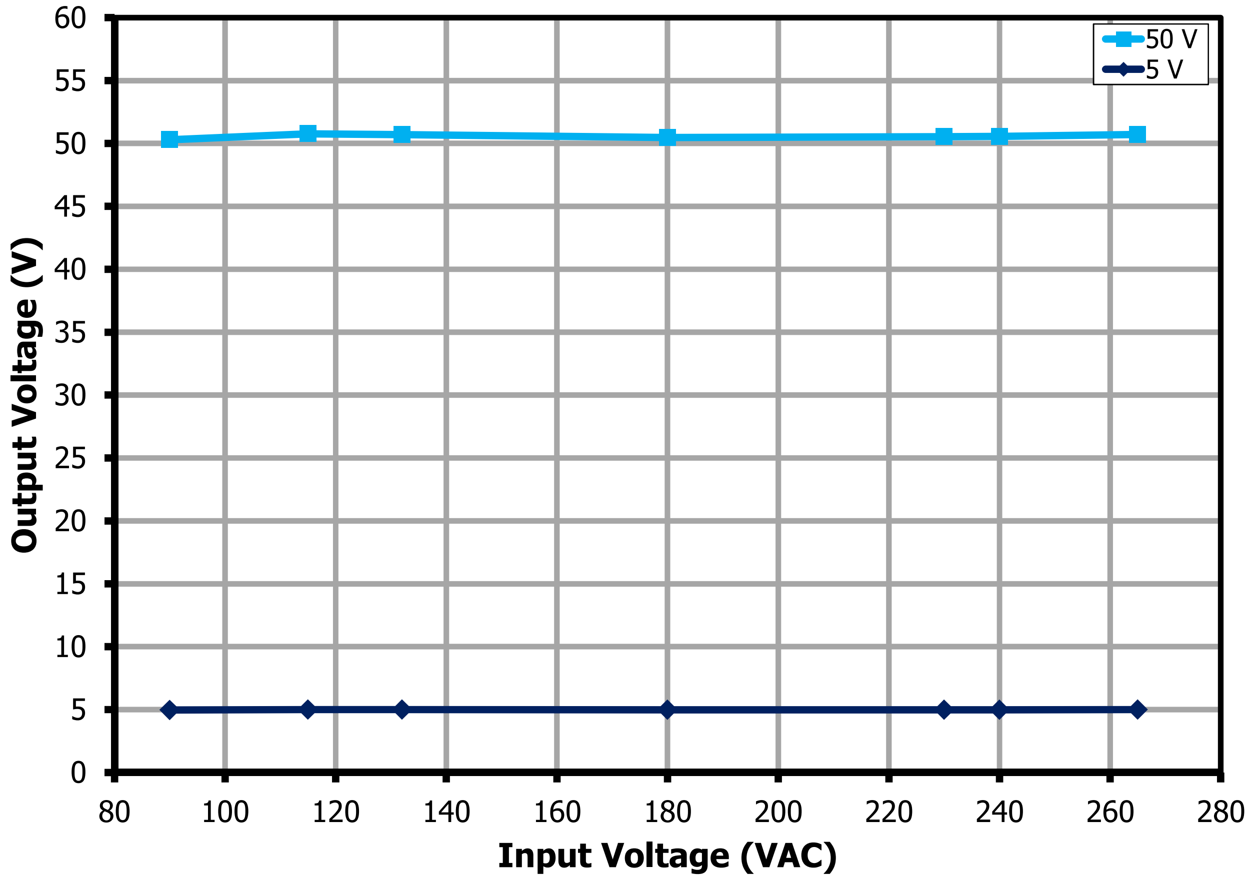

Figure 12 – Output Voltage vs Line at 25 ºC.

10.4 5 V Output Load Regulation

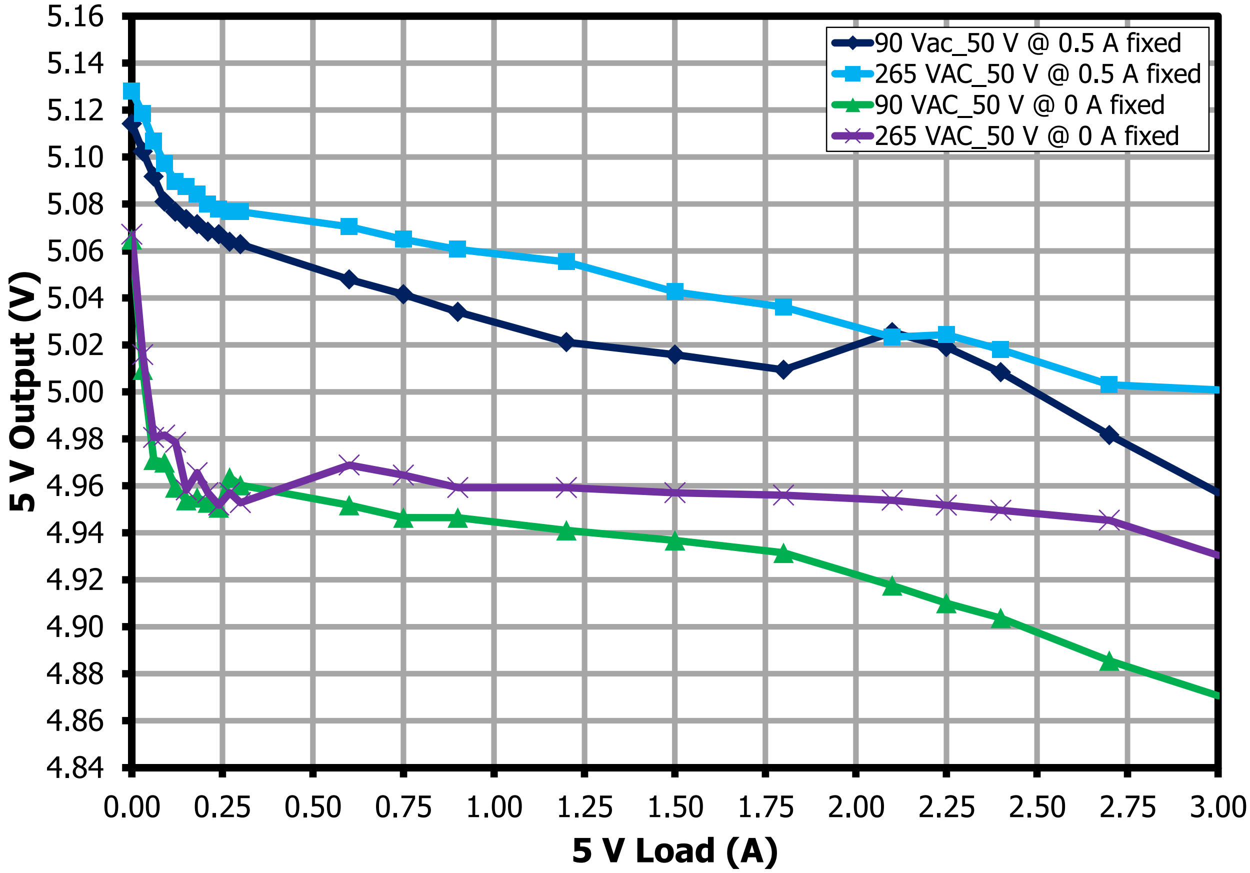

Figure 13 – 5 V output vs. 5 V Load at 25 ºC.

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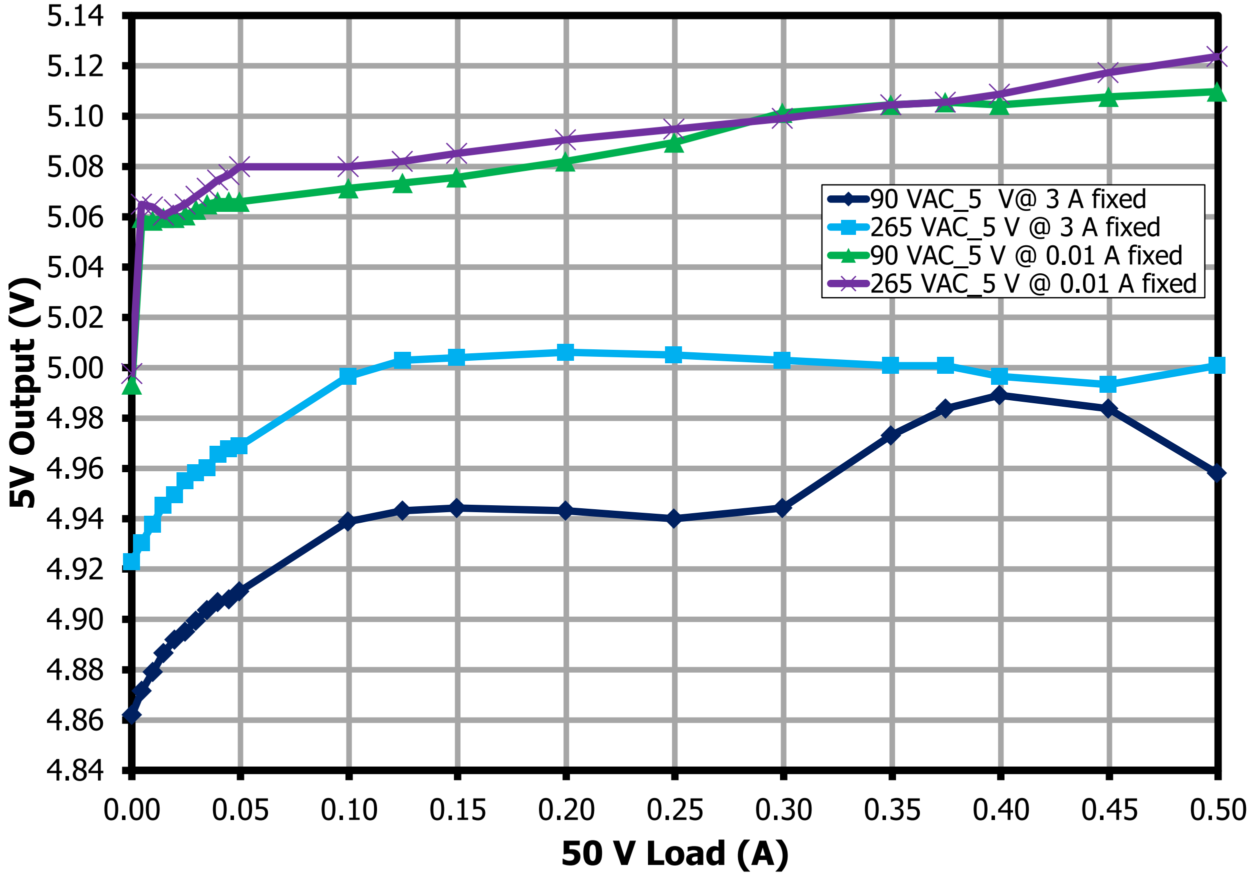

Figure 14 – 5 V output vs. 50 V Load at 25 ºC.

10.5 50 V Output Load Regulation

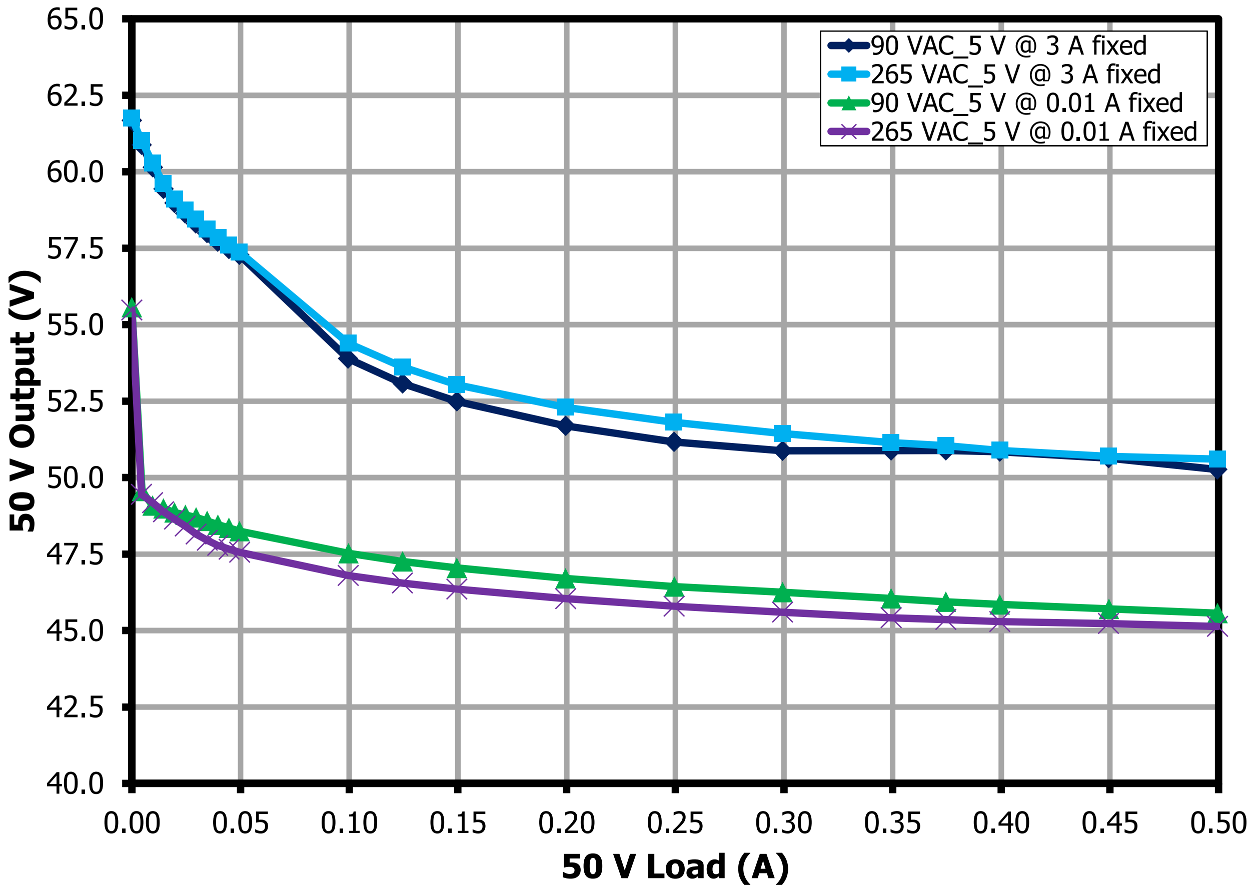

Figure 15 – 50 V output vs. 50 V Load at 25 ºC.

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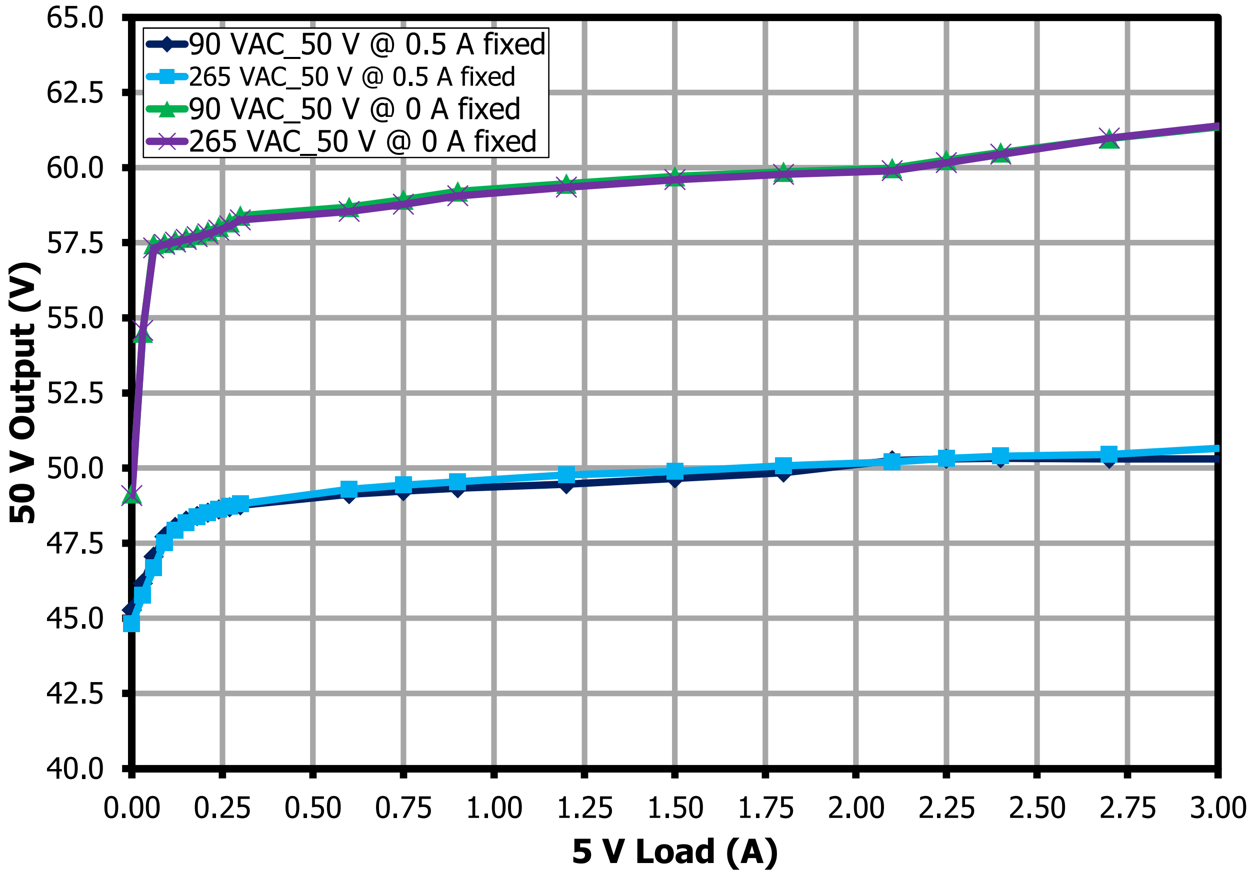

Figure 16 – 50 V output vs. 5 V Load at 25 ºC.

10.6 Input No-Load and Light Load Input Power

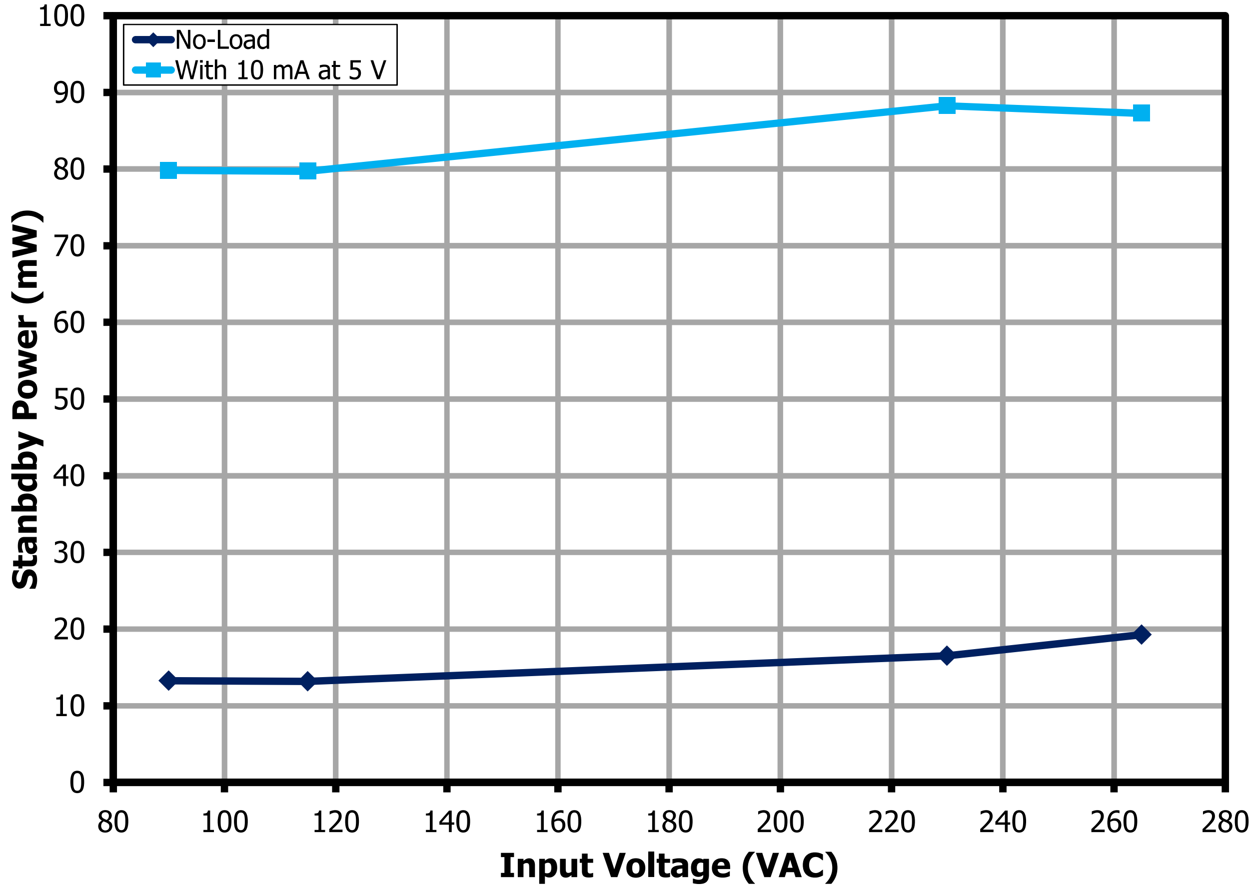

Figure 17 – No-Load and Light Load Input Power at 25 ºC.

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11 Thermal Measurement Set-Up

Equipment used:

1. Agilent 6812B AC Power Source/Analyzer
2. Chroma 6314A DC Electronic Load Mainframe and Chroma 63113A DC Electronic Load
3. Yokogawa GP20 Data Logger
4. Yokogawa WT310E Digital Power Meter
5. TPS Tenney Thermal Chamber

Figure 18 – Test Set-up Picture.

Open frame unit was placed inside the enclosure to prevent airflow that may affect the thermal measurements. Ambient temperature inside enclosure is set at 25 ºC and 40 ºC. Temperature was measured using T-type thermocouple. Soak time at full load is more than 1 hour.

11.1 Room Temperature Thermal Data

Circuit Code	Description	Thermal Reading at Room Temp			
		90 VAC	115 VAC	230 VAC	265 VAC
AMBIENT		27.4	26.3	26.1	26.7
RT1	Thermistor	78.5	70.4	53.4	51.6
C1	X-Capacitor	58.3	51.5	41.0	40.8
L1	Common Mode Choke	80.5	67.1	47.1	45.9
BR1	Bridge Diode	74.7	63.7	46.4	45.4
C2	Bulk Capacitor	54.1	47.6	38.9	39.0
L2	Common Mode Choke	58.2	51.2	42.3	42.3
C3	Bulk Capacitor	55.8	50.9	44.1	44.3
C5	Bias Capacitor	57.0	53.4	49.4	50.0
D1	Primary Snubber	70.4	64.5	57.2	57.3
T1	Flyback Transformer	61.6	59.1	57.6	58.4
C11	Output Capacitor	58.1	55.5	54.1	54.6
C12	Output Capacitor	57.3	54.6	53.2	53.9
L3	Output Inductor	63.4	60.9	59.2	60.2
C16	Output Capacitor	54.3	51.5	49.1	49.9
C13	Output Capacitor	45.0	42.5	41.6	42.9
L4	Output Inductor	45.5	42.9	42.2	43.7
C14	Output Capacitor	42.6	40.1	39.4	40.8
U1	InnoSwitch3-CE INN3168C	75.6	66.8	57.9	59.1
Q1	SR FET	62.0	59.6	57.6	57.6
D4	Ultrafast Diode	70.3	68.7	67.6	67.0

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11.2 40 ºC Ambient Thermal Data

Circuit Code	Description	Thermal Reading at Room Temp			
		90 VAC	115 VAC	230 VAC	265 VAC
AMBIENT		40.4	40.8	40.7	40.8
RT1	Thermistor	85.4	78.3	63.7	61.7
C1	X-Capacitor	70.0	64.1	54.4	53.5
L1	Common Mode Choke	91.6	79.5	60.8	58.9
BR1	Bridge Diode	86.2	76.0	59.7	58.1
C2	Bulk Capacitor	66.0	60.7	52.5	51.9
L2	Common Mode Choke	71.3	64.7	56.2	55.8
C3	Bulk Capacitor	68.9	64.9	58.6	58.0
C5	Bias Capacitor	70.4	66.8	63.1	63.5
D1	Primary Snubber	84.6	78.5	71.3	71.6
T1	Flyback Transformer	74.8	72.6	71.1	71.9
C11	Output Capacitor	71.1	68.9	67.7	68.1
C12	Output Capacitor	70.1	67.9	66.8	67.3
L3	Output Inductor	76.3	74.7	73.1	73.6
C16	Output Capacitor	67.6	65.4	63.3	63.7
C13	Output Capacitor	56.9	56.1	55.3	55.6
L4	Output Inductor	57.5	56.6	55.9	56.1
C14	Output Capacitor	54.6	54.1	53.3	53.5
U1	InnoSwitch3-CE INN3168C	90.9	81.1	72.8	74.5
Q1	SRFET	76.8	73.4	71.5	72.1
D4	Ultrafast Diode	83.4	81.3	80.2	80.5

12 Waveforms

12.1 Load Transient Response

Loading condition: 5 V / 3 A; 50 V / 0 A - 0.5 A at 50 ms and 0.5 A – 0 A at 50 ms; Slew Rate 200 mA / μs

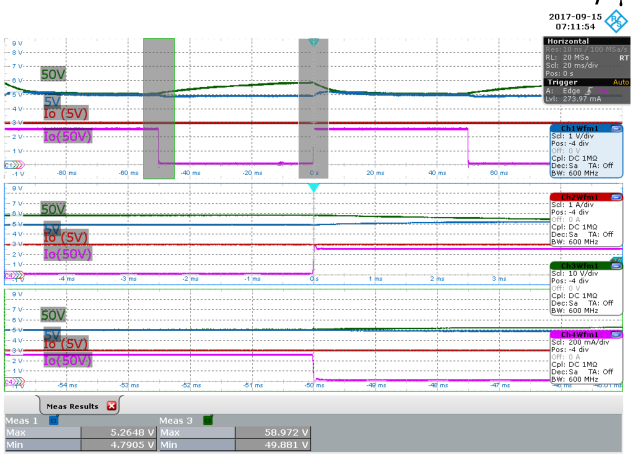

Figure 19 – 90 VAC.
Ch1: (5 V) V_{OUT}, 1 V / div., 20 ms / div.
Ch2: (5 V) I_{OUT}, 1 A / div., 20 ms / div.
Ch3: (50 V) V_{OUT}, 10 V / div., 20 ms / div.
Ch4: (50 V) I_{OUT}, 200 mA / div., 20 ms / div.
5 V_{MAX}: 5.2648 V.
5 V_{MIN}: 4.7905 V.
50 V_{MAX}: 58.972 V.
50 V_{MIN}: 49.881 V.

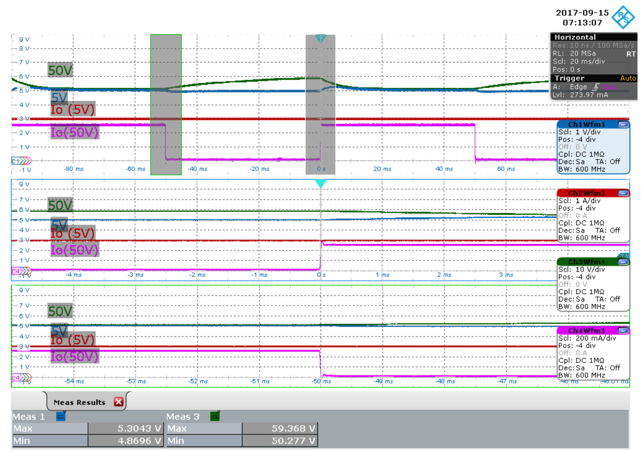

Figure 20 – 265 VAC.
Ch1: (5 V) V_{OUT}, 1 V / div., 20 ms / div.
Ch2: (5 V) I_{OUT}, 1 A / div., 20 ms / div.
Ch3: (50 V) V_{OUT}, 10 V / div., 20 ms / div.
Ch4: (50 V) I_{OUT}, 200 mA / div., 20 ms / div.
5 V_{MAX}: 5.3043 V.
5 V_{MIN}: 4.8696 V.
50 V_{MAX}: 59.368 V.
50 V_{MIN}: 50.277 V.

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Loading condition: 50 V / 0.5 A; 50 V / 0 A - 3.0 A at 50 ms and 3.0 A – 0 A at 50 ms; Slew Rate 200 mA / µS

Figure 21 – 90 VAC.
Ch1: (5 V) V_{OUT}, 1 V / div., 20 ms / div.
Ch2: (5 V) I_{OUT}, 1 A / div., 20 ms / div.
Ch3: (50 V) V_{OUT}, 10 V / div., 20 ms / div.
Ch4: (50 V) I_{OUT}, 200 mA / div., 20 ms / div.
5 V_{MAX}: 5.4625 V.
5 V_{MIN}: 4.4743 V.
50 V_{MAX}: 51.067 V.
50 V_{MIN}: 44.743 V.

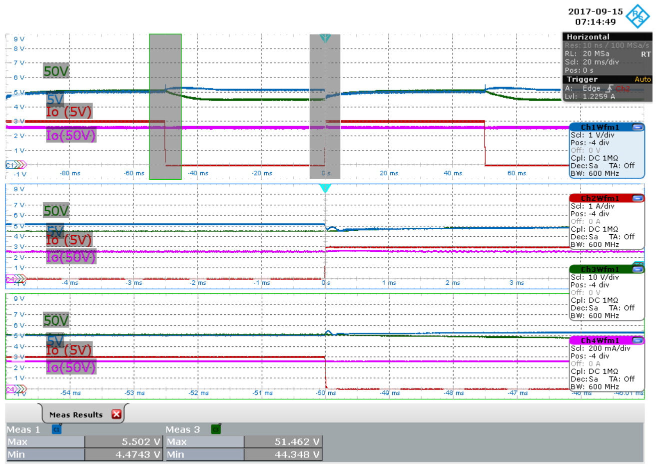

Figure 22 – 265 VAC.
Ch1: (5 V) V_{OUT}, 1 V / div., 20 ms / div.
Ch2: (5 V) I_{OUT}, 1 A / div., 20 ms / div.
Ch3: (50 V) V_{OUT}, 10 V / div., 20 ms / div.
Ch4: (50 V) I_{OUT}, 200 mA / div., 20 ms / div.
5 V_{MAX}: 5.502 V.
5 V_{MIN}: 4.4743 V.
50 V_{MAX}: 51.462 V.
50 V_{MIN}: 44.348 V.

12.2 Switching Waveforms

12.2.1 INN3138C (U1) Voltage and Current Waveforms

12.2.1.1 Normal Operation

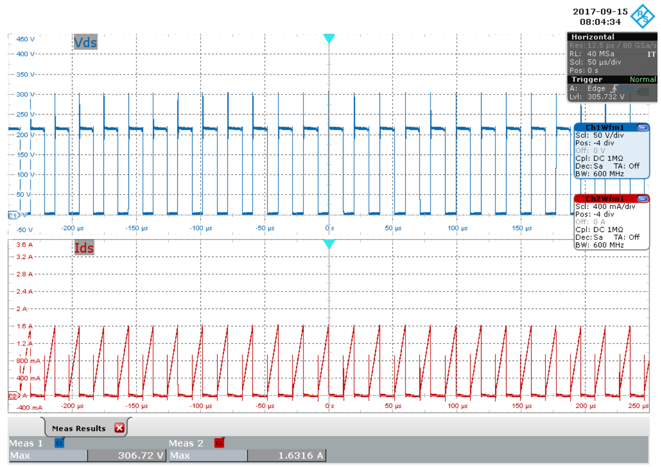

Figure 23 – 90 VAC, Full Load.
Upper: V_{DS}, 50 V / div., 50 µs / div.
Lower: I_{DS}, 400 mA / div., 50 µs / div.
$V_{DS(MAX)}$ = 306.72 V.
$I_{DS(MAX)}$ = 1.6316 A.

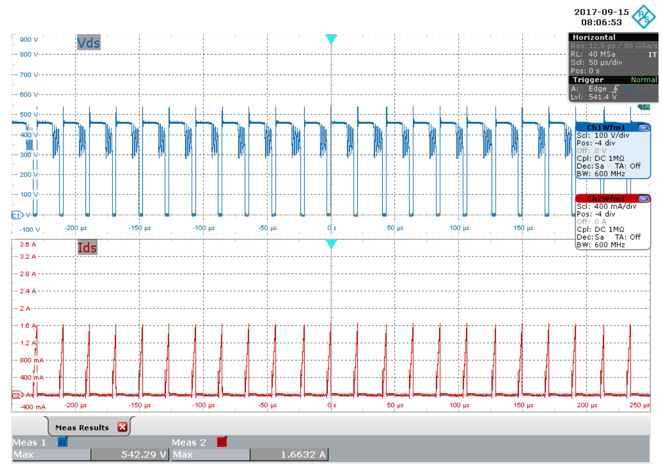

Figure 24 – 265 VAC, Full Load.
Upper: V_{DS}, 100 V / div., 50 µs / div.
Lower: I_{DS}, 400 mA / div., 50 µs / div.
$V_{DS(MAX)}$ = 542.29 V.
$I_{DS(MAX)}$ = 1.6632 A.

12.2.1.2 Start-Up Operation

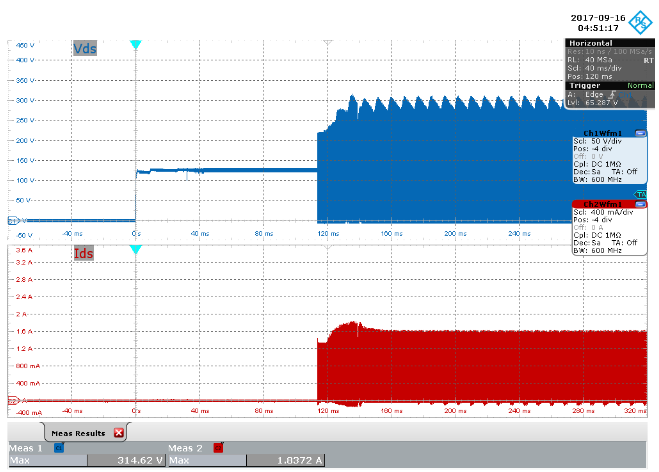

Figure 25 – 90 VAC, Full Load.
Upper: V_{DS}, 50 V / div., 40 ms / div.
Lower: I_{DS}, 400 mA / div., 40 ms / div.
$V_{DS(MAX)}$ = 314.62 V.
$I_{DS(MAX)}$ = 1.8372 A.

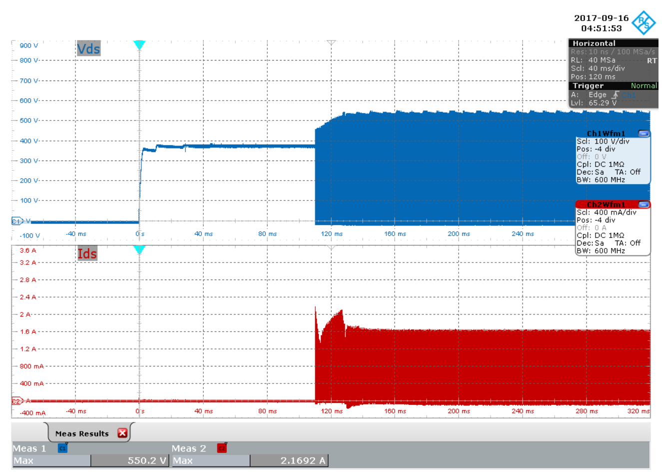

Figure 26 – 265 VAC, Full Load.
Upper: V_{DS}, 100 V / div., 40 ms / div.
Lower: I_{DS}, 400 mA / div., 40 ms / div.
$V_{DS(MAX)}$ = 550.2 V.
$I_{DS(MAX)}$ = 2.1692 A.

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12.2.2 SR FET (Q1) Voltage and Current Waveforms

12.2.2.1 Normal Operation

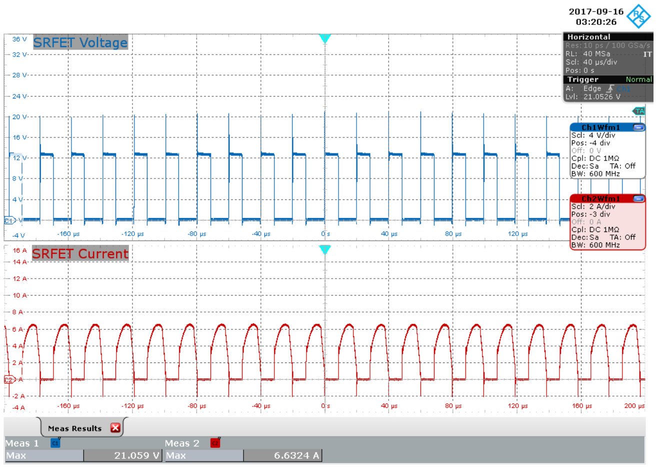

Figure 27 – 90 VAC, Full Load.
Upper: V_{DS}, 4 V / div., 40 µs / div.
Lower: I_{DS}, 2 A / div., 40 µs / div.
$V_{DS(MAX)}$ = 21.059 V.
$I_{DS(MAX)}$ = 6.6324 A.

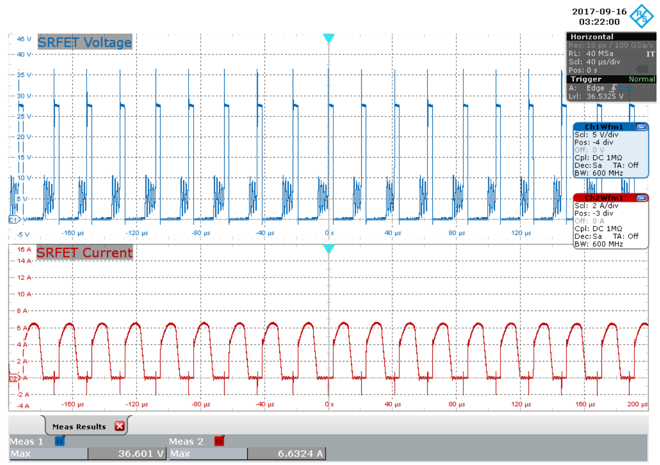

Figure 28 – 265 VAC, Full Load.
Upper: V_{DS}, 5 V / div., 40 µs / div.
Lower: I_{DS}, 2 A / div., 40 µs / div.
$V_{DS(MAX)}$ = 36.601 V.
$I_{DS(MAX)}$ = 6.6324 A.

12.2.2.2 Start-Up Operation

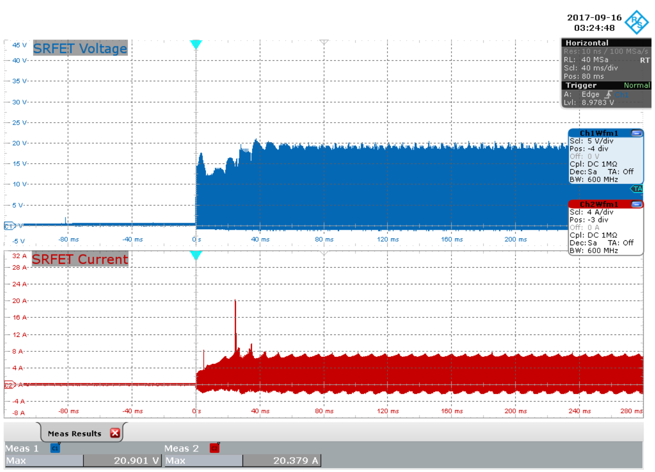

Figure 29 – 90 VAC, Full Load.
Upper: V_{DS}, 5 V / div., 40 ms / div.
Lower: I_{DS}, 4 A / div., 40 ms / div.
$V_{DS(MAX)}$ = 20.901 V.
$I_{DS(MAX)}$ = 20.379 A.

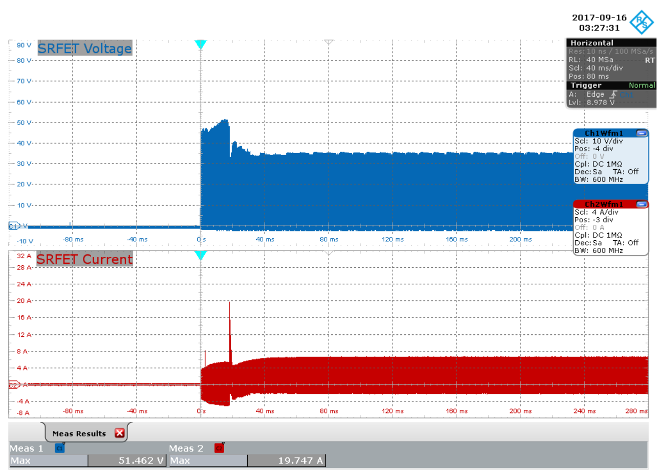

Figure 30 – 265 VAC, Full Load.
Upper: V_{DS}, 10 V / div., 40 ms / div.
Lower: I_{DS}, 4 A / div., 40 ms / div.
$V_{DS(MAX)}$ = 51.462 V.
$I_{DS(MAX)}$ = 19.747 A.

12.2.3 Ultrafast Diode (D4) Voltage and Current Waveforms

12.2.3.1 Normal Operation

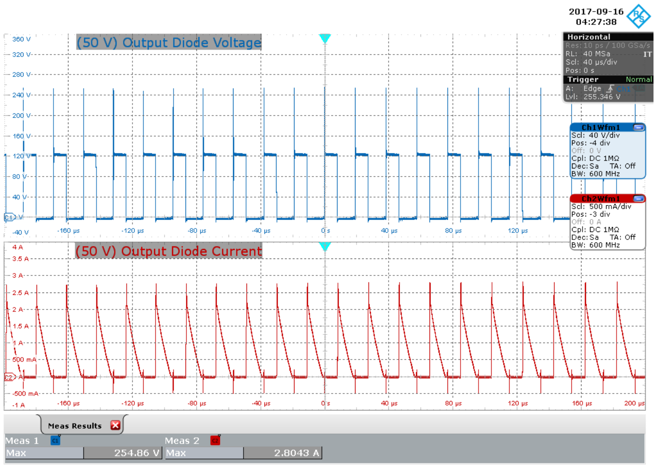

Figure 31 – 90 VAC, Full Load.
Upper: V_{D4}, 40 V / div., 40 µs / div.
Lower: I_{D4}, 500 mA / div., 40 µs / div.
$V_{D4(MAX)}$ = 254.86 V.
$I_{D4(MAX)}$ = 2.8043 A.

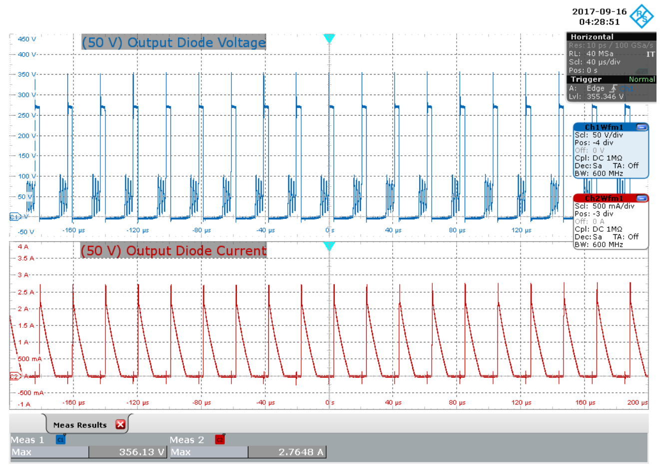

Figure 32 – 265 VAC, Full Load.
Upper: V_{D4}, 50 V / div., 40 µs / div.
Lower: I_{D4}, 500 mA / div., 40 µs / div.
$V_{D4(MAX)}$ = 356.13 V.
$I_{D4(MAX)}$ = 2.7648 A.

12.2.3.2 Start-Up Operation

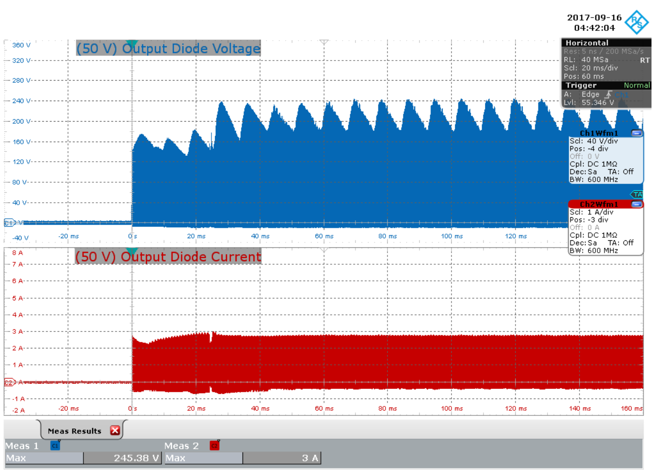

Figure 33 – 90 VAC, Full Load.
Upper: V_{D4}, 40 V / div., 20 ms / div.
Lower: I_{D4}, 1 A / div., 20 ms / div.
$V_{D4(MAX)}$ = 245.38 V.
$I_{D4(MAX)}$ = 3.0 A.

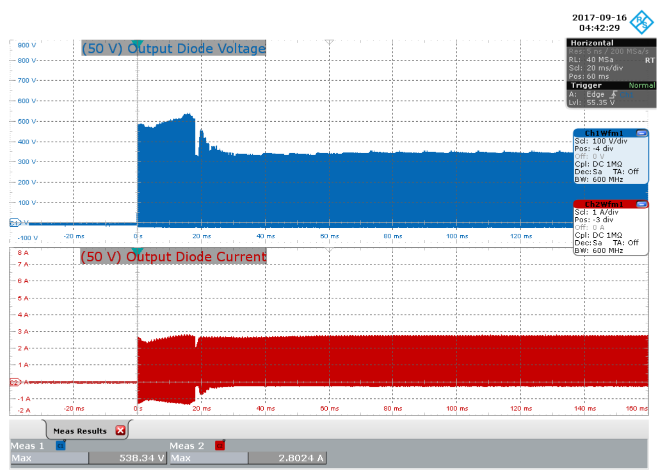

Figure 34 – 265 VAC, Full Load.
Upper: V_{D4}, 100 V / div., 20 ms / div.
Lower: I_{D4}, 1 A / div., 20 ms / div.
$V_{D4(MAX)}$ = 538.34 V.
$I_{D4(MAX)}$ = 2.8024 A.

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12.3 Brown-in and Brown-out

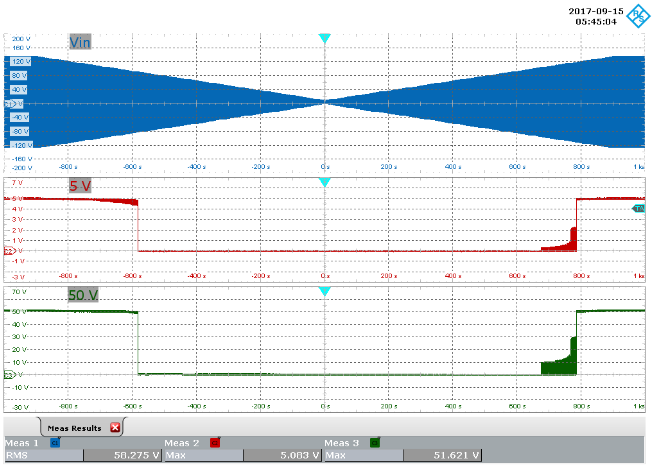

Figure 35 – 90 VAC, 6 V / min, Full Load.
CH1: V_{AC}, 40 V / div., 200 s / div.
CH2: $V_{OUT(5\ V)}$, 1 V / div., 200 s / div.
CH3: $V_{OUT(50\ V)}$, 10 V / div., 200 s / div.

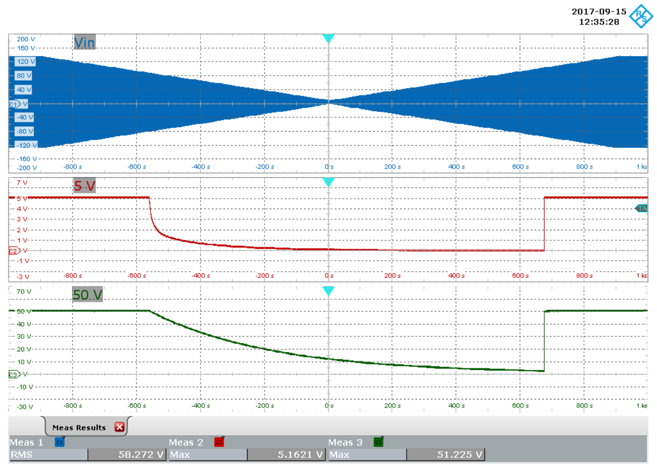

Figure 36 – 90 VAC, 6 V / min, No-Load.
CH1: V_{AC}, 40 V / div., 200 s / div.
CH2: $V_{OUT(5\ V)}$, 1 V / div., 200 s / div.
CH3: $V_{OUT(50\ V)}$, 10 V / div., 200 s / div.

12.4 Line UV / OV

12.4.1 Line UV+ and UV-

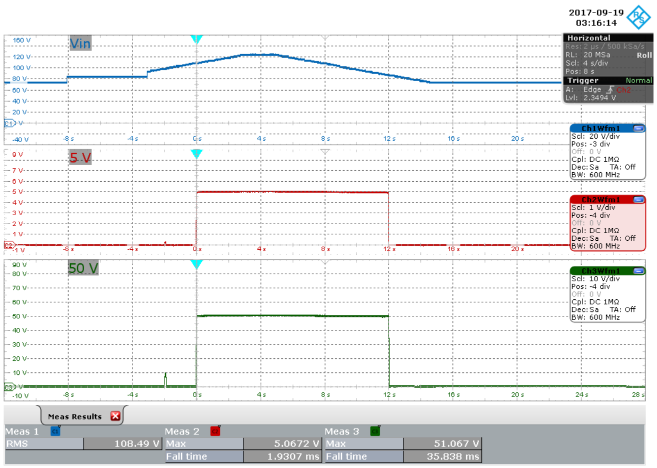

Figure 37 – 70 VDC Input, Full Load.
CH1: V_{IN}, 20 V / div., 4 s / div.
CH2: $V_{OUT(5\ V)}$, 1 V / div., 4 s / div.
CH3: $V_{OUT(50\ V)}$, 10 V / div., 4 s / div.
Line UV+: 108.49 V.

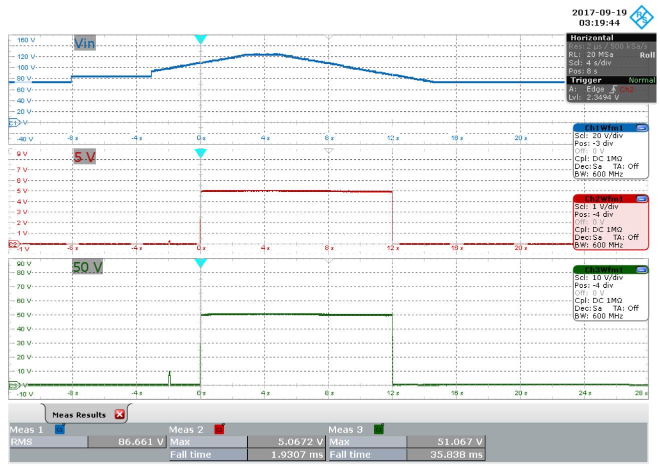

Figure 38 – 70 VDC Input, Full Load.
CH1: V_{AC}, 20 V / div., 4 s / div.
CH2: $V_{OUT(5\ V)}$, 1 V / div., 4 s / div.
CH3: $V_{OUT(50\ V)}$, 10 V / div., 4 s / div.
Line UV-: 86.661 V.

12.4.1.1 Line OV+ and OV-

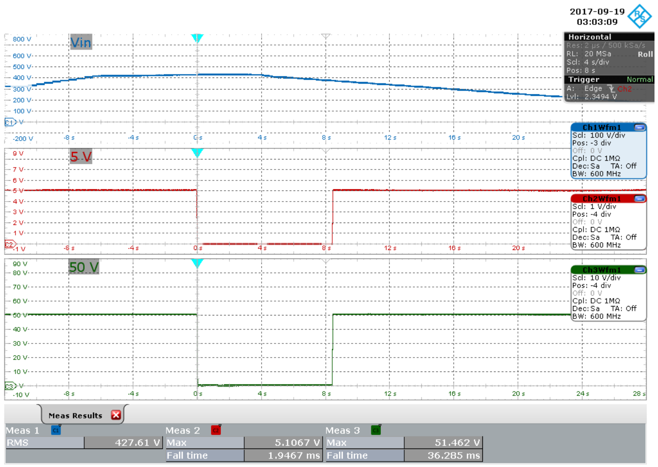

Figure 39 – 320 VDC Input, Full Load.
CH1: V_{IN}, 100 V / div., 4 s / div.
CH2: $V_{OUT(5\ V)}$, 1 V / div., 4 s / div.
CH3: $V_{OUT(50\ V)}$, 10 V / div., 4 s / div.
Line UV+: 427.61 V.

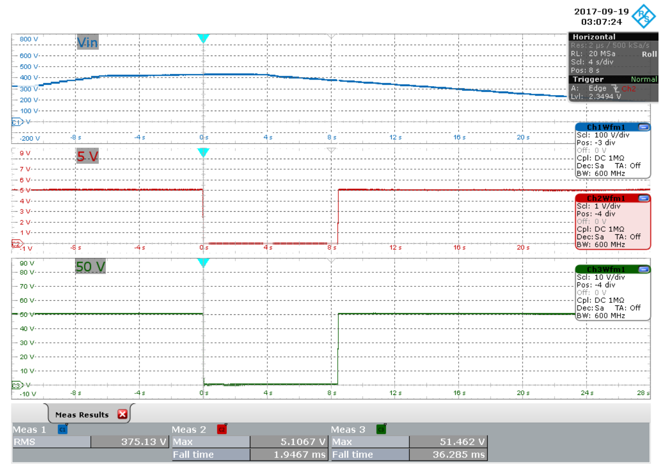

Figure 40 – 320 VDC Input, Full Load.
CH1: V_{AC}, 100 V / div., 4 s / div.
CH2: $V_{OUT(5\ V)}$, 1 V / div., 4 s / div.
CH3: $V_{OUT(50\ V)}$, 10 V / div., 4 s / div.
Line UV-: 375.13 V.

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12.5 Output Measurements

12.5.1.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4901-2 Probe Master in 10X setting is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/100 V ceramic type and one (1) 10 μF/16 V aluminum electrolytic for 5 V output and one (1) 0.1 μF/100 V ceramic type and one (1) 10 μF/63 V aluminum electrolytic for 50 V output . The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

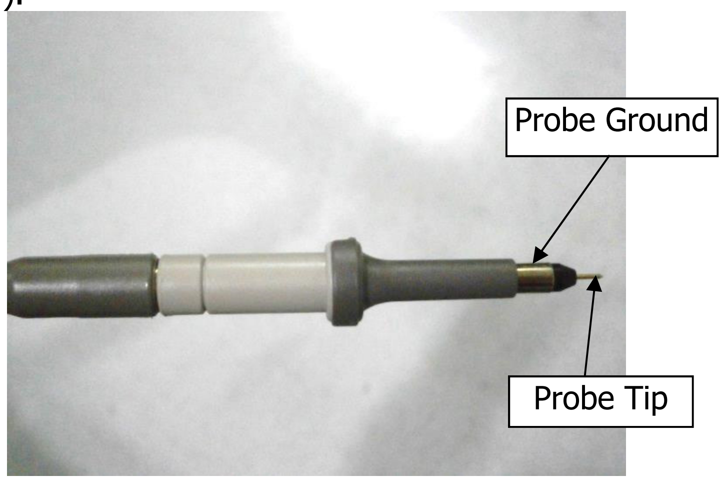

Figure 41 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

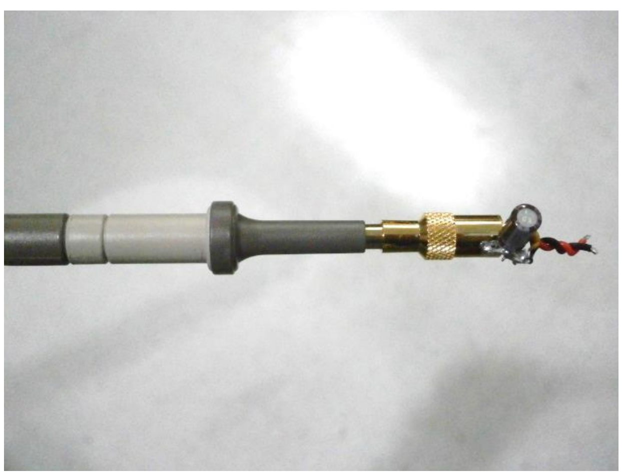

Figure 42 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4901-2 BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

12.5.1.2 Ripple Voltage Waveforms

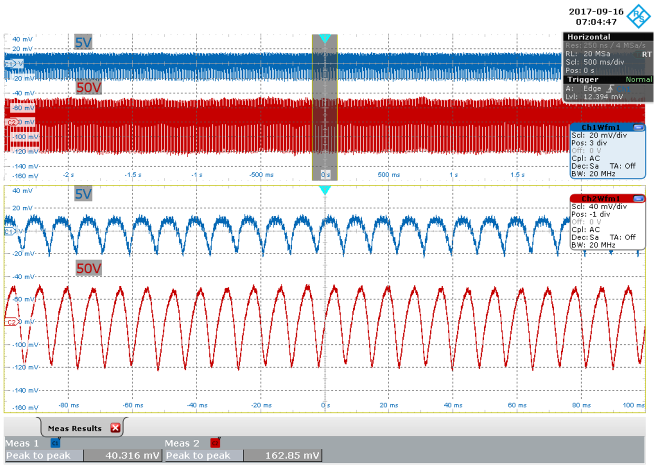

Figure 43 – 90 VDC Input, Full Load.
CH1: $V_{OUT(5\ V)}$, 20 mV / div., 500 ms / div.
CH2: $V_{OUT(50\ V)}$, 40 mV / div., 500 ms / div.
$V_{OUT(5\ V)PK-PK}$: 40.316 mV.
$V_{OUT(50\ V)PK-PK}$: 162.85 mV.

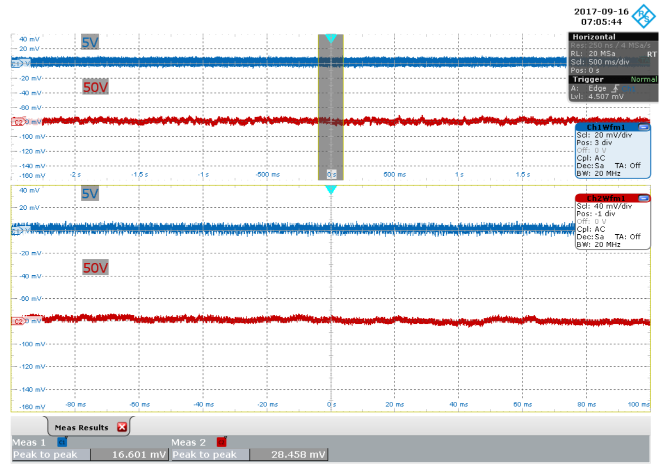

Figure 44 – 265 VDC Input, Full Load.
CH1: $V_{OUT(5\ V)}$, 20 mV / div., 500 ms / div.
CH2: $V_{OUT(50\ V)}$, 40 mV / div., 500 ms / div.
$V_{OUT(5\ V)PK-PK}$: 16.601 mV.
$V_{OUT(50\ V)PK-PK}$: 28.458 mV.

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13 Conducted EMI

10.1 Test Set-up

Unit is powered-up at full load and grounded

Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power hitester.
4. Chroma measurement test fixture.
5. Input Voltage set at 230 VAC and 115 VAC.

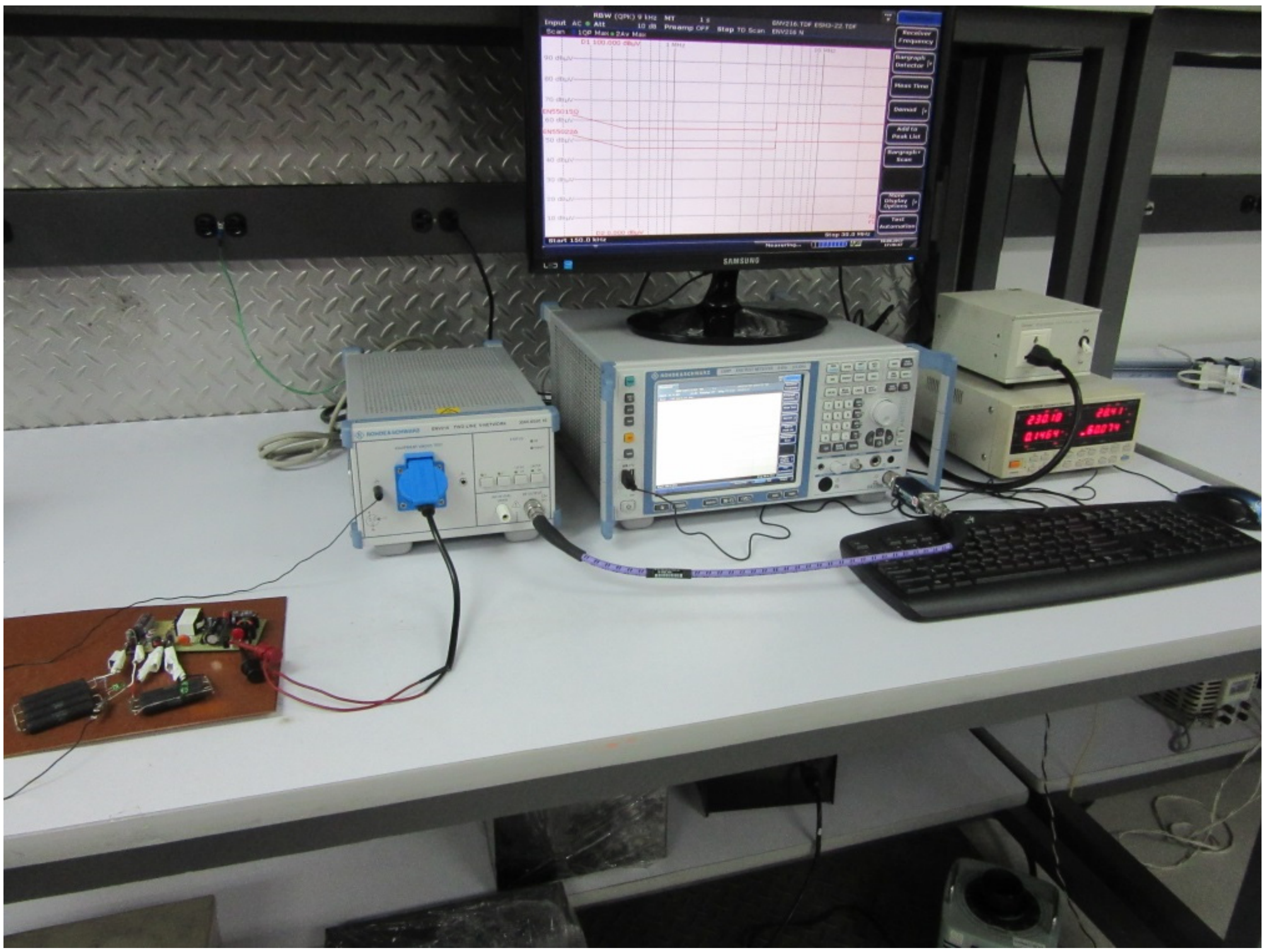
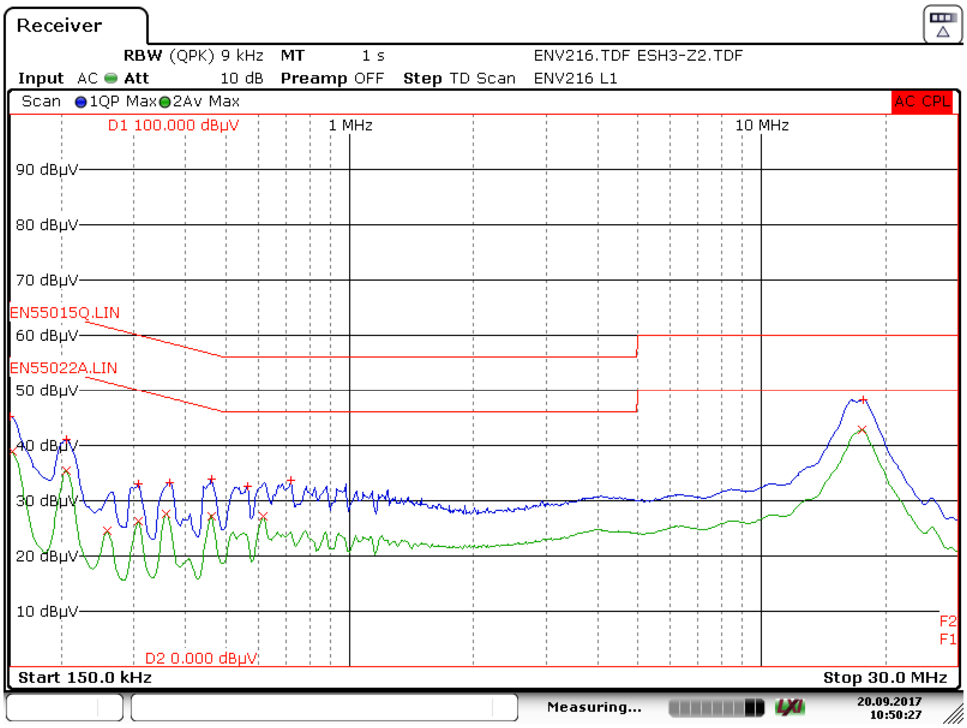


Figure 45 – Conducted EMI Test Set-up.

13.1 EMI Test Result

13.1.1 115 VAC Line



Date: 20.SEP.2017 10:50:27

Trace1: EN55015Q.LIN Trace2: EN55022A.LIN

Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	17.5335 MHz	42.82 L1	-7.18 dB
1 Quasi Peak	17.6438 MHz	48.28 L1	-11.72 dB
2 Average	152.2500 kHz	38.88 L1	-17.00 dB
2 Average	206.2500 kHz	35.47 L1	-17.88 dB
2 Average	618.0000 kHz	27.13 L1	-18.87 dB
2 Average	462.7500 kHz	27.28 L1	-19.36 dB
1 Quasi Peak	150.0000 kHz	45.25 L1	-20.75 dB
2 Average	359.2500 kHz	27.69 L1	-21.06 dB
1 Quasi Peak	206.2500 kHz	41.13 L1	-22.22 dB
1 Quasi Peak	721.5000 kHz	33.70 L1	-22.30 dB
1 Quasi Peak	462.7500 kHz	33.87 L1	-22.77 dB
1 Quasi Peak	566.2500 kHz	32.70 L1	-23.30 dB
2 Average	307.5000 kHz	26.26 L1	-23.78 dB
1 Quasi Peak	366.0000 kHz	33.29 L1	-25.30 dB

Figure 46 – PE Connected to Negative Output.

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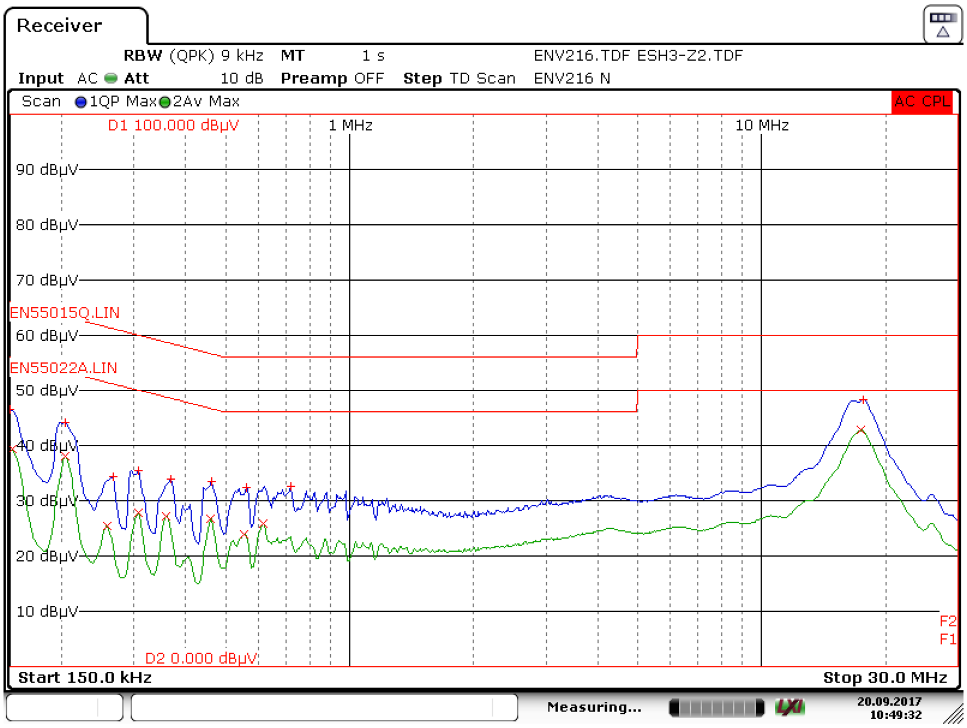
13.1.2 115 VAC Neutral



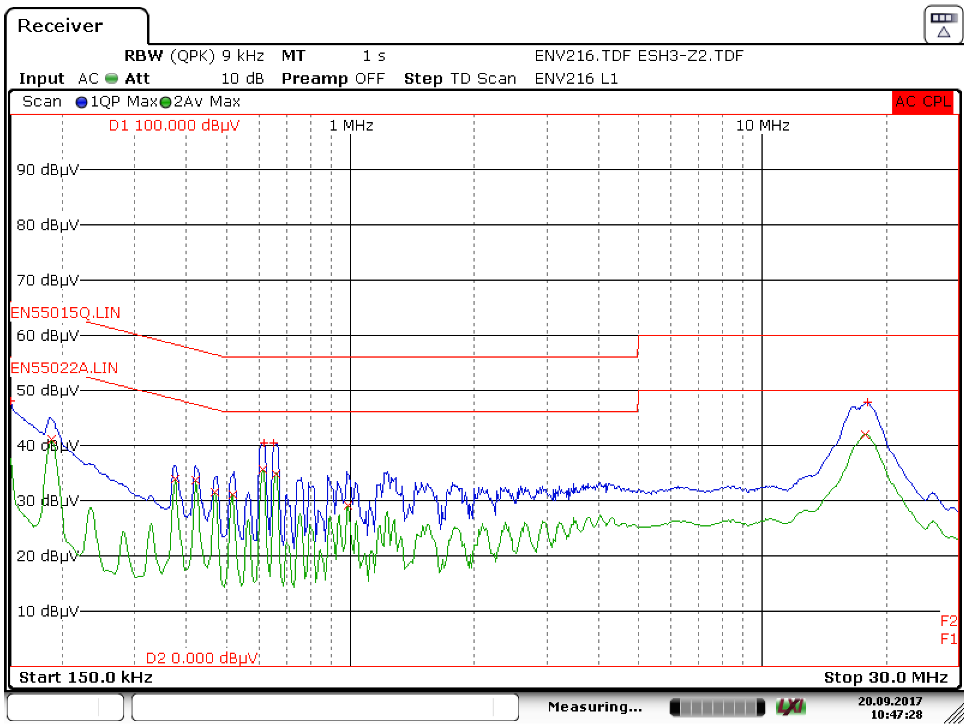
Date: 20.SEP.2017 10:49:32

Trace1: EN55015Q.LIN Trace2: EN55022A.LIN

Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	17.4683 MHz	42.73 N	-7.27 dB
1 Quasi Peak	17.6258 MHz	48.22 N	-11.78 dB
2 Average	204.0000 kHz	37.96 N	-15.49 dB
2 Average	152.2500 kHz	39.38 N	-16.50 dB
1 Quasi Peak	204.0000 kHz	44.10 N	-19.35 dB
1 Quasi Peak	150.0000 kHz	46.47 N	-19.53 dB
2 Average	460.5000 kHz	26.79 N	-19.89 dB
2 Average	618.0000 kHz	25.94 N	-20.06 dB
2 Average	359.2500 kHz	27.27 N	-21.48 dB
2 Average	555.0000 kHz	23.86 N	-22.14 dB
2 Average	307.5000 kHz	27.84 N	-22.20 dB
1 Quasi Peak	462.7500 kHz	33.42 N	-23.22 dB
1 Quasi Peak	719.2500 kHz	32.56 N	-23.44 dB
1 Quasi Peak	564.0000 kHz	32.44 N	-23.56 dB

Figure 47 – PE Connected to Negative Output.

13.1.3 230 VAC Line



Date: 20.SEP.2017 10:47:28

Trace1: EN55015Q.LIN Trace2: EN55022A.LIN

Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	17.7743 MHz	42.03 L1	-7.97 dB
2 Average	613.5000 kHz	35.74 L1	-10.26 dB
2 Average	660.7500 kHz	34.89 L1	-11.11 dB
1 Quasi Peak	17.9993 MHz	47.78 L1	-12.22 dB
2 Average	188.2500 kHz	40.98 L1	-13.13 dB
2 Average	422.2500 kHz	33.73 L1	-13.67 dB
2 Average	375.0000 kHz	33.82 L1	-14.57 dB
2 Average	519.0000 kHz	31.06 L1	-14.94 dB
2 Average	469.5000 kHz	31.54 L1	-14.98 dB
1 Quasi Peak	651.7500 kHz	40.50 L1	-15.50 dB
1 Quasi Peak	615.7500 kHz	40.47 L1	-15.53 dB
2 Average	987.0000 kHz	29.19 L1	-16.81 dB
1 Quasi Peak	150.0000 kHz	48.09 L1	-17.91 dB

Figure 48 – PE Connected to Negative Output.

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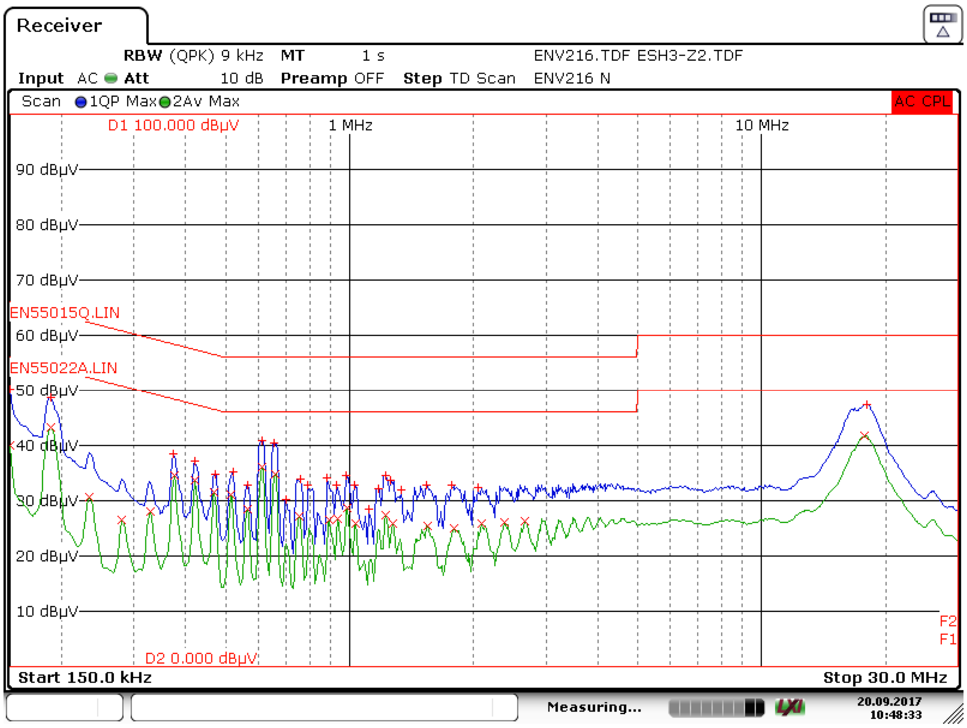
13.1.4 230 VAC Neutral



Date: 20.SEP.2017 10:48:33

Trace1: EN55015Q.LIN Trace2: EN55022A.LIN

Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	17.8148 MHz	41.79 N	-8.21 dB
2 Average	613.5000 kHz	36.05 N	-9.95 dB
2 Average	188.2500 kHz	43.34 N	-10.77 dB
2 Average	660.7500 kHz	34.86 N	-11.14 dB
1 Quasi Peak	17.9655 MHz	47.44 N	-12.56 dB
2 Average	422.2500 kHz	33.77 N	-13.63 dB
2 Average	375.0000 kHz	34.54 N	-13.85 dB
2 Average	516.7500 kHz	31.01 N	-14.99 dB
2 Average	469.5000 kHz	31.51 N	-15.01 dB
1 Quasi Peak	613.5000 kHz	40.78 N	-15.22 dB
1 Quasi Peak	188.2500 kHz	48.72 N	-15.39 dB
1 Quasi Peak	654.0000 kHz	40.54 N	-15.46 dB
1 Quasi Peak	150.0000 kHz	50.14 N	-15.86 dB
2 Average	150.0000 kHz	39.96 N	-16.04 dB

Figure 49 – PE Connected to Negative Output.

14 Line Surge

The unit was subjected to ±6000 V, 100 kHz ring wave, ±1000 V differential surge, and ±2000 V common mode surge with 10 strikes at each condition. A test failure is defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

14.1 Differential Surge Test Results

Surge Voltage (kV)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+1	0	L1 / L2	2	10	PASS
-1	0	L1 / L2	2	10	PASS
+1	90	L1 / L2	2	10	PASS
-1	90	L1 / L2	2	10	PASS
+1	180	L1 / L2	2	10	PASS
-1	180	L1 / L2	2	10	PASS
+1	270	L1 / L2	2	10	PASS
-1	270	L1 / L2	2	10	PASS

14.2 Common Mode Surge Test Results

Surge Voltage (kV)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+2	0	L1 / PE, L2 / PE	12	10	PASS
-2	0	L1 / PE, L2 / PE	12	10	PASS
+2	90	L1 / PE, L2 / PE	12	10	PASS
-2	90	L1 / PE, L2 / PE	12	10	PASS
+2	180	L1 / PE, L2 / PE	12	10	PASS
-2	180	L1 / PE, L2 / PE	12	10	PASS
+2	270	L1 / PE, L2 / PE	12	10	PASS
-2	270	L1 / PE, L2 / PE	12	10	PASS

14.3 Ring Wave Test Results

Surge Voltage (kV)	Phase Angle (º)	IEC Coupling	Waveform (A)	Number Strikes	Result
+6	0	L1, L2 / PE	500	10	PASS
-6	0	L1, L2 / PE	500	10	PASS
+6	90	L1, L2 / PE	500	10	PASS
-6	90	L1, L2 / PE	500	10	PASS
+6	180	L1, L2 / PE	500	10	PASS
-6	180	L1, L2 / PE	500	10	PASS
+6	270	L1, L2 / PE	500	10	PASS
-6	270	L1, L2 / PE	500	10	PASS

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15 ESD Test Results

Level (V)	Input Voltage (VAC)	Discharge	Number of Discharges	Test Result (Pass/Fail)
8000	230	Contact	10	No damage, No Auto-Restart
-8000	230	Contact	10	No damage, No Auto-Restart
Level (V)	**Input Voltage (VAC)**	**Discharge**	**Number of Discharges**	**Test Result (Pass/Fail)**
16500	230	Air	10	No Damage
-16500	230	Air	10	No Damage

16 Revision History

Date	Author	Revision	Description and Changes	Reviewed
03-Oct-17	JMR	1.0	Initial release	Apps & Mktg

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