Design Example Report

Title	***60 W USB PD 3.0 Power Supply with 3.3 V – 21 V PPS Output Using InnoSwitch™3-Pro PowiGaN™ INN3379C-H302, MinE-CAP MIN1072M, and VIA Labs VP302 Controller***
Specification	90 VAC – 265 VAC Input; 5 V / 3 A, 9 V / 3 A, 15 V / 3 A, 20 V / 3 A, 3.3 V – 21 V / 3 A PPS Output
Application	USB PD / PPS Power Adapter
Author	Applications Engineering Department
Document Number	DER-822
Date	October 7, 2020
Revision	1.0

Summary and Features

- InnoSwitch3-Pro - digitally controllable CV/CC QR flyback switcher IC with integrated high-voltage MOSFET, synchronous rectification and FluxLink™ feedback
  - I²C Interface enables low pin count USB PD Controller VP302 (8 pin)
  - Sophisticated telemetry and comprehensive protection features
- Very high power density design enabled by MinE-CAP MIN1072M
  - Power Density: 32.8 W / inch³ without enclosure (52 mm (L) x 26.2 mm (W) x 22 mm (H) form factor)
- Meets DOE6 and CoC v5 2016 Average Efficiency requirements with high margin (>2.5%)
  - 5 V Output: 91.47% at 115 VAC (9.67% margin); 90.29% at 230 VAC (8.49% margin)
  - 9 V Output: 92.11% at 115 VAC (4.81% margin); 92.04% at 230 VAC (4.74% margin)
  - 15 V Output: 92.17% at 115 VAC (3.27% margin); 92.85% at 230 VAC (3.95% margin)
  - 20 V Output: 91.89% at 115 VAC (2.89% margin); 93.04% at 230 VAC (4.04% margin)
- <60 mW no-load input power at 230 VAC
- Meets CISPR22 / EN55022 Class B Conducted EMI
- Low component count

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PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

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Important Note:

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Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 60 W USB PD 3.0 power supply using InnoSwitch3-Pro INN3379-H302 IC and VIA Labs VP302 USB PD controller. The USB PD source capabilities of the power supply are listed below.

- PDO1: 5 V / 3 A (Fixed Supply)
- PDO2: 9 V / 3 A (Fixed Supply)
- PDO3: 15 V / 3 A (Fixed Supply)
- PDO4: 20 V / 3 A (Fixed Supply)
- PDO5: 3.3 V – 21 V / 3 A (Programmable Power Supply)

This report demonstrates the high power density, exceptional performance, and high efficiency designs possible when the InnoSwitch3-Pro family of controllers is paired with the input capacitor volume-reduction capabilities of the MinE-CAP IC.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, magnetics specifications, and performance data.

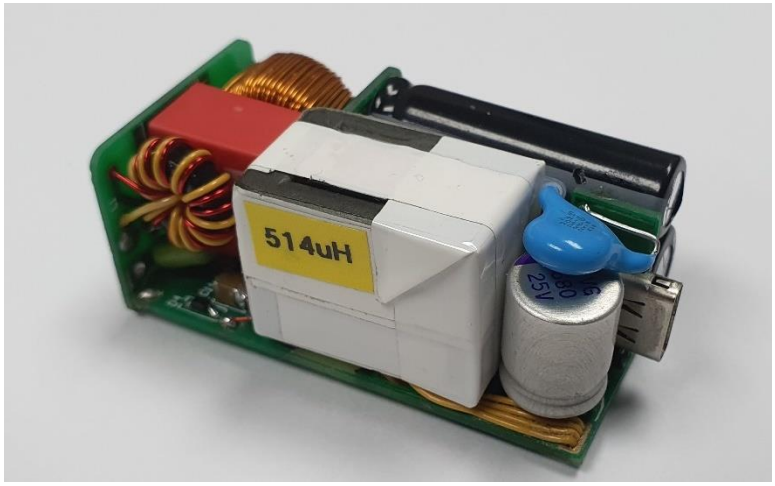

Figure 1 – Complete PCB Assembly.

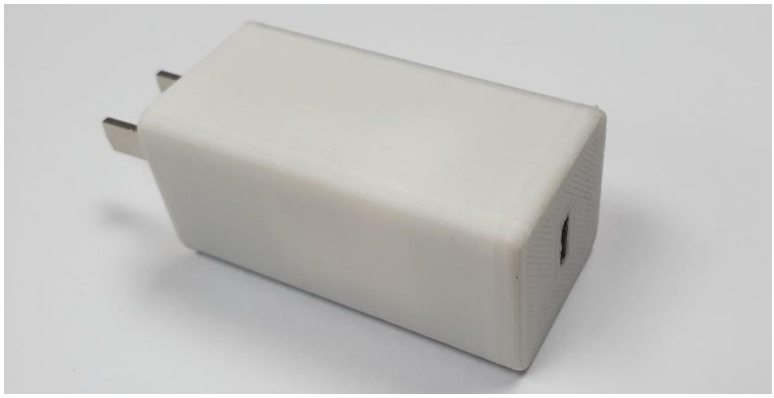

Figure 2 - DER-822 Unit with Enclosure.

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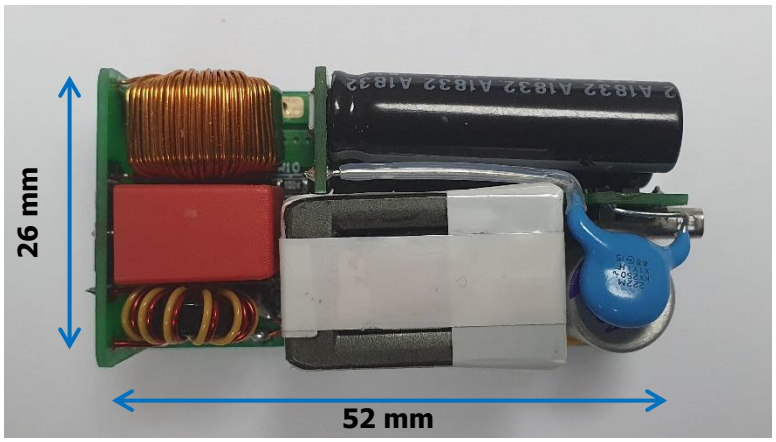

Figure 3 – Complete PCB Assembly Top View.

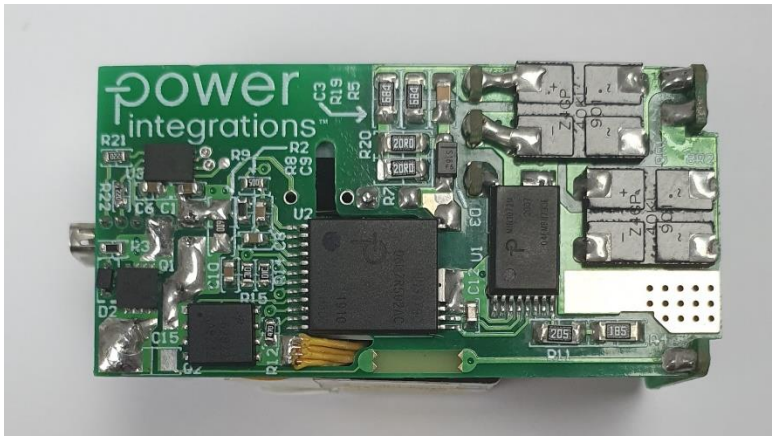

Figure 4 – Complete PCB Assembly Bottom View.

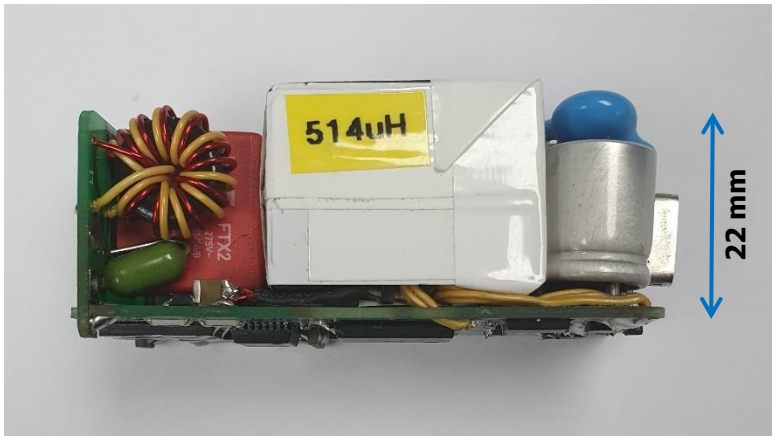

Figure 5 – Complete PCB Assembly Side View.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power			46	50	mW	Measured at 230 VAC
5 V / 3 A Setting						
Output Voltage	$V_{OUT(5\ V)}$		5.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(5\ V)}$			200	mV	Measured at End of 100 mΩ Cable.
Output Current	$I_{OUT(5\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(5\ V)}$		91.25		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(5\ V)}$			15	W	
9 V / 3 A Setting						
Output Voltage	$V_{OUT(9\ V)}$		9.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(9\ V)}$			200	mV	Measured at End of 100 mΩ Cable.
Output Current	$I_{OUT(9\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(9\ V)}$		92.00		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(9\ V)}$			27	W	
15 V / 3 A Setting						
Output Voltage	$V_{OUT(15\ V)}$		15.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(15\ V)}$			200	mV	Measured at End of 100 mΩ Cable.
Output Current	$I_{OUT(15\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(15\ V)}$		92.00		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(15\ V)}$			45	W	
20 V / 3 A Setting						
Output Voltage	$V_{OUT(20\ V)}$		20.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(20\ V)}$			250	mV	Measured at End of 100 mΩ Cable.
Output Current	$I_{OUT(20\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(20\ V)}$		91.75		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(20\ V)}$			60	W	
3.3 – 21 V PPS Setting						
Maximum Programmable Output Voltage	$V_{OUT,MAX}$			21	V	APDO Maximum Voltage.
Minimum Programmable Output Voltage	$V_{OUT,MIN}$	3.3			V	APDO Minimum Voltage.
Output Current	$I_{OUT,PPS}$			3.0	A	±3%
PPS Voltage Step	$V_{STEP,PPS}$		20		mV	PPS Voltage Step (USB PD 3.0).
PPS Current Step	$I_{STEP,PPS}$		50		mA	PPS Current Step (USB PD 3.0).
Continuous Output Power	P_{OUT}			60	W	PPS Power Limited bit = 1 (USB PD 3.0).
Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		40	ºC	Open Frame, Sea Level.

Note: To use this design for a charger/adapter with a different shape and form factor, the changes in the circuit board layout must be carefully evaluated to meet the target specifications for EMI, ESD, and Line Surge performance.

3 Schematic

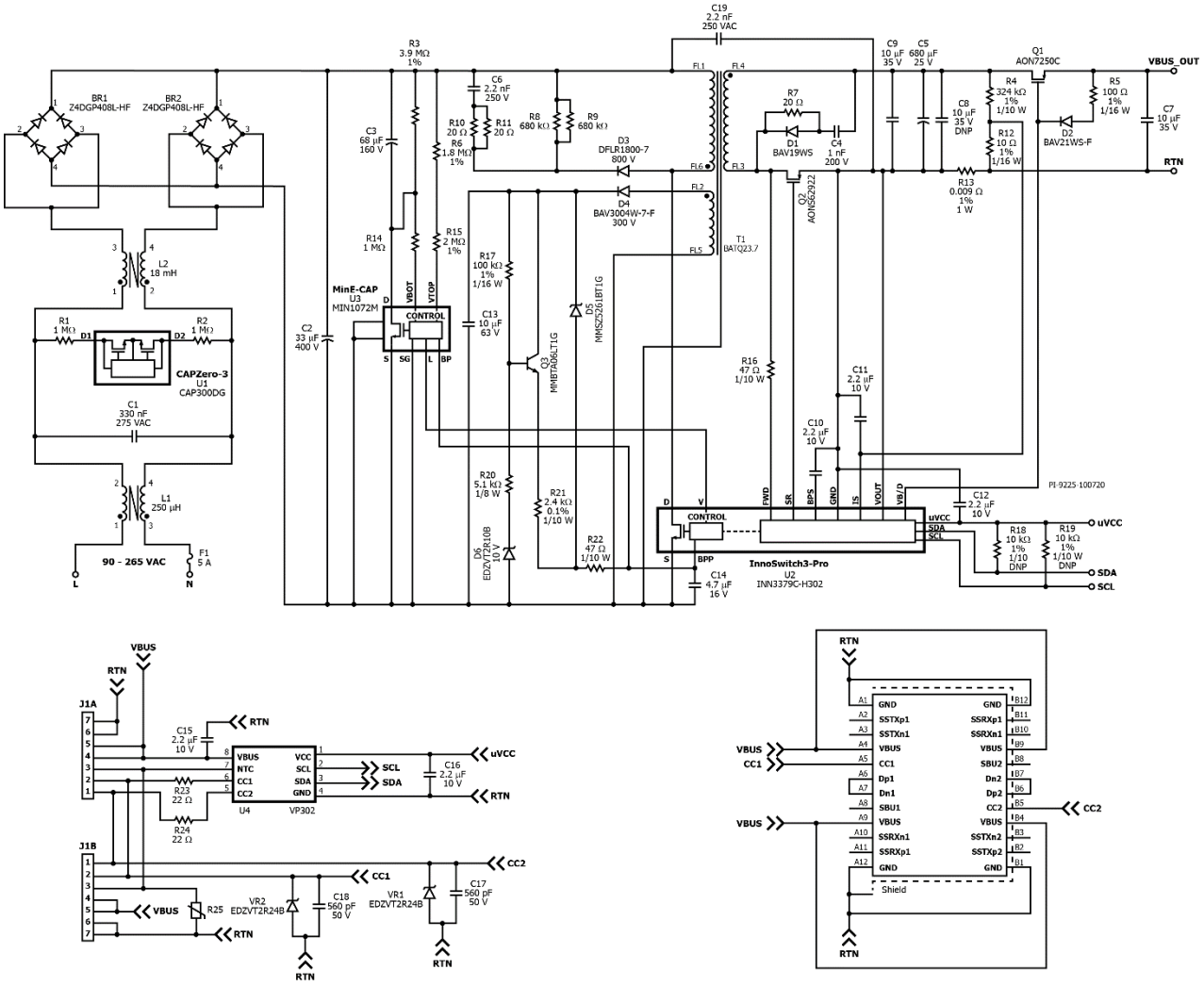

Figure 6 – Power Section Schematic

Note: Component references R18, R19, and C8 should not be populated.

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4 Circuit Description

4.1 *Input Rectifier and EMI Filter*

The input fuse F1 isolates the circuit and provides protection from component failure. Common mode chokes L1 and L2, with capacitors C1 and C19 provide common mode and differential mode noise filtering for EMI attenuation. Bridge rectifiers, BR1 and BR2, rectifies the AC input and then filtered by bulk capacitors C2 and C3. Two bridge rectifiers are used to improve heat dissipation by doubling the rectifier surface area since power loss from two rectifiers is the same as that of a single device.

Resistors R1 and R2 along with the CapZero™-3 IC, U1, discharges capacitor C1 when the power supply is disconnected from the AC mains for user safety purposes.

4.2 *InnoSwitch3-Pro IC Primary and MinE-CAP*

One end of the flyback transformer, T1, primary winding is connected to the rectified DC bus and the other end is connected to the drain terminal of the InnoSwitch3-Pro IC, U3.

The V pin of the InnoSwitch3-Pro IC is connected directly to the L pin of the MinE-CAP IC. Resistors R6 and R15 provide input voltage sensing for both the MinE-CAP IC and InnoSwitch3-Pro ICs. The MinE-CAP uses resistors R6 and R15 to monitor the line voltage as well as the voltage across the high-voltage bulk capacitor, C2. Resistor R3 is a bleeder resistor used to help regulate the voltage across C3, while resistor R14 is used by the MinE-CAP to sample the voltage at the negative terminal of C3. The MinE-CAP IC combines the information from the V_{TOP} and V_{BOT} pins to determine and control the voltage across the low-voltage bulk capacitor, C3.

The InnoSwitch3-Pro IC uses the current from the L pin to determine line undervoltage and overvoltage conditions. During regular operation, the current from the L pin follows the value of the current flowing through R6 and R15. Thus, the InnoSwitch3-Pro IC operates as if said resistors are directly connected to the V pin.

For this specific design, bypass capacitor C14 is shared by both the BPP pin of the InnoSwitch3-Pro IC and the BP pin of the MinE-CAP IC. The value of C14 is chosen based on the desired current limit of the InnoSwitch3-Pro.

A low-cost RCD snubber formed by diode D3, resistors R8, R9, R10, and R11, and capacitor C6 limits the voltage across the InnoSwitch3-Pro Drain-Source nodes during turn-off by dissipating the energy stored in the leakage inductance of the transformer, T1.

The InnoSwitch3-Pro IC has an internal current source that charges capacitor C14 when AC input is first applied. Once the InnoSwitch3-Pro IC starts switching and during normal operation, bias current is drawn from the auxiliary winding of the transformer. The

output of the auxiliary winding is rectified using diode D4 and filtered by capacitor C13. Since the output voltage of this design varies from 3.3 V to 21 V, the output of the auxiliary winding also varies depending on the secondary to auxiliary turns-ratio as well as the coupling coefficient between the primary and auxiliary. A linear regulator comprising resistors R17 and R20, Zener diode D6, and transistor Q3 provides a relatively stable DC voltage based on the breakdown voltage of D6 at the emitter terminal of Q3. Bias current is controlled using resistor R21.

Zener diode D5 offers primary sensed overvoltage protection. In case of overvoltage at the output of the converter, the auxiliary winding voltage also increases until D5 breaks down, causing excess current to flow into the BPP pin of the InnoSwitch3-Pro IC. If the current flowing into the BPP pin exceeds the I_{SD} threshold, the InnoSwitch3-Pro controller latches off to prevent any further increase in output voltage. Resistor R22 limits the current injected to the BPP pin during an overvoltage event.

4.3 *InnoSwitch3-Pro IC Secondary and USB Power Delivery Controller*

The secondary-side of the InnoSwitch3-Pro IC has pins for output voltage and current sensing as well as a MOSFET driver to control an N-MOSFET for synchronous rectification.

The voltage across the transformer secondary winding is rectified by the secondary-side synchronous rectifier N-MOSFET (SR FET) Q5 and filtered by capacitors C5, C8 and C9. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via an RCD snubber composed of R7, D2 and C4. The RCD snubber also protects the SR FET from exceeding its rated voltage by clamping the voltage across the Drain-Source nodes of the SR FET.

The gate of Q5 is controlled by the secondary-side controller and gate driver within U3, based on the secondary winding voltage sensed by the FWD pin through resistor R16.

In continuous conduction mode of operation, the SR FET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power switch prevents the possibility of cross conduction, which occurs when both switches are ON at the same time. This feature allows for a highly reliable synchronous rectifier operation.

The secondary-side of the IC is powered from either the secondary winding forward voltage or the output capacitors. Capacitor C10 connected to the BPS pin of the U3 provides decoupling for the secondary-side internal circuitry of U3.

Output current is sensed by monitoring the voltage across resistor R13. Resistors R4 and R12 are used to add a DC offset to the sensed output current to provide a positive slope

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to the CC characteristic curve. This feature can be disabled by shorting R12 and leaving R4 OPEN. The current sense signal is filtered by capacitor C11 and monitored across the IS and SECONDARY GROUND pins. The internal current sense threshold of the InnoSwitch3-Pro is I^2C programmable and can be adjusted up to approximately 32 mV. The InnoSwitch3-Pro IC regulates the average output current to the programmed value by controlling the number of primary switch pulses when the current sense threshold is exceeded.

During constant current (CC) operation, when the output voltage falls, the secondary side controller inside U3 will power itself from the secondary winding directly. During the On-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C10 via resistor R16 and an internal regulator. This allows output current regulation until the minimum output UV threshold is reached, after which the unit enters auto-restart until the output load is reduced.

When the output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch3-Pro IC. Similar to current regulation, the output voltage is also compared to an I^2C programmable internal voltage reference. The InnoSwitch3-Pro IC regulates the output voltage by controlling the number and frequency of the primary switch pulses.

N-MOSFET Q1 functions as the bus switch used connect or disconnect the output of the flyback converter from the USB Type-C receptacle. Q1 is controlled by the VB/D pin on the InnoSwitch3-Pro IC. Resistor R5 and diode D1 are connected across the Source and Gate nodes of Q1 to provide for a discharge path for the bus voltage when the Q1 is turned off. Capacitor C7 is used to provide ESD protection and output voltage ripple reduction.

This design uses the VIA Labs VP302 (U4) as its USB Power Delivery (USB PD) controller. It is powered directly by the InnoSwitch3-Pro IC through the µVCC pin. USB PD protocol is communicated over either the CC1 or CC2 lines depending on the orientation in which Type-C plug is connected.

The VP302 uses I^2C to communicate with InnoSwitch3-Pro to control the InnoSwith3-Pro's CV, CC, V_{KP}, OVA and UVA parameters. These parameters correspond to the output voltage, constant output current, constant output power voltage threshold, output overvoltage threshold, and output undervoltage threshold registers of the InnoSwitch3-Pro IC, respectively. The status of the InnoSwitch3-Pro IC is read by the VP302 from the telemetry registers also using the I^2C interface.

Capacitor C16 provides decoupling for the VCC of the VP302 IC. Capacitors C17 and C18, resistors R24 and R25, and Zener diodes VR1 and VR2, provide protection from ESD to pins CC1 and CC2.

Thermistor R25 is connected to the NTC pin of the VP302 IC to provide temperature detection of the USB Type-C receptacle. The VBUS pin of the VP302 IC is used to sense the output voltage at the USB Type-C receptacle. The VBUS pin is also used to discharge capacitor C7 when the bus switch Q1 is opened.

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5 PCB Fabrication and Assembly Drawings

Finished PCB thickness is 1 mm or 0.039 inches. Copper weight is 2 oz. on all layers.

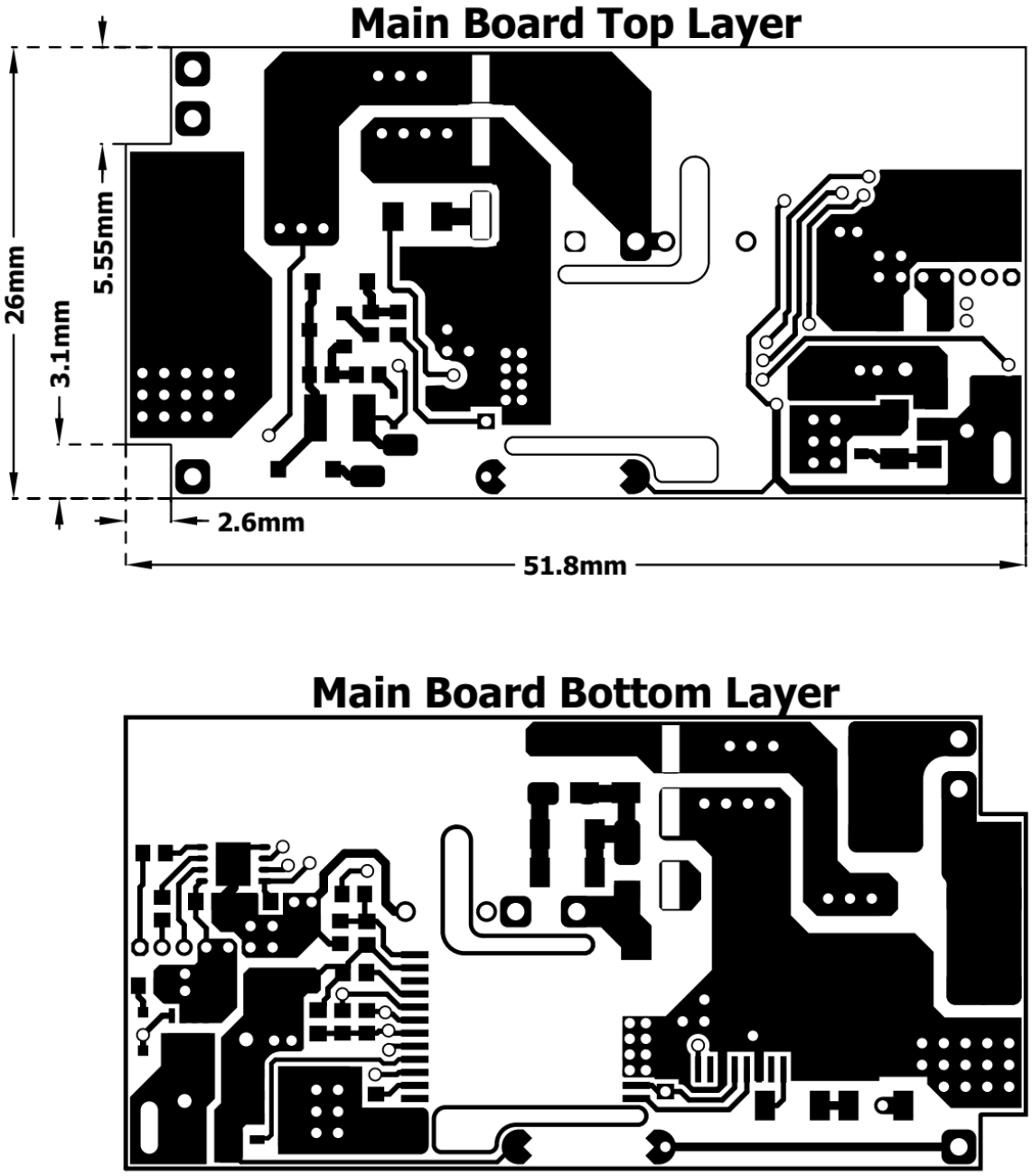

Figure 7 – DER-822 Rev B Main Board Top and Bottom Layers.

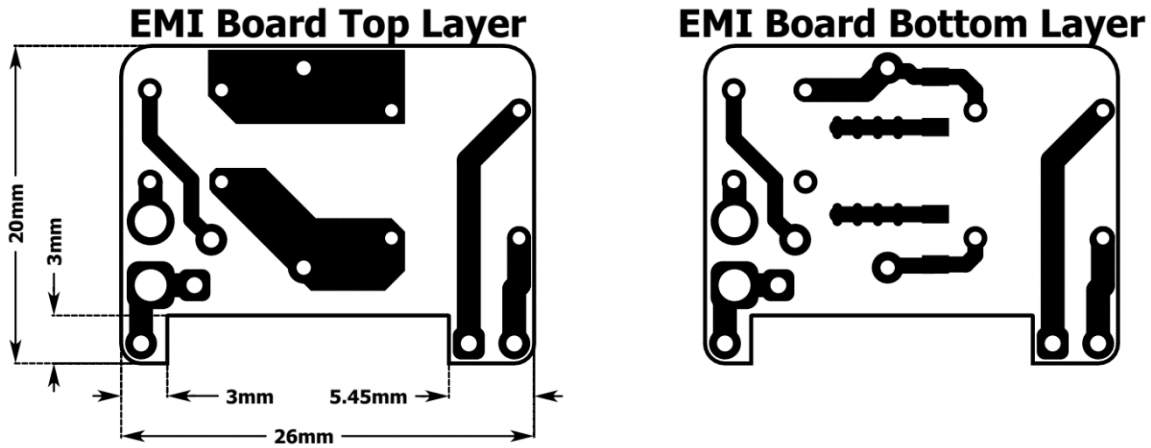

Figure 8 – DER-822 Rev B EMI Board Top and Bottom Layers.

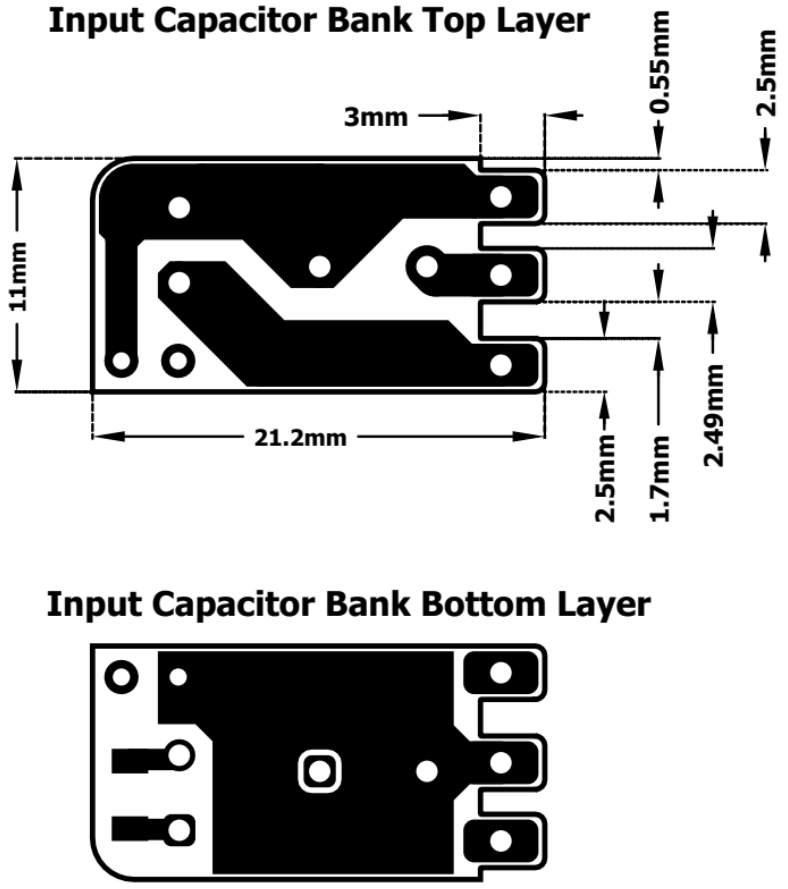

Figure 9 – DER-822 Rev B Input Capacitor Board Top and Bottom Layers.

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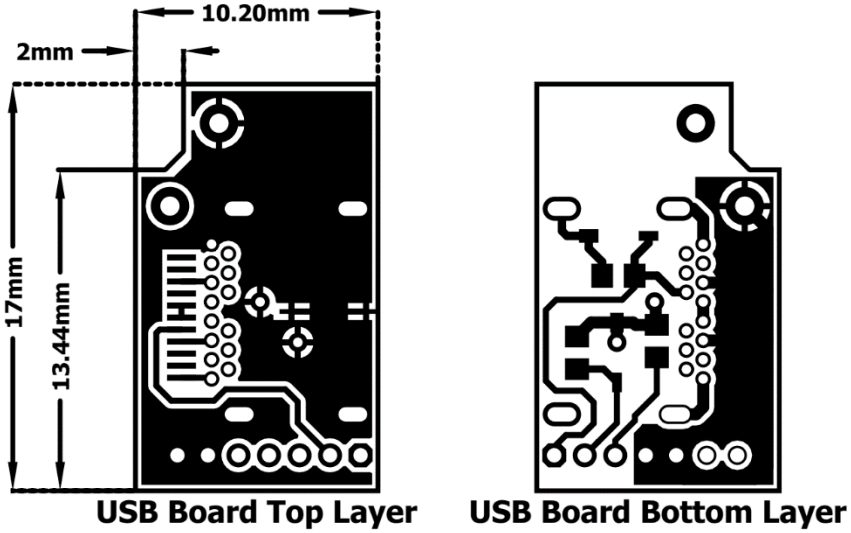

Figure 10 – DER-822 Rev B USB-C Board Top and Bottom Layers.

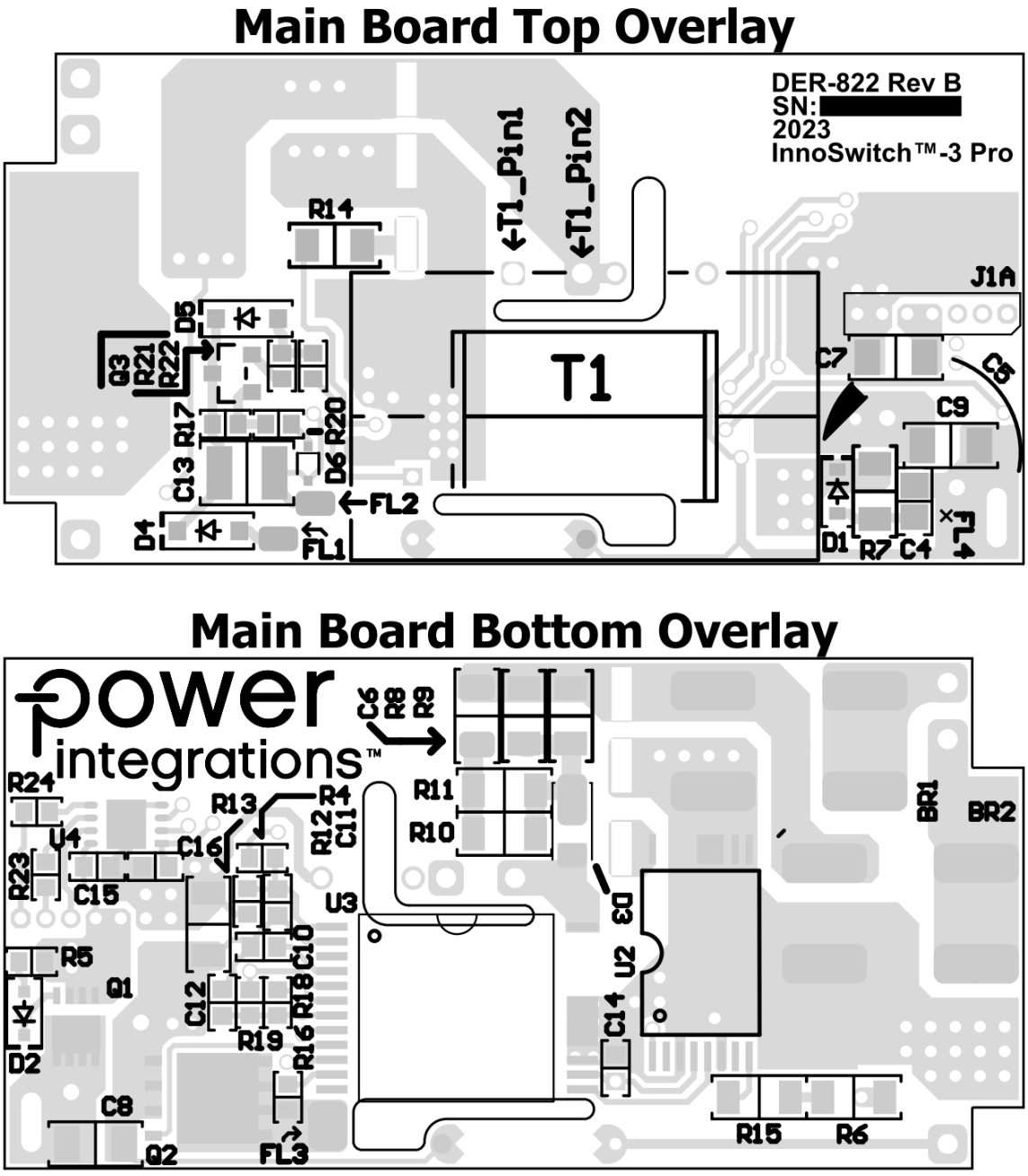

Figure 11 – DER-822 Rev B Main Board Top and Bottom Overlay.

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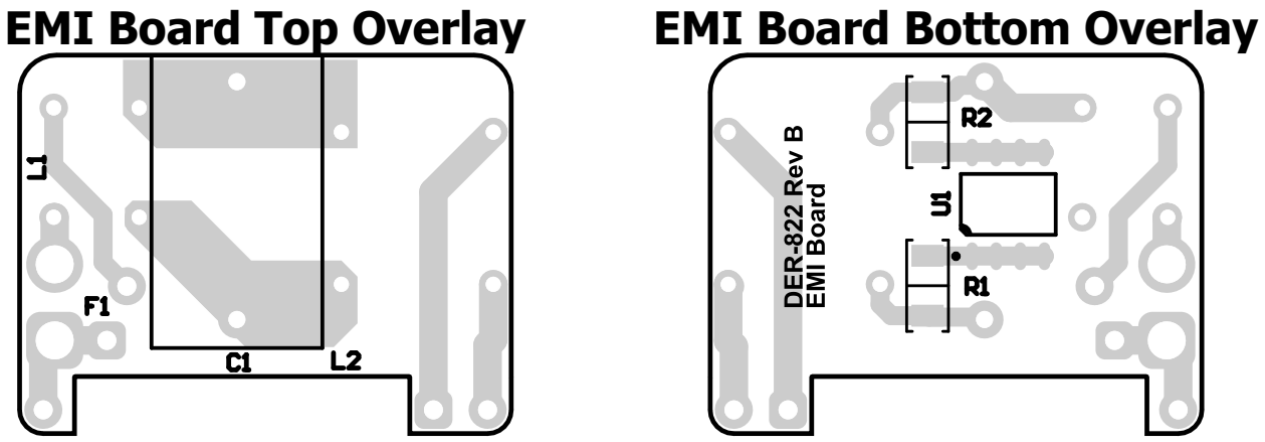

Figure 12 – DER-822 Rev B EMI Board Top and Bottom Overlay.

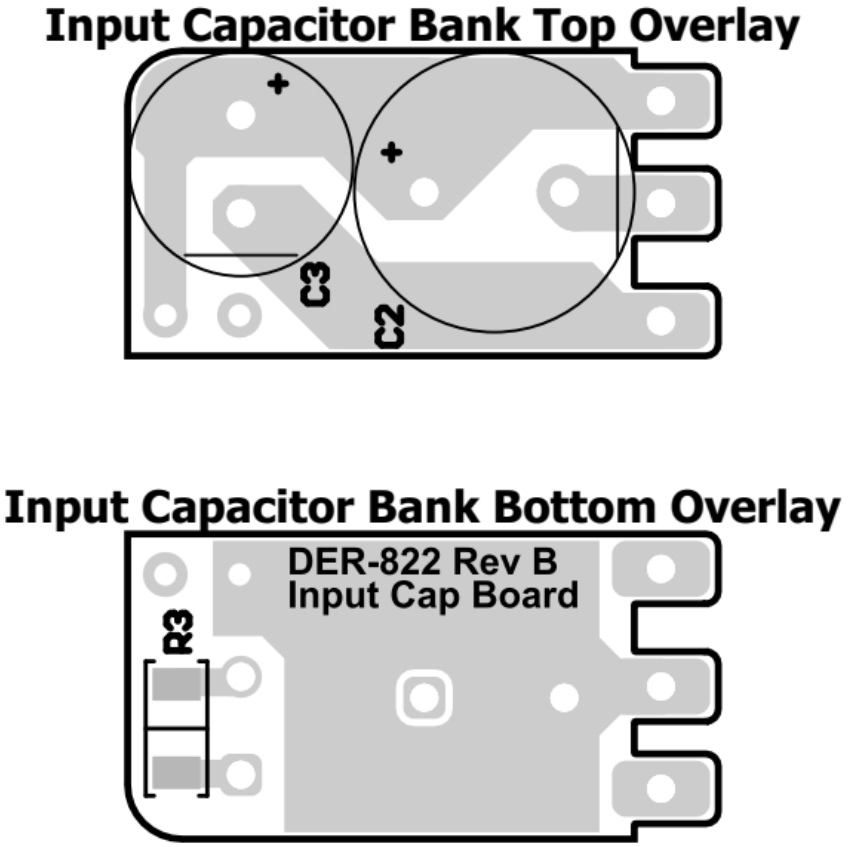

Figure 13 – DER-822 Rev B Input Capacitor Board Top and Bottom Overlay.

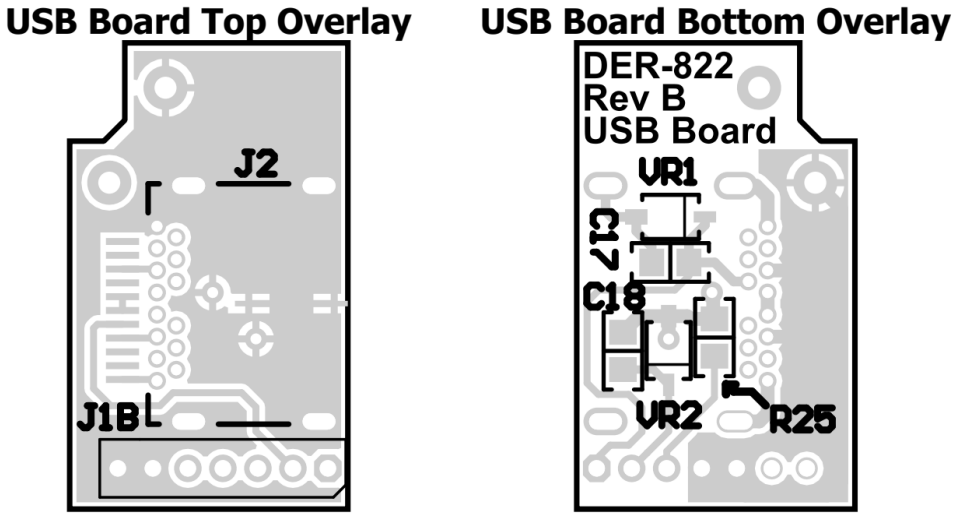

Figure 14 – DER-822 Rev B USB-C Board Top and Bottom Overlay.

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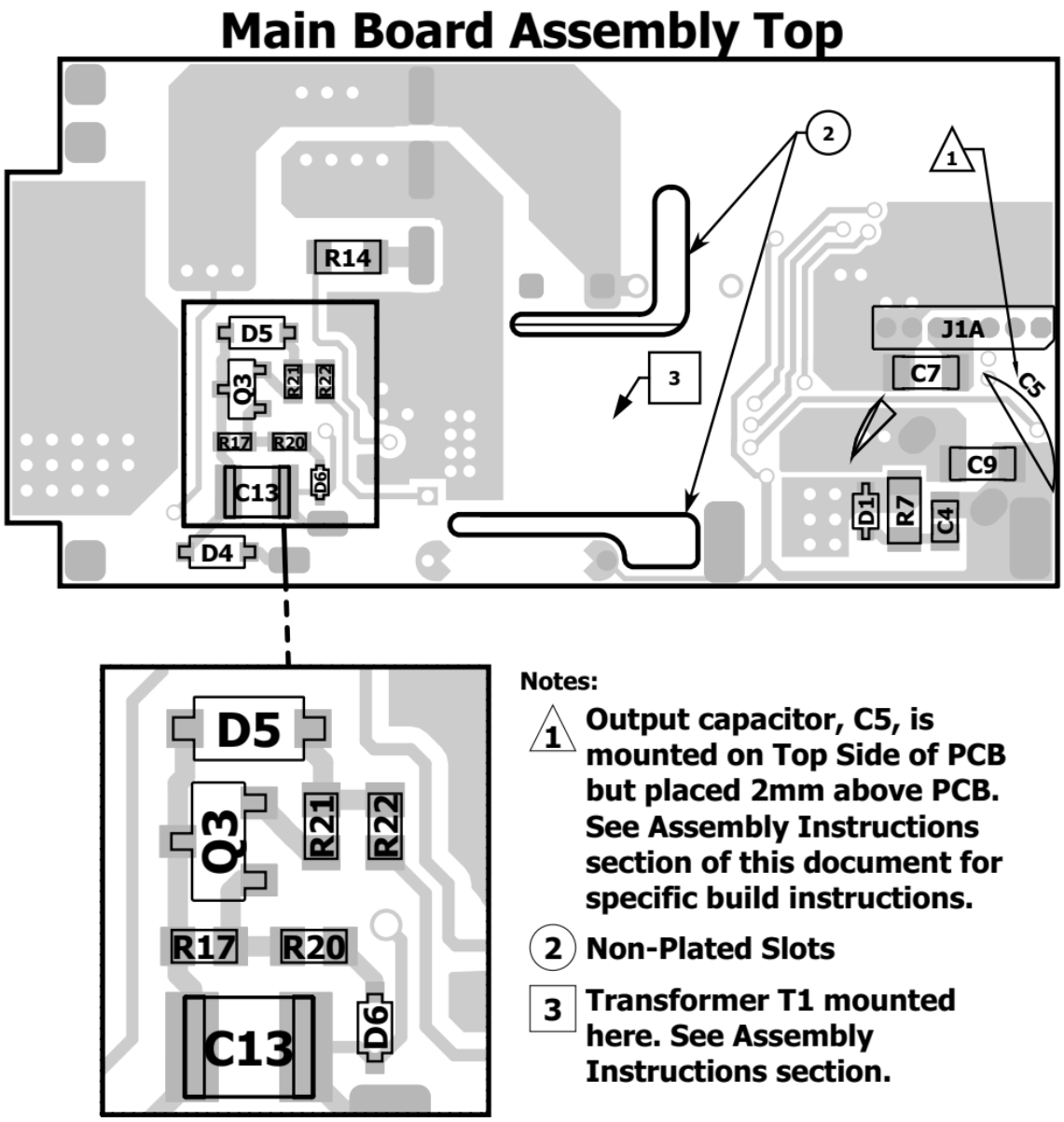

Figure 15 – DER-822 Rev B Main Board Assembly Top.

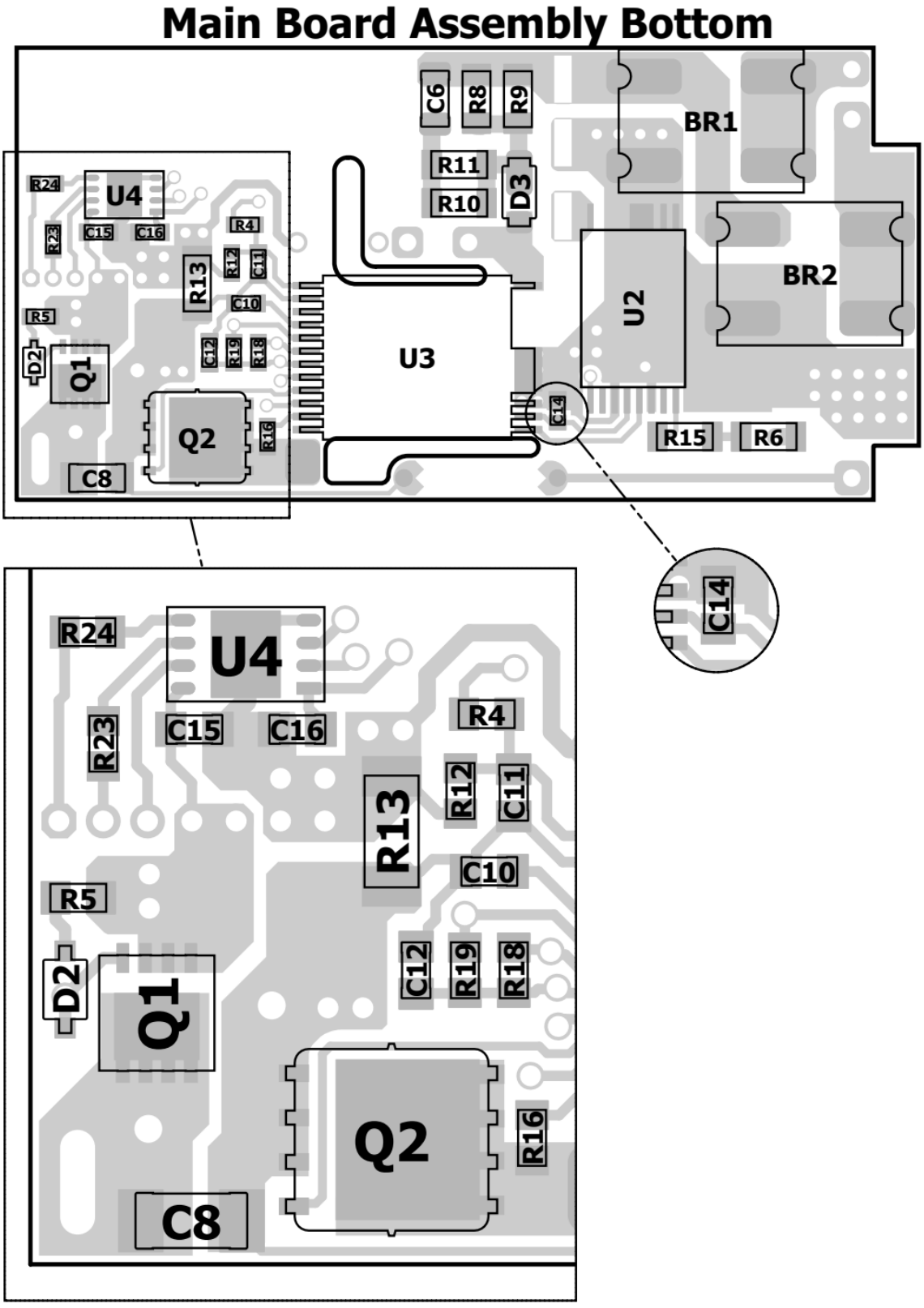

Figure 16 – DER-822 Rev B Main Board Assembly Bottom.

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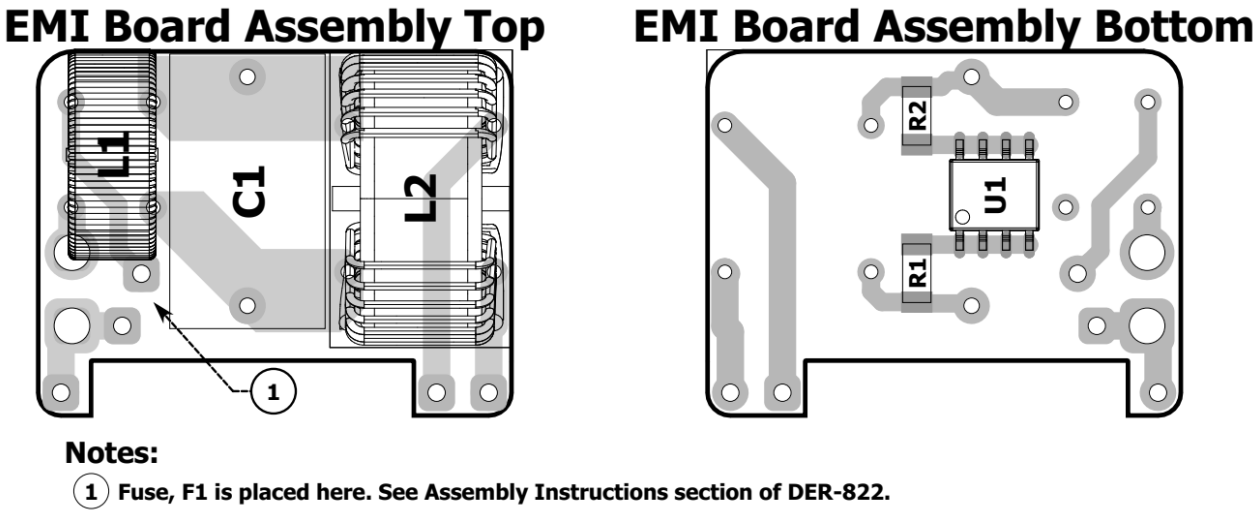

Figure 17 – DER-822 Rev B EMI Assembly Top and Bottom.

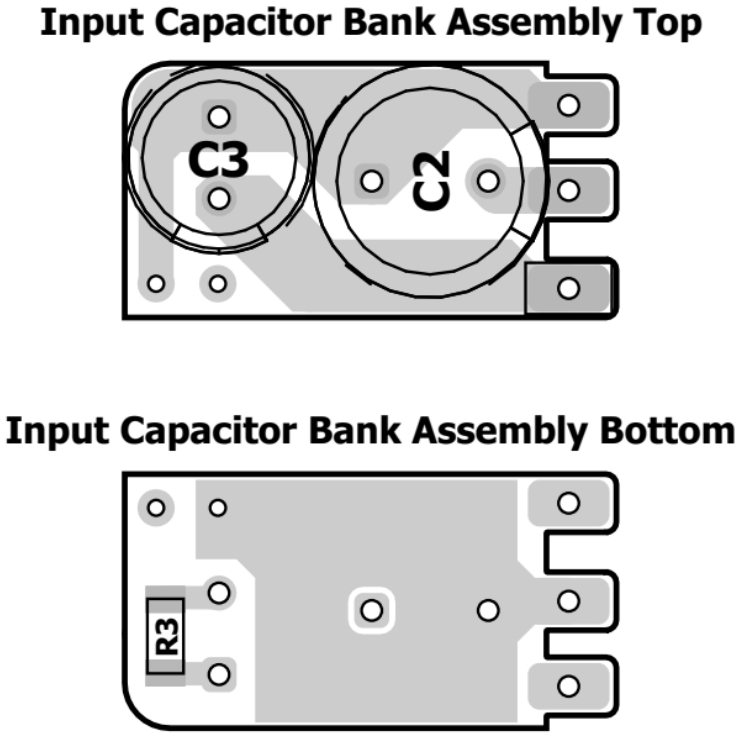

Figure 18 – DER-822 Rev B Input Capacitor Board Assembly Top and Bottom.

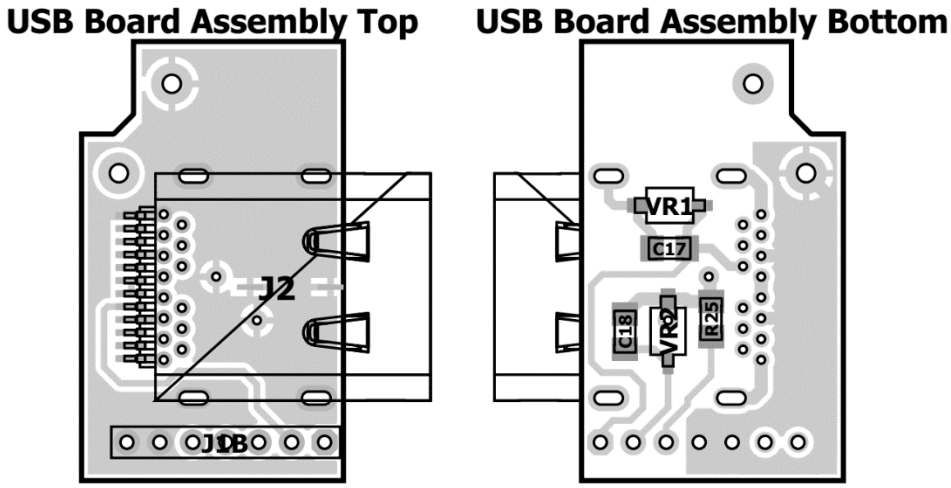

Figure 19 – DER-822 Rev B USB-C Board Assembly Top and Bottom.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	BR1, BR2	RECT BRIDGE, GP, 800V, 4A, Z4-D	Z4DGP408L-HF	Comchip
2	1	C1	330 nF, ±10%, 275 VAC, Polypropylene Film, X2, 15.00 mm x 8.50 mm	890324024003CS	Würth
3	1	C2	33 μF 400 V Aluminum Electrolytic Radial, Can 12000 Hrs @ 105°C	400BXW33MEFR10X30	Rubycon
4	1	C3	68 μF 160V Aluminum Electrolytic Radial, Can 12000 Hrs @ 105°C	160TXW68MEFR8X30	Rubycon
5	1	C4	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
6	1	C5	680 μF, ±20%, 25V, Aluminum Polymer Radial, Can, 292.56 mΩ, 1500 Hrs @ 125°C, (10 x 13.5)	687AVG025MGBJ	Illinois Capacitor
7	1	C6	CER 0805 2.2NF 250V X7R 10%	C0805C222KARACAUTO	KEMET
8	3	C7, C8 (DNP), C9	CER 10 μF 35V X7R 1206	CL31B106KLHNNNE	Samsung
9	5	C10, C11, C12, C15, C16	2.2 μF, 10 V, Ceramic, X7R, 0603	GRM188R71A225KE15D	Murata
10	1	C13	CER 10 μF 63V X7R 1210	CL32B106KMVNNWE	Samsung-
11	1	C14	4.7 μF, ±10%, 16 V, Ceramic, X5R, Low ESL, 0603	C1608X5R1C475K080AC	TDK
12	2	C17, C18	560 pF, 50 V, Ceramic, X7R, 0603, 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	CC0603KRX7R9BB561	Yageo
13	1	C19	2200 pF ±20% 250 VAC Ceramic E Radial, Disc	DE1E3RA222MN4AN01F	Murata
14	2	D1,D2	DIODE GEN PURP 200 V 200 mA SOD323	BAV21WS-7-F	Diodes, Inc.
15	1	D3	800 V, 1 A, Fast Recovery Rectifier, POWERDI123	DFLF1800-7	Diodes, Inc.
16	1	D4	DIODE, GEN PURP, FAST RECOVERY, 300 V, 225 mA, SOD323	BAV3004WS-7	Diodes, Inc.
17	1	D5	DIODE ZENER 47 V 500 mW SOD123	MMSZ5261BT1G	ON Semi
18	1	D6	10 V, 5%, 150 mW, SSMINI-2	EDZVT2R10B	Rohm
19	1	J1	Connector Header Through Hole, Right Angle 7 position 0.050" (1.27mm)	GRPB071VWCN-RC	Sullins Connector
20	1	J2	Connector, "Certified", USB - C, USB 3.1, For 0.062" PCB Material! ,Superspeed+, Receptacle Connector, 24 Pos, SMT, Right Angle, Through Hole	632723300011	Wurth
21	1	L1	250 μH, Toroidal Common Mode Choke, custom, DER-538, wound on 32-00275-00 core.	32-00367-00	Power Integrations
22	1	L2	Custom, CMC, 18 mH @ 10 kHz, Toroidal, 17.5 mm OD x 11.0 mm thick. 40 turns x 2, 0.40 mm wire 190 mΩ max	04291-T231	Sumida
23	1	Q1	MOSFET, N-CH, 30V, 48A (Ta), 50A (Tc), 6.2W (Ta), 8.3W (Tc), SMT, 8-DFN-EP (3.3x3.3)	AON7520C	Alpha & Omega Semi
24	1	Q2	MOSFET, N-CH, 120V, 85A (at VGS=10V), Trench Power AlphaSGT 120V TM Technology, DFN5x6	AONS62922	Alpha & Omega Semi
25	1	Q3	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1G	On Semi
26	3	R1, R2, R14	RES, 1 M, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105V	Panasonic
27	1	R3	RES SMD 3.9 MΩ 1% 1/4W 1206	RC1206FR-073M9L	Panasonic
28	1	R4	RES SMD 324 KΩ 1% 1/10W 0603	RC0603FR-07324KL	Yageo
29	1	R5	RES, 100 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1000V	Panasonic
30	1	R6	RES, 1.80 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
31	3	R7, R10, R11	RES, 20 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ200V	Panasonic
32	2	R8, R9	RES, 680 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ684V	Panasonic
33	1	R12	RES, 10 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
34	1	R13	0.009 Ω ±1% 1W Chip Resistor 1206 Automotive AEC-Q200, Current Sense Thick Film	PMR18EZPFU9L00	Rohm
35	1	R15	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
36	2	R16, R22	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic

37	2	R23, R24	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
38	1	R17	RES, 100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
39	2	R18 (DNP) R19 (DNP)	RES SMD 10 kΩ 1% 1/10W 0603	RC0603FR-0710KL	Yageo
40	1	R20	RES, 5.1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ512V	Panasonic
41	1	R21	RES SMD 2.4 kΩ 0.1% 1/10W 0603	RC0603FR-072K4L	Yageo
42	1	R25	THERM NTC 100 kΩ 4250K 0603	NTCG164KF104FT1S	TDK
43	1	T1	Custom, DER-822 Transformer ATQ23.7-14, Lp = 515 µH	Custom	Power Integrations
44	1	U1	CAPZero-3, SO-8C	CAP300DG	Power Integrations
45	1	U2	InnoSwitch3-Pro	INN3379C-H302	Power Integrations
46	1	U3	MinE-CAP	MIN1072M	Power Integrations
47	1	U4	IC, USB PD Type-C Controller for SMPS, DFN-8	VP302	VIA Labs
48	2	VR1, VR2	DIODE ZENER 24 V 150 mW EMD2	EDZVT2R24B	Rohm
49	1	F1	5 A, 250 V, Fast, Microfuse, Axial	0263005.MXL	Littlefuse

Note: Component references R18, R19, and C8, although present in the layout, should not be installed.

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7 Transformer Specification (T1)

7.1 *Electrical Diagram*

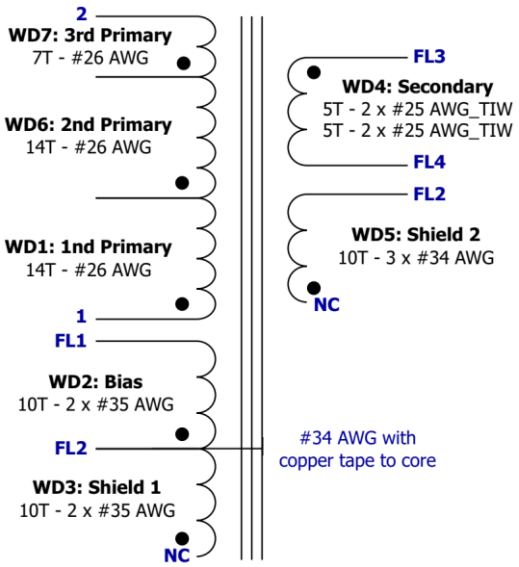

Figure 20 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Across pin 1 to pin 2, with all other windings open.	515 µH ± 5%
Resonant Frequency	Across pin 1 to pin 2, with all other windings open.	1,200 kHz (Min.)
Primary Leakage Inductance	Across pin 1 to pin 3, with FL3 and FL4 shorted.	7.7 µH (Max.)
LCR Meter Setting	L_S measurement, 100 kHz switching frequency, 1.0 V test level.	

7.3 *Material List*

Item	Description
[1]	Core: ATQ23.7-14, Mg/Zn Ferrite material. PI#: 99-00072-00.
[2]	Bobbin: BATQ23.7-14 horizontal. PI#: 25-01171-00.
[3]	Magnet Wire: #26 AWG, Double Coated.
[4]	Magnet Wire: #35 AWG, Double Coated.
[5]	Magnet Wire: #34 AWG, Double Coated.
[6]	Magnet Wire: #25 AWG, Triple Insulated Wire.
[7]	Copper Foil: Copper Tape, 1 mil Thickness, 5.0 mm Width
[8]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 7.0 mm Width.
[9]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 18.2 mm Width.
[10]	Varnish: Dolph BC-359.
[11]	Heat shrink: Heat Shrink 3/32” inner Diameter, Alpha Wire F221B3/32 BK100 or equivalent, cut. into ~1.5” length
[12]	Teflon Tubing, #24 AWG PTFE 20 mil OD. PI#:66-00133-00

7.4 *Transformer Build Diagram*

WD7 (Primary 3): 7T – #26 AWG

WD6 (Primary 2): 14T – #26 AWG

WD5 (Shield 2): 10T – 3 x #34 AWG

WD4 (Secondary): 5T – 4 x #25 AWG TIW

WD3 (Shield 1): 10T – 2 x #35 AWG
(wound together with…)
WD2 (Bias): 10T – 2 x #35 AWG

WD1 (Primary 1): 14T - #26 AWG

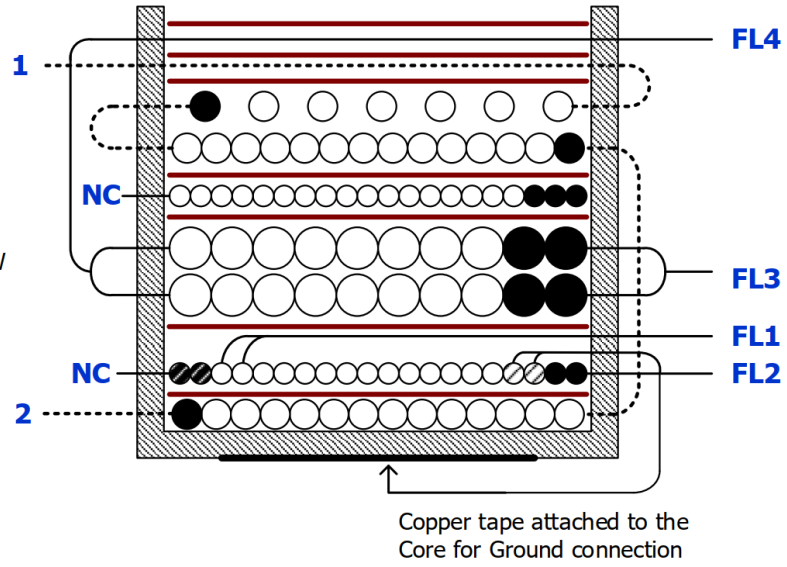

Figure 21 – Transformer Build Diagram.

7.5 *Transformer Construction*

Bobbin and Winding Preparation	Remove the pins of the bobbin but leave 2 adjacent pins on 1 side. Designate these pins as Pins 1 and 2. Bend the pins to offset the pin center to edge of the bobbin. Use a grinding wheel or a file to make slots in between the standoffs where the pins have been removes. The slots must be deep enough to reach the bobbin's inner drum. Label the slots as Slot 1, 2, 3, and 4. Position the bobbin on the mandrel such that the pins are on the left side when viewed from the top. Rotation of the mandrel is clockwise when viewed from the right.
WD1 1st Primary	Starting at pin 2, wind 1 layer with 14 turns of wire Item [3], going from left to right.
Insulation	Secure first layer of primary winding use tape Item [8]. Set aside primary wire for use later. Make sure remaining primary wire is long enough to complete the 35-turn primary.
WD2 Bias & WD3 Shield 1	Use 4 strands of Item [4]. Starting at Slot 1, wind 1 layer with 10 turns going right to left. Mandrel rotation is same as the previous winding. At the end of last turn, place tape Item [8] to secure the winding. Bring back 2 strands of wire to Slot 1 – this will be FL1 and termination of WD2. Cut the remaining 2 strands and leave as No-Connect (NC) – this will be the end of the Shield Winding 1.
Insulation	1 layer of tape Item [8].
WD4 Secondary	For WD4, use 2 strands of Item [6]. Start from slot 3 and wind 1 layer with 5 turns in the direction shown. End the winding in slot 4. Repeat the previous step with another 2 strands of Item [6]. Group all 4 wires – this will be the secondary winding.
Insulation	2 layers of tape Item [8].

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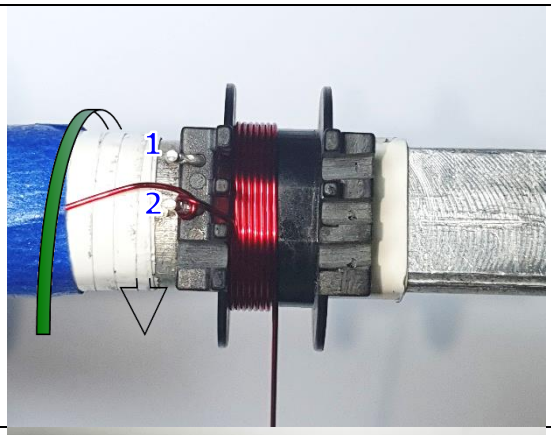
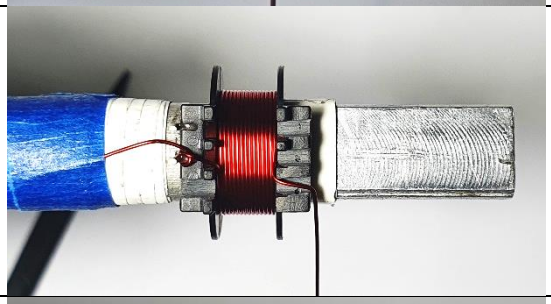
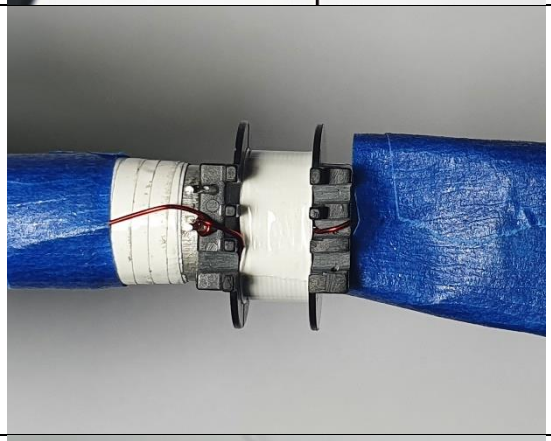
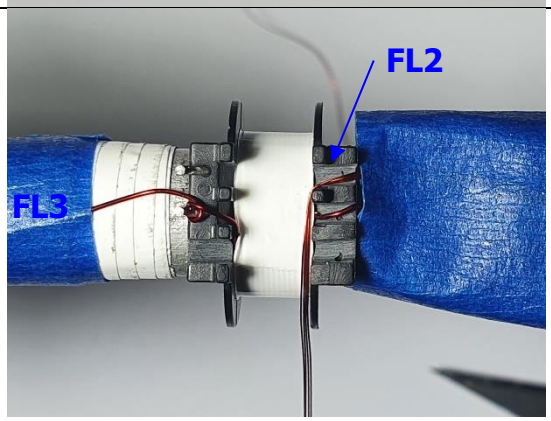
WD5 Shield 2	Again starting at Slot 1, wind 1 layer of 10 turns using 3 strands of Item [5] from left to right. Keep winding as flat as possible. Mandrel rotation is the same as the primary and first shield winding. At the end of last turn, place tape Item [8] to secure the winding, then cut the wires as No-Connect.
Insulation	1 layer of tape Item [8].
WD6 and WD7 2nd and 3rd Primary	Use wire hanging from WD1 and continue winding 14 turns from right to left. After 14 turns, place 1 layer of tape Item [8]. Wind the 7-turn 3rd layer of the primary from left to right. At the end of last turn, place tape Item [8] to secure the winding.
Insulation	Bend the end of the primary winding to Pin 1. Bend FL4 to Slot 3. Use a nylon sleeve Item [12] to protect the 2 wires of the bias winding, FL1. Twist together the other end of the bias winding with the shield windings – label this as FL2
Gap and Ground Core	Use shrink tube Item [12] to reinforce bias and shield winding insulation. Gap the middle leg of core Item [1] to get 515 μH ±5% primary inductance. Insert the cores into the bobbin and secure with copper tape Item [7], as shown. Solder one end of wire Item [5] to a section of the copper tape. Twist to combine this wire with FL2.
Insulate Core	Cover the transformer core with 2 layers of tape Item [9] to isolate core from the secondary.
Finish	Varnish using Item [10]. Position the fly leads to preparation for transformer installation.

7.6 *Winding Illustrations*

Bobbin Preparation		
Winding Preparation		Position the bobbin on the mandrel such that the pins are on the left side when viewed from the top. Rotation of the mandrel is clockwise when viewed from the right.
WD1 **1st Primary**		Starting at pin 2, wind 1 layer with 14 turns of wire Item [3], going from left to right.
Insulation		Secure first layer of primary winding use tape Item [8]. Set aside primary wire for use later. Make sure remaining primary wire is long enough to complete the 35-turn primary.
WD2: Bias **&** **WD3: Shield 1**		Use 4 strands of Item [4]. Starting at Slot 1, wind 1 layer with 10 turns going right to left. Mandrel rotation is same as the previous winding. At the end of last turn, place tape Item [8] to secure the winding. Bring back 2 strands of wire to Slot 1 – this will be FL1 and termination of WD2. Cut the remaining 2 strands and leave as No-Connect (NC) – this will serve as Shield 1.

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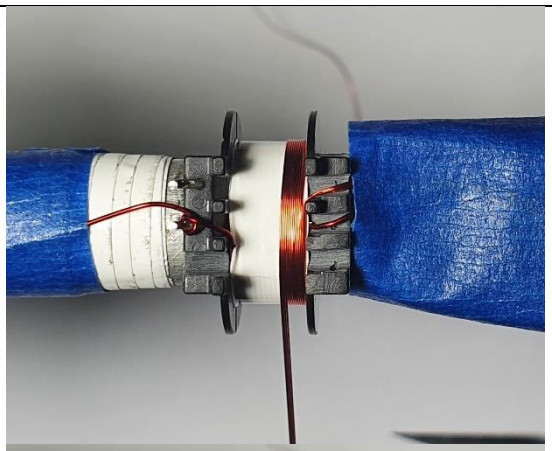
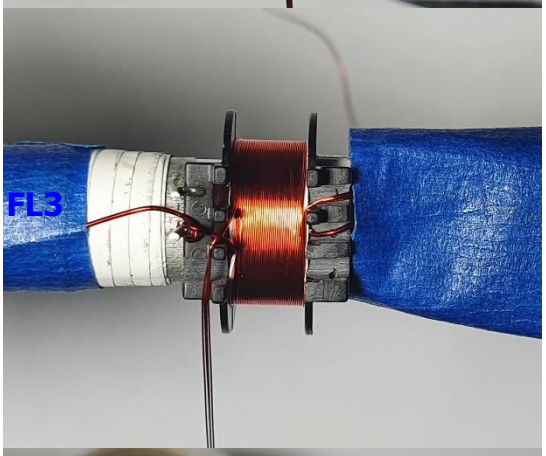
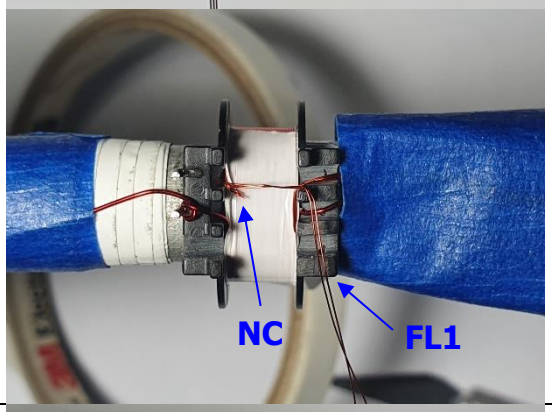
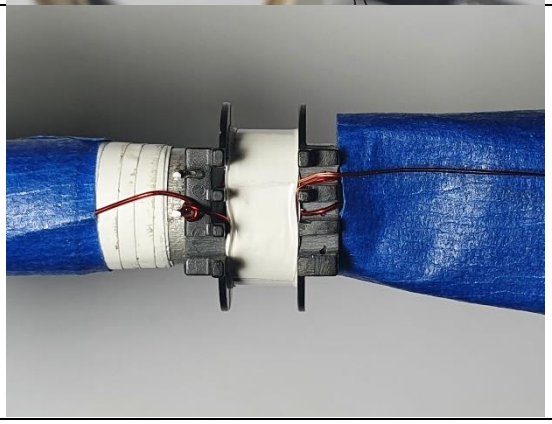
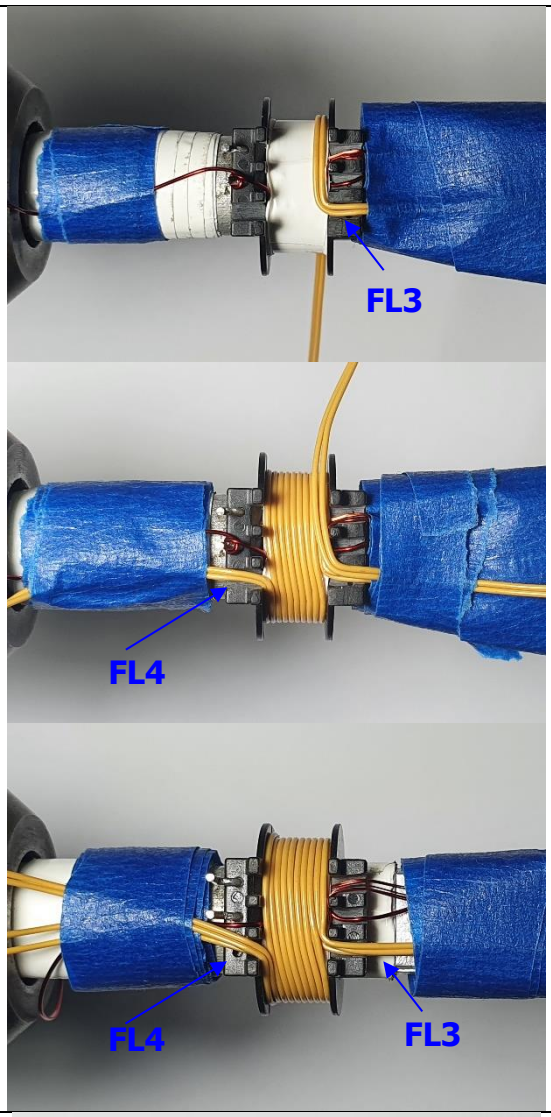
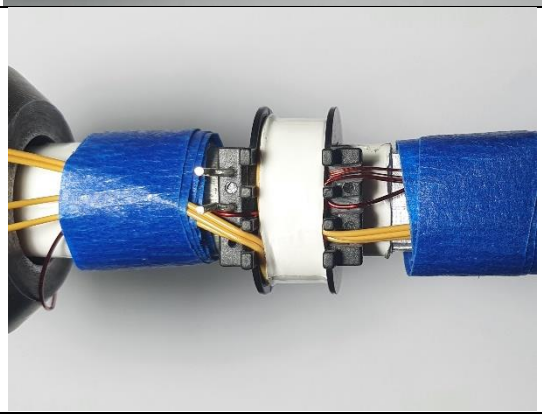
	  	
Insulation		1 layer of tape Item [8].

WD4 **Secondary**		For WD4, use 2 strands of Item [6]. Start from slot 3 and wind 1 layer with 5 turns in the direction shown. End the winding in slot 4. Repeat the previous step with another 2 strands of Item [6]. Group all 4 wires – this will be the secondary winding.
Insulation		2 layers of tape Item [8].

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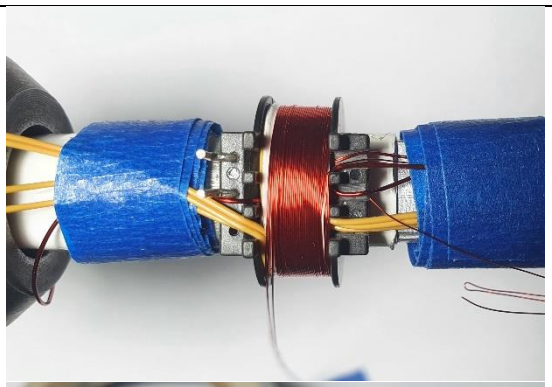
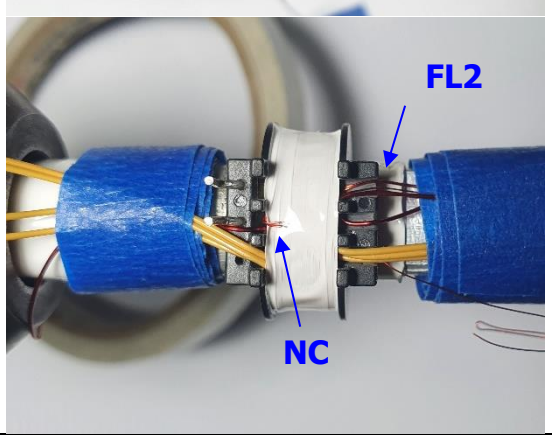
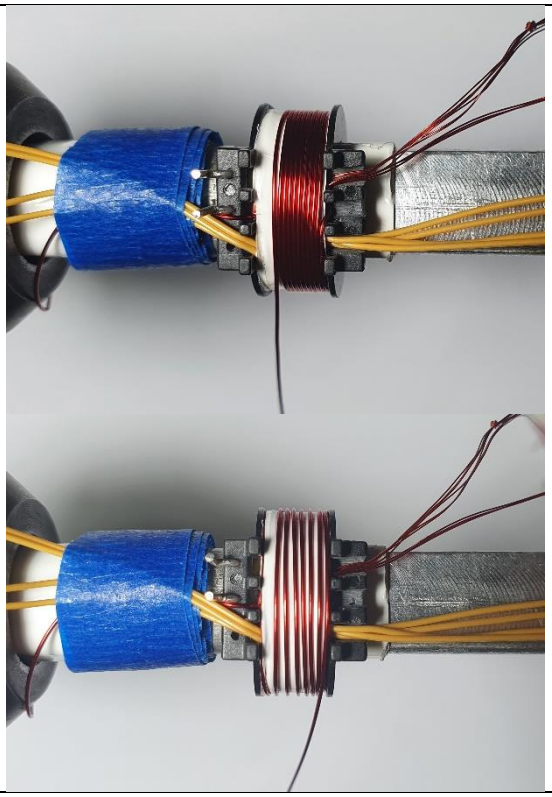
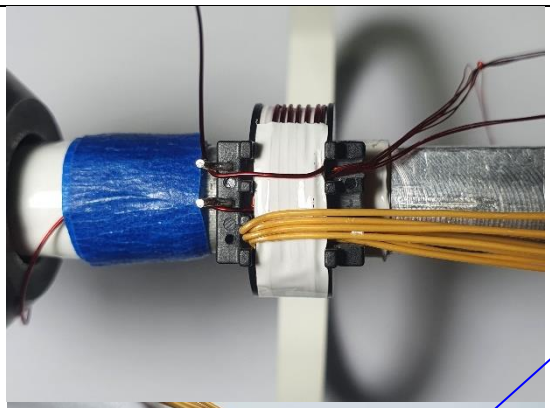
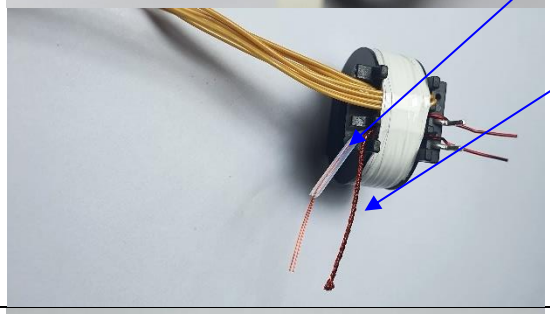
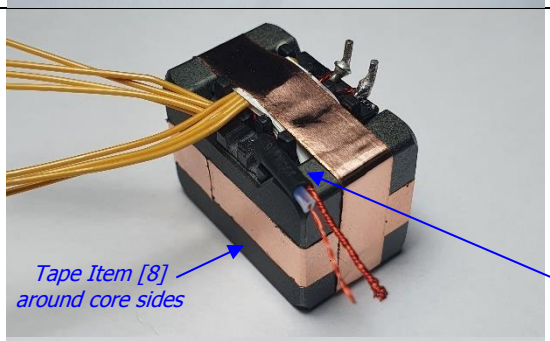
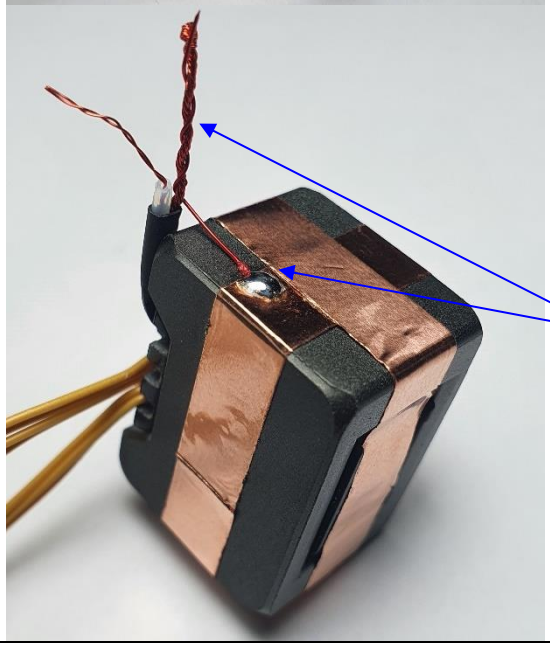
WD5 **Shield2**	 	Again starting at Slot 1, wind 1 layer of 10 turns using 3 strands of Item [5] from left to right. Keep winding as flat as possible. Mandrel rotation is the same as the primary and first shield winding. At the end of last turn, place tape Item [8] to secure the winding, then cut the wires as No-Connect.
Insulation		1 layer of tape Item [9].
WD6 and WD7 **2nd and 3rd Primary**		Use wire hanging from WD1 and continue winding 14 turns from right to left. After 14 turns, place 1 layer of tape Item [8]. Wind the 7-turn 3rd layer of the primary from left to right. At the end of last turn, place tape Item [8] to secure the winding.

Insulation	 	Bend the end of the primary winding to Pin 1. Bend FL4 to Slot 3. Use a 5mm long nylon sleeve Item [12] to protect the wires of the bias winding, FL1 Twist together the other end of the bias winding with the shield windings – label this as FL2
Gap and Ground Core	 	Use shrink tube Item [11] to reinforce the bias and shield winding insulation. Gap the middle leg of core Item [1] to get 515 µH ±5% primary inductance. Insert the cores into the bobbin and secure with copper tape Item [7], as shown. Solder one end of wire Item [5] to a section of the copper tape. Twist to combine this wire with FL2.

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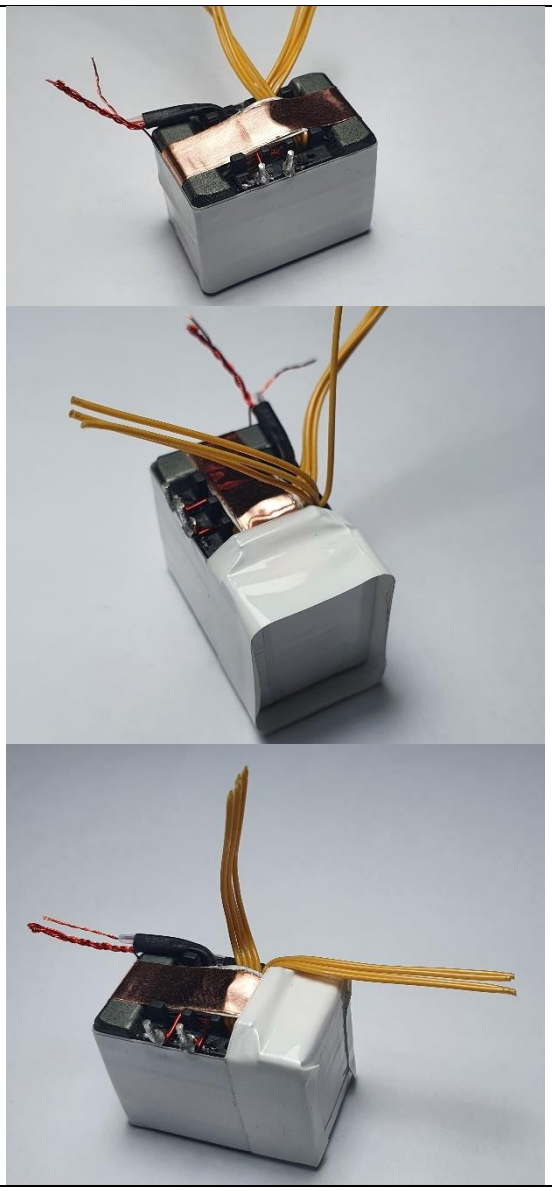
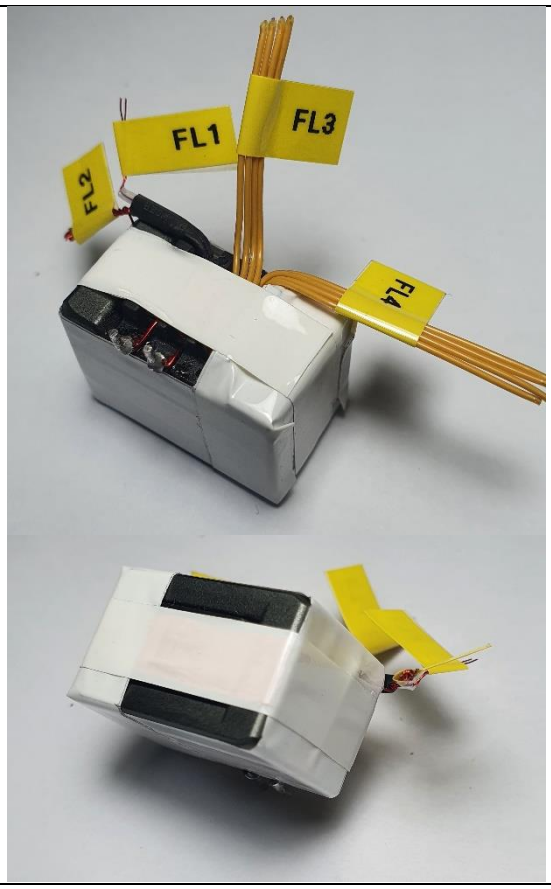
Insulate Core		Cover the transformer core with 2 layers of tape Item [9] to isolate core from the secondary.

Finish Assembly		Position the fly leads as shown. Solder the primary winding terminations to their corresponding pins.

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8 Common Mode Choke Specifications

8.1 *250 ·H Common Mode Choke (L1)*

8.1.1 Electrical Diagram

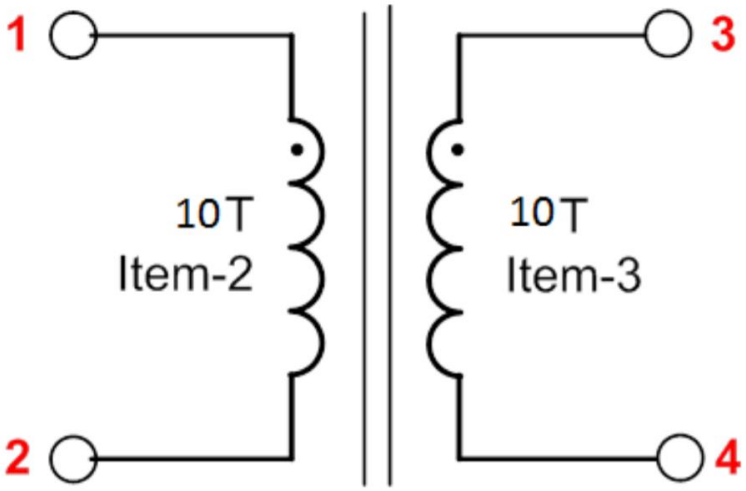


Figure 22 – Inductor Electrical Diagram.

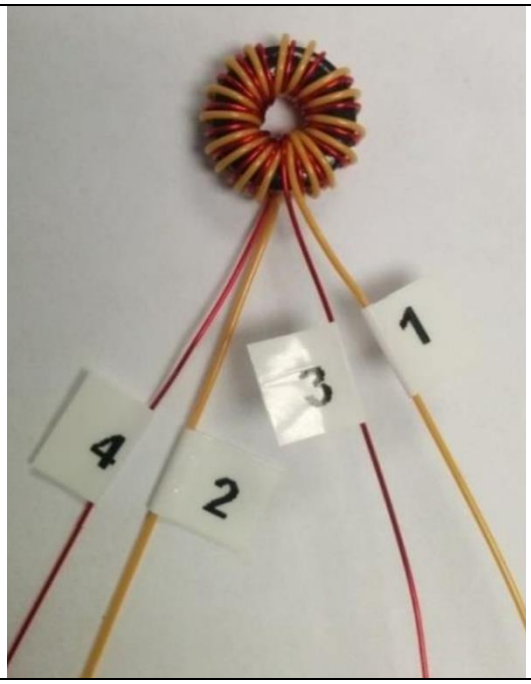
8.1.2 Electrical Specifications

Inductance	Across pin 1 to pin 2 (or pin 4 to pin 3) with the other winding open.	250 μH ±10%
LCR Meter Setting	L_S measurement, 100 kHz switching frequency, 1.0 V test level.	

8.1.3 Material List

Item	Description
[1]	Core, Ferrite Inductor Toroid; PI#: 32-00275-00.
[2]	Magnet Wire: #24 AWG, Triple Insulated Wire.
[3]	Magnet Wire: #24 AWG, Double Coated.
[4]	Varnish: Dolph BC-359.

8.1.4 Winding Instructions

	Start as Pin 1 for Item [2] and Pin 4 for Item [3]. Wind together 10 turns on core Item [1]. Mark end of Item [2] as Pin 2 and end of Item [3] as Pin 3. Varnish the CMC using Item [4].

8.2 ***18 mH Common Mode Choke (L2)***

8.2.1 Electrical Diagram

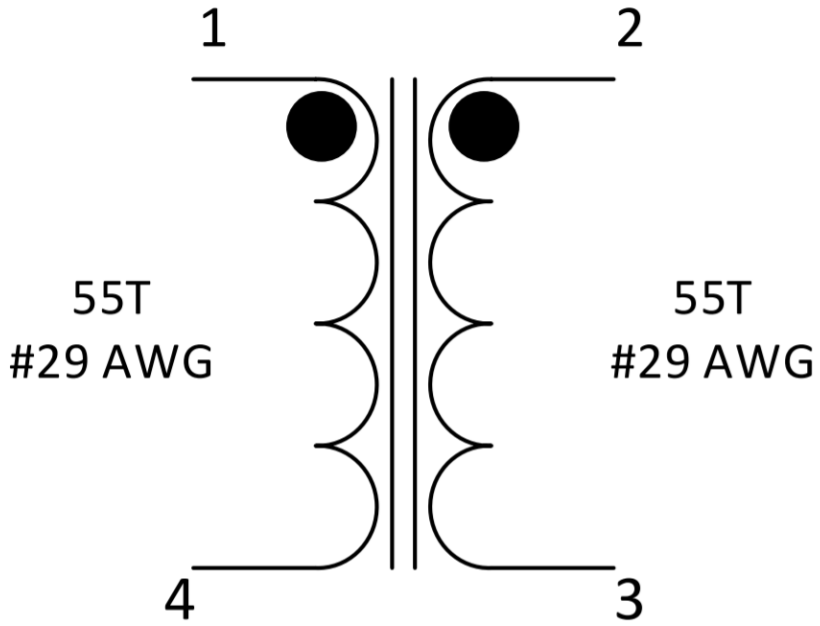


Figure 23 – Inductor Electrical Diagram.

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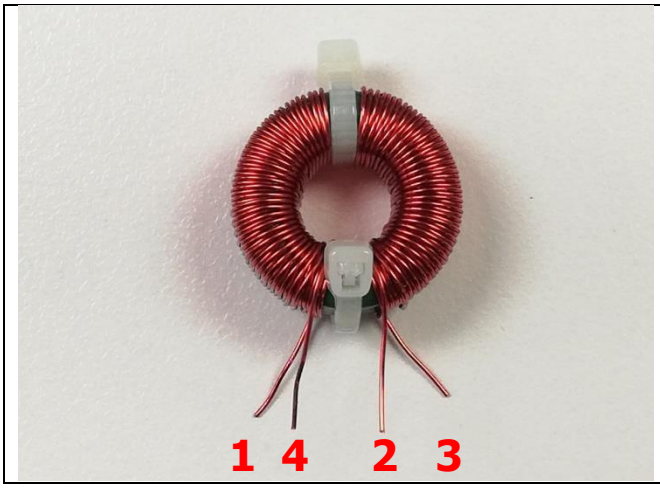
8.2.2 Electrical Specifications

Inductance	Across pin 1 to pin 4 (or pin 2 to pin 3) with the other winding open.	18 mH ±25%
Leakage Inductance	Across pin 1 to pin 4 (or pin 2 to pin 3) with the other winding shorted.	80 µH ±10%
LCR Meter Setting	L_S measurement, 100 kHz switching frequency, 1.0 V test level.	

8.2.3 Material List

Item	Description
[1]	Core, Ferrite Inductor Toroid, 14 mm OD x 8 mm ID x 5.5 mm H. PI#: 32-00286-00.
[2]	Cable Tie, PLT.6SM-M, 1.8mm Thick. PI#: 75-00202-00
[3]	Magnet Wire: #29 AWG, Double Coated.
[4]	Varnish: Dolph BC-359.
[5]	Heat shrink: Heat shrink 1” Inner diameter, 0.035” Wall Thickness. PI#: 62-00002-00; cut to 0.75” Length.

8.2.4 Winding Instructions



Place cable ties Item [2] to divide core Item [1] into two sections.

Start as Pin 1 with Item [3], wind 55 turns in two layers on half section of the core. Mark end of wire as Pin 4.

Repeat procedure on remaining half of core. Start as Pin 2 and end as Pin 3.

Remove cable ties and varnish the CMC using Item [4].

9 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-Pro_Flyback_050420; Rev.1.3; Copyright Power Integrations 2020	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-Pro Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VAC_MIN	90		90	V	Minimum AC line voltage
4	VAC_MAX	265		265	V	Maximum AC input voltage
5	VAC_RANGE			UNIVERSAL		AC line voltage range
6	FLINE			60	Hz	AC line voltage frequency
7	CAP_INPUT	100.0		100.0	uF	Input capacitance
9	**SET-POINT 1**					
10	VOUT1	21.00		21.00	V	Output voltage 1, should be the highest output voltage required
11	IOUT1	3.000		3.000	A	Output current 1
12	POUT1			63.00	W	Output power 1
13	EFFICIENCY1	0.9		0.92		Converter efficiency for output 1
14	Z_FACTOR1	0.50		0.50		Z-factor for output 1
16	**SET-POINT 2**					
17	VOUT2	20.00		20.00	V	Output voltage 2
18	IOUT2	3.000		3.000	A	Output current 2
19	POUT2			60.00	W	Output power 2
20	EFFICIENCY2	0.92		0.92		Converter efficiency for output 2
21	Z_FACTOR2	0.50		0.50		Z-factor for output 2
23	**SET-POINT 3**					
24	VOUT3	15.00		15.00	V	Output voltage 3
25	IOUT3	3.000		3.000	A	Output current 3
26	POUT3			45.00	W	Output power 3
27	EFFICIENCY3	0.92		0.92		Converter efficiency for output 3
28	Z_FACTOR3	0.50		0.50		Z-factor for output 3
30	**SET-POINT 4**					
31	VOUT4	9.00		9.00	V	Output voltage 4
32	IOUT4	3.000		3.000	A	Output current 4
33	POUT4			27.00	W	Output power 4
34	EFFICIENCY4	0.92		0.92		Converter efficiency for output 4
35	Z_FACTOR4	0.50		0.50		Z-factor for output 4
37	**SET-POINT 5**					
38	VOUT5	5.00		5.00	V	Output voltage 5
39	IOUT5	3.000		3.000	A	Output current 5
40	POUT5			15.00	W	Output power 5
41	EFFICIENCY5	0.92		0.92		Converter efficiency for output 5
42	Z_FACTOR5	0.50		0.50		Z-factor for output 5
44	**SET-POINT 6**					
45	VOUT6			0.00	V	Output voltage 6
46	IOUT6			0.000	A	Output current 6
47	POUT6			0.00	W	Output power 6
48	EFFICIENCY6			0.00		Converter efficiency for output 6
49	Z_FACTOR6			0.00		Z-factor for output 6
51	**SET-POINT 7**					
52	VOUT7			0.00	V	Output voltage 7
53	IOUT7			0.000	A	Output current 7
54	POUT7			0.00	W	Output power 7
55	EFFICIENCY7			0.00		Converter efficiency for output 7
56	Z_FACTOR7			0.00		Z-factor for output 7
58	**SET-POINT 8**					
59	VOUT8			0.00	V	Output voltage 8
60	IOUT8			0.000	A	Output current 8
61	POUT8			0.00	W	Output power 8
62	EFFICIENCY8			0.00		Converter efficiency for output 8
63	Z_FACTOR8			0.00		Z-factor for output 8

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65	**SET-POINT 9**					
66	VOUT9			0.00	V	Output voltage 9
67	IOUT9			0.000	A	Output current 9
68	POUT9			0.00	W	Output power 9
69	EFFICIENCY9			0.00		Converter efficiency for output 9
70	Z_FACTOR9			0.00		Z-factor for output 9
71						
72	VOLTAGE_CDC	0.000		0.000	V	Cable drop compensation desired at maximum output current
76	**PRIMARY CONTROLLER SELECTION**					
77	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
78	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
79	VDRAIN_BREAKDOWN	750		750	V	Device breakdown voltage
80	DEVICE_GENERIC	INN33X9		INN33X9		Device selection
81	DEVICE_CODE			INN3379C		Device code
82	PDEVICE_MAX			65	W	Device maximum power capability
83	RDSON_25DEG			0.44	Ω	Primary switch on-time resistance at 25°C
84	RDSON_100DEG			0.62	Ω	Primary switch on-time resistance at 100°C
85	ILIMIT_MIN			1.980	A	Primary switch minimum current limit
86	ILIMIT_TYP			2.130	A	Primary switch typical current limit
87	ILIMIT_MAX			2.279	A	Primary switch maximum current limit
88	VDRAIN_ON_PRSW			0.47	V	Primary switch on-time voltage drop
89	VDRAIN_OFF_PRSW			588.31	V	Peak drain voltage on the primary switch during turn-off
93	**WORST CASE ELECTRICAL PARAMETERS**					
94	FSWITCHING_MAX	77350		77350	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
95	VOR	145.0		145.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
96	VMIN			88.10	V	Valley of the rectified minimum input AC voltage at full load
97	KP			0.737		Measure of continuous/discontinuous mode of operation
98	MODE_OPERATION			CCM		Mode of operation
99	DUTYCYCLE			0.623		Primary switch duty cycle
100	TIME_ON			12.10	us	Primary switch on-time
101	TIME_OFF			4.87	us	Primary switch off-time
102	LPRIMARY_MIN			489.3	uH	Minimum primary magnetizing inductance
103	LPRIMARY_TYP			515.0	uH	Typical primary magnetizing inductance
104	LPRIMARY_TOL	5.0		5.0	%	Primary magnetizing inductance tolerance
105	LPRIMARY_MAX			540.8	uH	Maximum primary magnetizing inductance
107	**PRIMARY CURRENT**					
108	IAVG_PRIMARY			0.750	A	Primary switch average current
109	IPEAK_PRIMARY			2.134	A	Primary switch peak current
110	IPEDESTAL_PRIMARY			0.501	A	Primary switch current pedestal
111	IRIPPLE_PRIMARY			2.030	A	Primary switch ripple current
112	IRMS_PRIMARY			1.041	A	Primary switch RMS current
114	**SECONDARY CURRENT**					
115	IPEAK_SECONDARY			14.940	A	Secondary winding peak current
116	IPEDESTAL_SECONDARY			3.504	A	Secondary winding pedestal current
117	IRMS_SECONDARY			5.663	A	Secondary winding RMS current

118	IRIPPLE_CAP_OUT			4.803	A	Output capacitor ripple current
122	**TRANSFORMER CONSTRUCTION PARAMETERS**					
123	**CORE SELECTION**					
124	CORE	CUSTOM	Info	CUSTOM		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
125	CORE NAME	ATQ23.7-14		ATQ23.7-14		Core code
126	AE	103.0		103.0	mm^2	Core cross sectional area
127	LE	38.2		38.2	mm	Core magnetic path length
128	AL	7200		7200	nH	Ungapped core effective inductance per turns squared
129	VE	3934		3934	mm^3	Core volume
130	BOBBIN NAME	BAQT23.7-14		BAQT23.7-14		Bobbin name
131	AW	24.4		24.4	mm^2	Bobbin window area
132	BW	6.60		6.60	mm	Bobbin width
133	MARGIN	0.0		0.0	mm	Bobbin safety margin
135	**PRIMARY WINDING**					
136	NPRIMARY			35		Primary winding number of turns
137	BPEAK			3499	Gauss	Peak flux density
138	BMAX			3161	Gauss	Maximum flux density
139	BAC			1498	Gauss	AC flux density (0.5 x Peak to Peak)
140	ALG			420	nH	Typical gapped core effective inductance per turns squared
141	LG			0.290	mm	Core gap length
142	LAYERS_PRIMARY	2		2		Primary winding number of layers
143	AWG_PRIMARY	26		26		Primary wire gauge
144	OD_PRIMARY_INSULATED			0.465	mm	Primary wire insulated outer diameter
145	OD_PRIMARY_BARE			0.405	mm	Primary wire bare outer diameter
146	CMA_PRIMARY			244.2	Cmils/A	Primary winding wire CMA
148	**SECONDARY WINDING**					
149	NSECONDARY			5		Secondary winding number of turns
150	AWG_SECONDARY			19		Secondary wire gauge
151	OD_SECONDARY_INSULATED			1.217	mm	Secondary wire insulated outer diameter
152	OD_SECONDARY_BARE			0.912	mm	Secondary wire bare outer diameter
153	CMA_SECONDARY			227.5	Cmils/A	Secondary winding wire CMA
155	**BIAS WINDING**					
156	NBIAS			10		Bias winding number of turns
160	**PRIMARY COMPONENTS SELECTION**					
161	**LINE UNDERVOLTAGE**					
162	BROWN-IN REQURED	72.00		72.00	V	Required line brown-in threshold
163	RLS			3.56	MΩ	Connect two 1.91 MOhm resistors to the V-pin for the required UV/OV threshold
164	BROWN-IN ACTUAL			71.40	V	Actual brown-in threshold using standard resistors
165	BROWN-OUT ACTUAL			64.58	V	Actual brown-out threshold using standard resistors
167	**LINE OVERVOLTAGE**					
168	OVERVOLTAGE_LINE			297.50	V	The device voltage stress will be higher than 650V when overvoltage is trigerred
170	**BIAS WINDING**					
171	VBIAS			9.00	V	The rectified bias voltage maybe too low to supply the BP pin: Increase the rectified bias voltage to a value higher than 9V
172	VF_BIAS			0.70	V	Bias winding diode forward drop
173	VREVERSE_BIASDIODE			115.66	V	Bias diode reverse voltage (not

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						accounting parasitic voltage ring)
174	CBIAS			10	uF	Bias winding rectification capacitor
175	CBPP			4.70	uF	BPP pin capacitor
179	**SECONDARY COMPONENTS SELECTION**					
180	**RECTIFIER**					
181	VDRAIN_OFF_SRFET			74.33	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
182	SRFET	AONS62922		AONS62922		Secondary rectifier (Logic MOSFET)
183	VBREAKDOWN_SRFET			120	V	Secondary rectifier breakdown voltage
184	RDSON_SRFET			7.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
188	**SET-POINTS ANALYSIS**					
189	**TOLERANCE CORNER**					
190	USER_VAC	90		90	V	Input AC RMS voltage corner to be evaluated
191	USER_ILIMIT	MIN		1.767	A	Current limit corner to be evaluated
192	USER_LPRIMARY	MIN		395.3	uH	Primary inductance corner to be evaluated
194	**SET-POINT SELECTION**					
195	SET-POINT	2		2		Select the set-point which needs to be evaluated
196	FSWITCHING			73171.3	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
197	VOR			138.1	V	Voltage reflected to the primary winding when the primary switch turns off
198	VMIN			89.89	V	Valley of the minimum input AC voltage
199	KP			0.794		Measure of continuous/discontinuous mode of operation
200	MODE_OPERATION			CCM		Mode of operation
201	DUTYCYCLE			0.607		Primary switch duty cycle
202	TIME_ON			8.29	us	Primary switch on-time
203	TIME_OFF			5.38	us	Primary switch off-time
205	**PRIMARY CURRENT**					
206	IAVG_PRIMARY			0.699	A	Primary switch average current
207	IPEAK_PRIMARY			1.911	A	Primary switch peak current
208	IPEDESTAL_PRIMARY			0.394	A	Primary switch current pedestal
209	IRIPPLE_PRIMARY			1.517	A	Primary switch ripple current
210	IRMS_PRIMARY			0.960	A	Primary switch RMS current
212	**SECONDARY CURRENT**					
213	IPEAK_SECONDARY			13.378	A	Secondary winding peak current
214	IPEDESTAL_SECONDARY			2.756	A	Secondary winding pedestal current
215	IRMS_SECONDARY			5.412	A	Secondary winding RMS current
216	IRIPPLE_CAP_OUT			4.505	A	Output capacitor ripple current
218	**MAGNETIC FLUX DENSITY**					
219	BPEAK			2750	Gauss	Peak flux density
220	BMAX			2594	Gauss	Maximum flux density
221	BAC			1030	Gauss	AC flux density (0.5 x Peak to Peak)

10 Adapter Case and Heat Spreader Assembly

10.1 *Adapter Case Dimensions*

10.1.1 Adapter Case Main Body Dimension

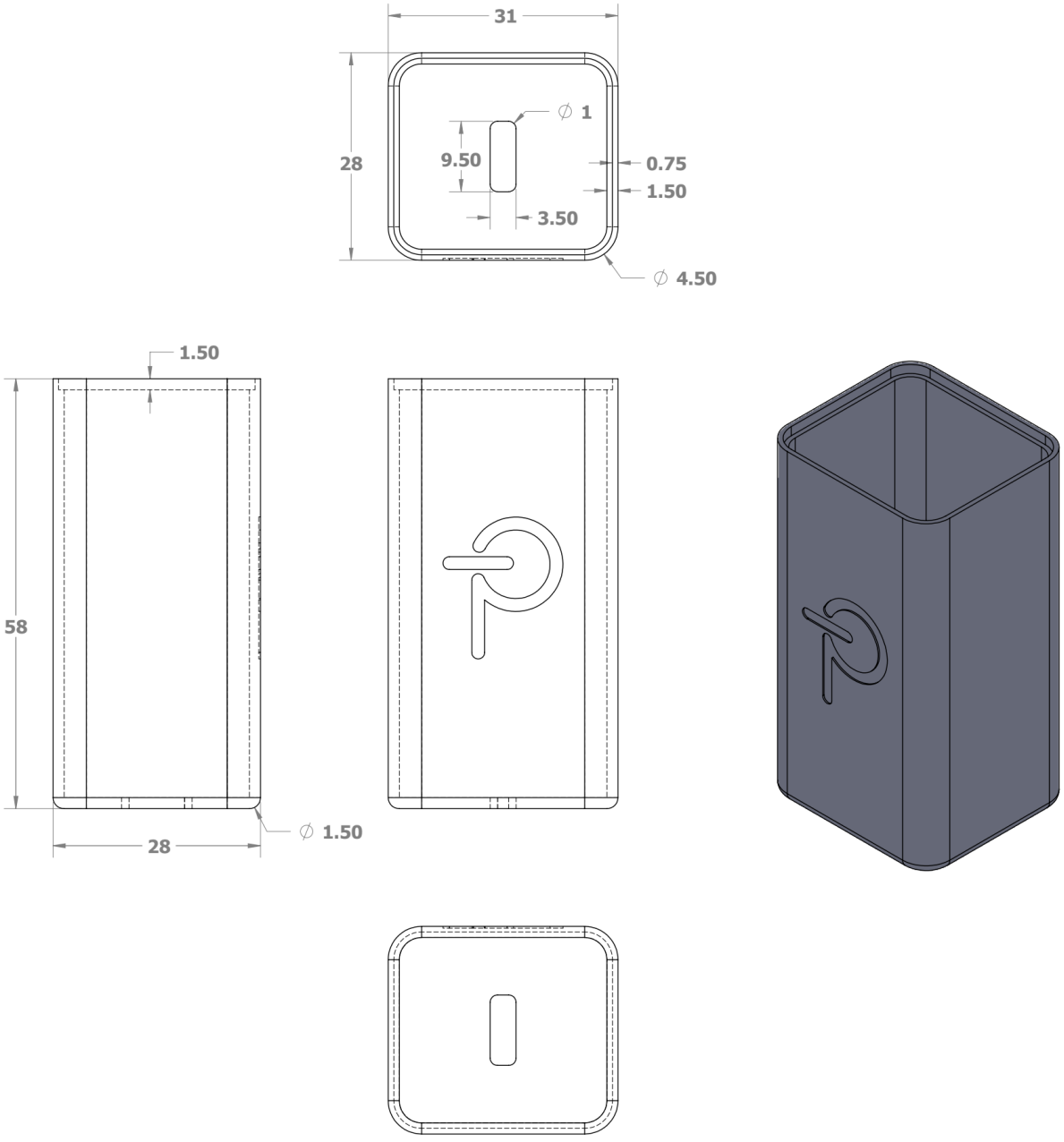

Figure 24 – DER-822 Adapter Main Body.

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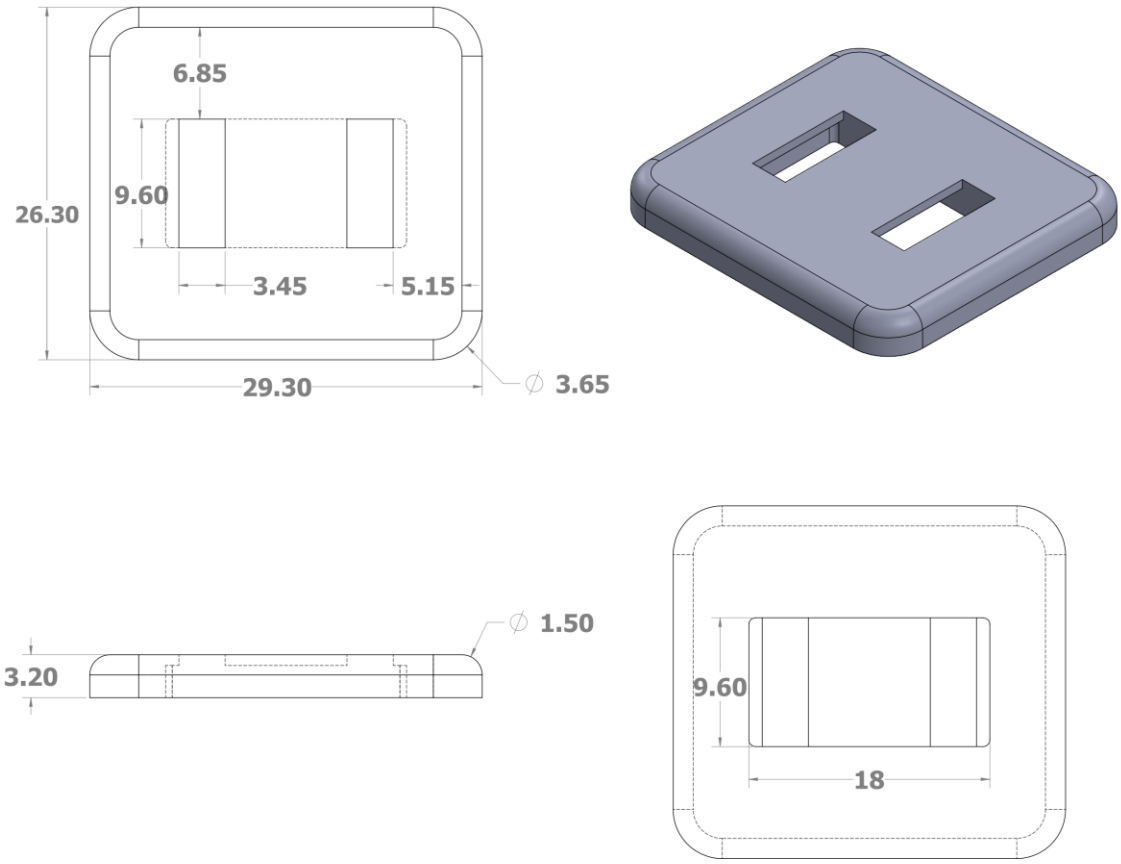

Figure 25 – DER-822 Adapter Case Cap.

10.1.2 Adapter Case Assembly

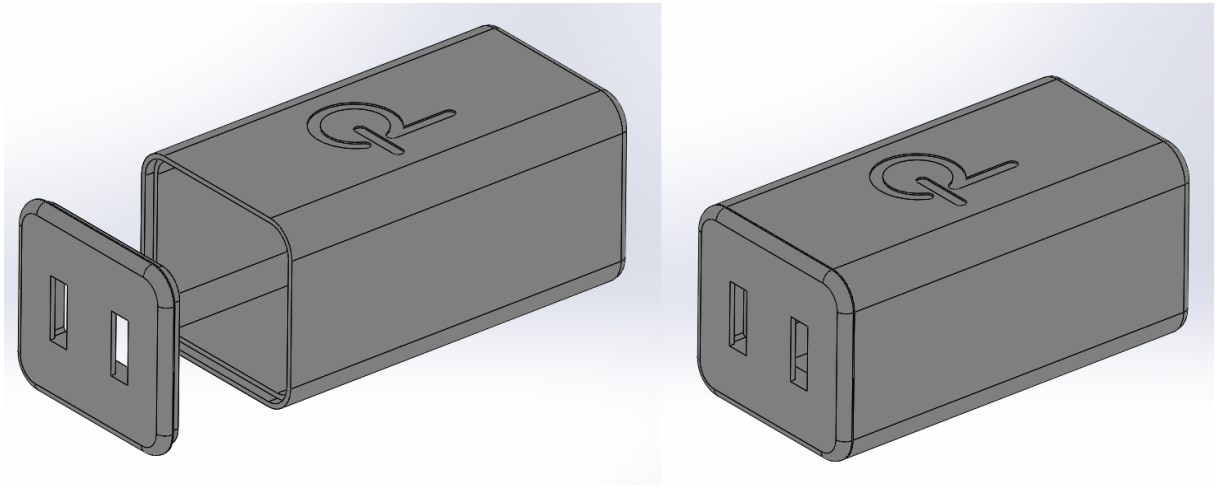

Figure 26 – DER-822 Case Assembly Drawing.

10.2 *Heat Spreader Drawings*

10.2.1 Aluminum Sheet

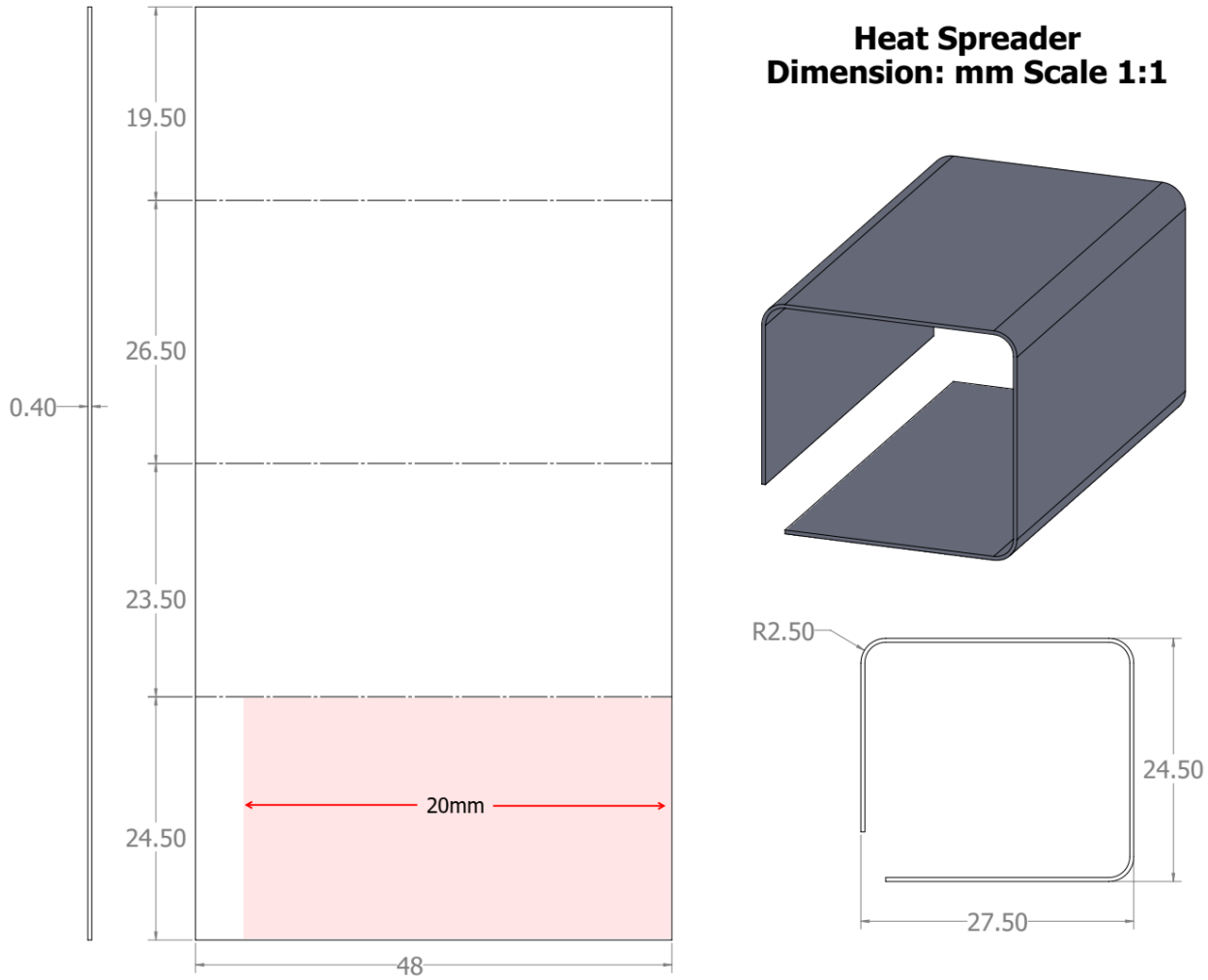

Figure 27 – Aluminum Heat Spreader.

Cover heat spreader entire inner area with tape except for area highlighted in red. Place tape on one face of the aluminum sheet only. Use two layers of 3M 1350-F, Polyester Film, 1 mil Thickness, 18.2 mm Width. Tape width greater than 18.2 mm can be also be used to minimize overlaps.

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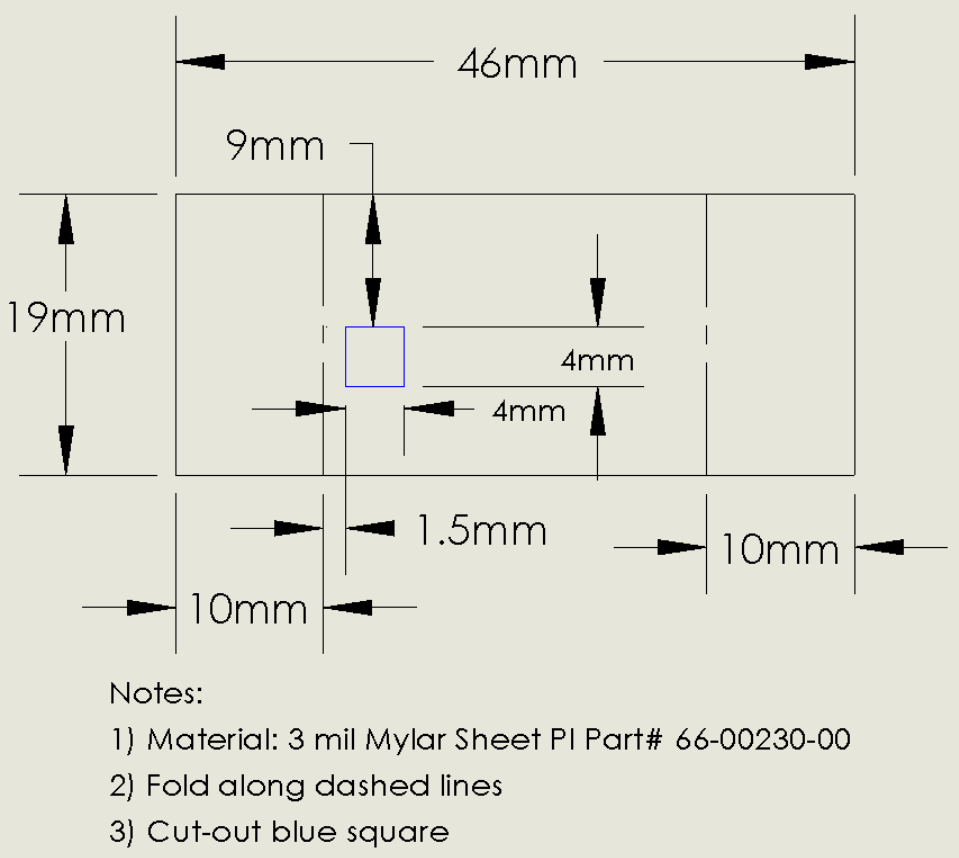
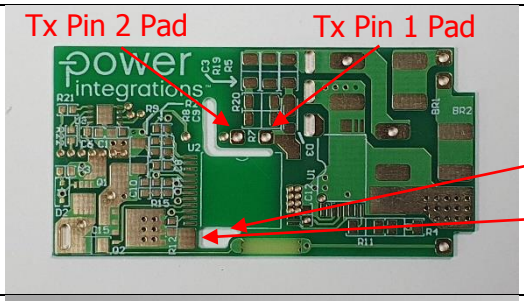
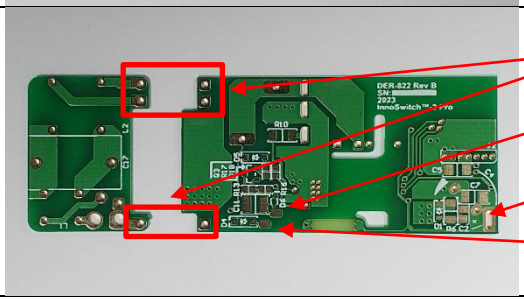
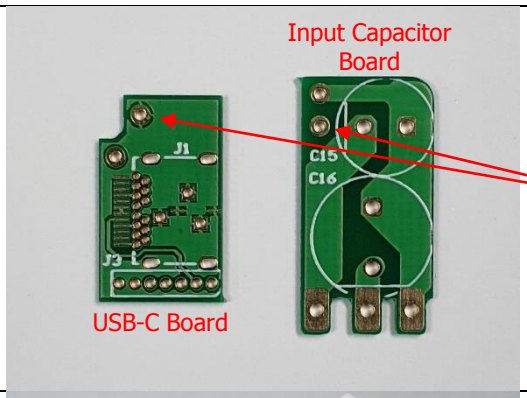
10.2.2 Heat Spreader Insulator



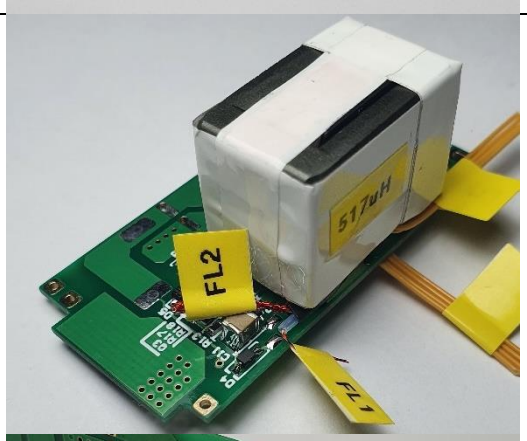
11 Assembly Instructions

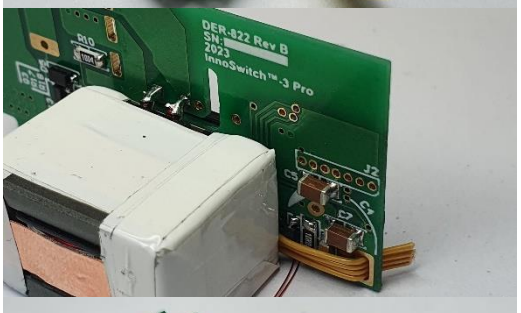
11.1 *Transformer Installation*

		Pad locations for transformer pins 1 and 2. Slot for FL3 FL3 Pad
		Connection pads for EMI and Main Board FL2 Pad FL4 Slot FL1 Pad



Pads for Y-capacitor, C19.





Position the transformer on the top side of the main PCB. Insert FL3 through the slot below the InnoSwitch IC to allow the transformer to sit flush on the board.

Insert Pins 1 and 2 to their corresponding pads and solder in place. Align FL1 and FL2 to their corresponding pads.

Insert FL4 in the slot near the edge of the board.

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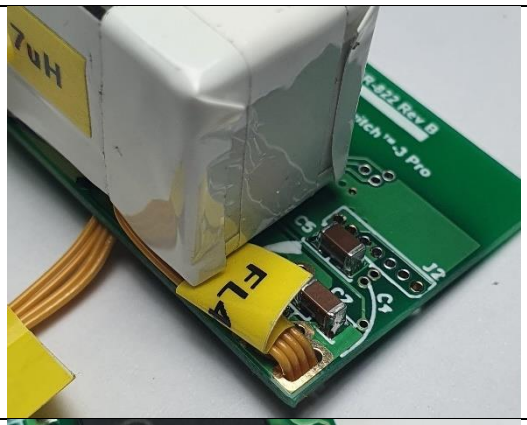

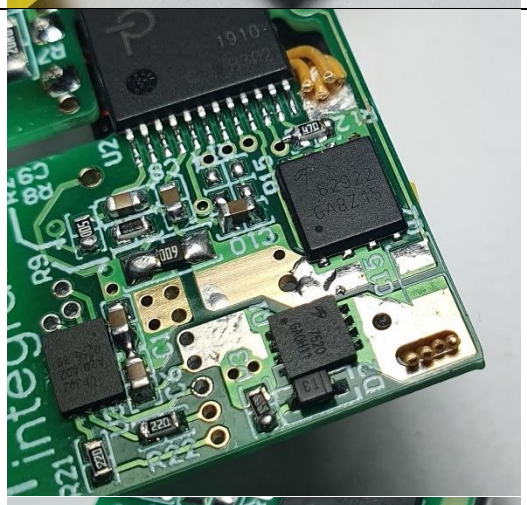

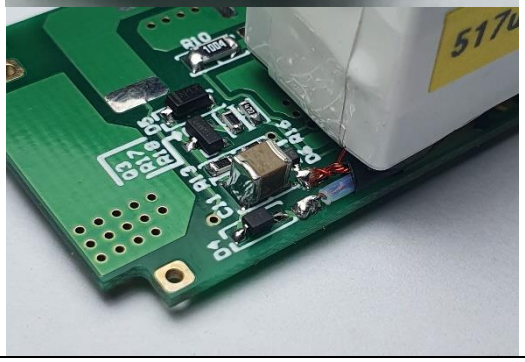

Trim FL3 and FL4. Bend FL3 to position it over the exposed pad as shown.

Solder FL3 to the exposed pad. Solder FL4 to the plated slot.

Finish installation of the transformer by trimming and soldering FL1 and FL2 to their corresponding pads.

11.2 ***Component Preparation***

 	Cover the upper half of the body of the input bulk capacitors using Polyester or Kapton tape. Use 2 layers of tape and ensure the metal vents are covered.
	Cut two pieces of 0.8mm inner diameter Teflon sleeve to a length of 2mm. Insert the sleeves into the leads of the output capacitor, C5.
	Cut a 0.8 mm inner diameter Teflon sleeve to lengths of 20 mm and 7.5 mm. Insert the sleeves into the leads of the Y-capacitor, C19. Bend the leads of the capacitor as shown.

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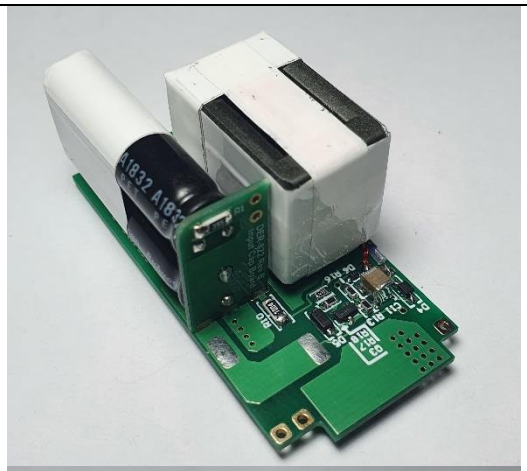
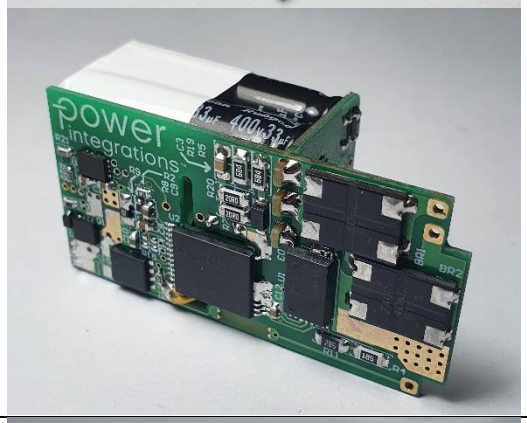
11.3 ***Unit Assembly***

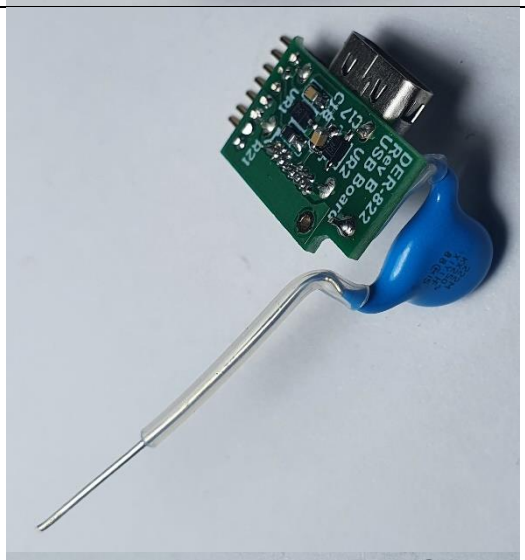
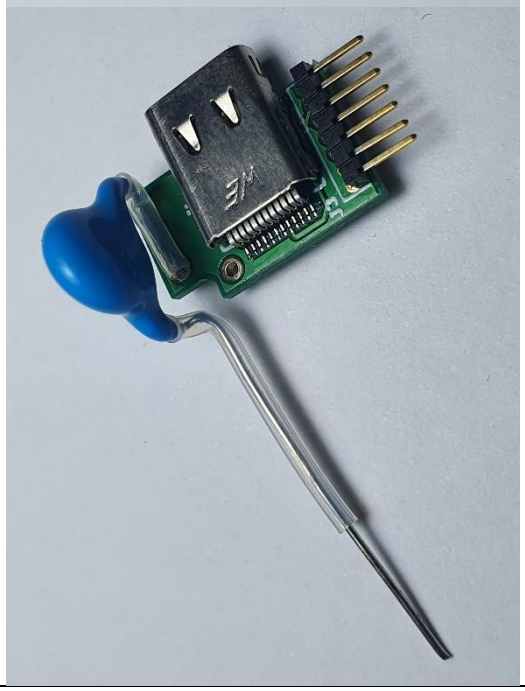




Important note: Always check that the Transformer is properly installed before installing the EMI, Input Capacitor, and PD Controller boards.

Install the input bulk capacitor PCB and solder the bottom tabs as shown.

Install the output capacitor. With the Nylon sleeve, the capacitor should be positioned 2 mm above the main PCB. Check to see that the bottom of the capacitor does not collide with the components below it.

  	Position and solder the Y-capacitor, C19, as shown in the image to the left.

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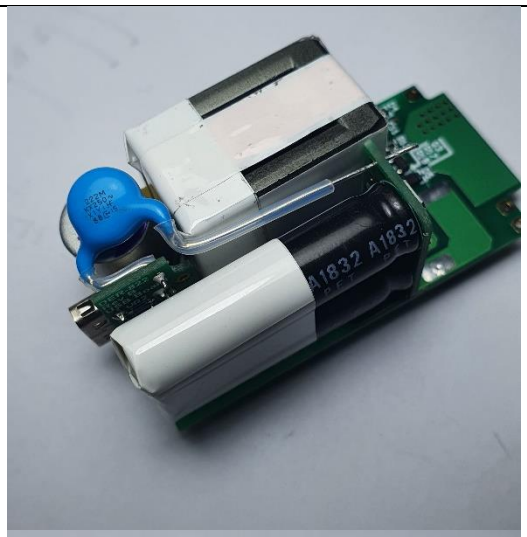
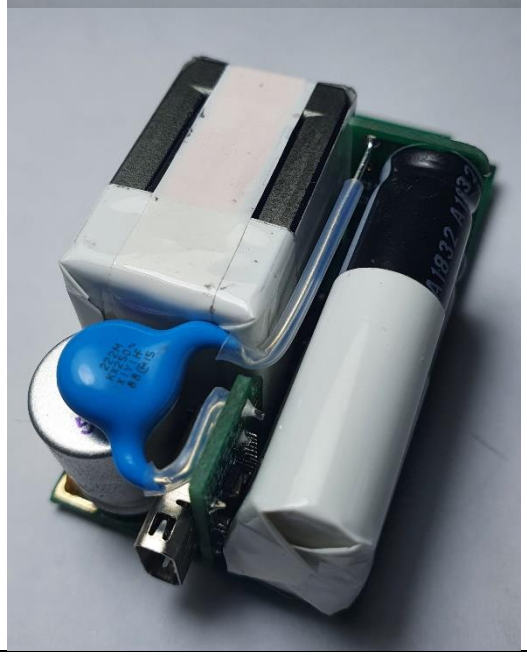
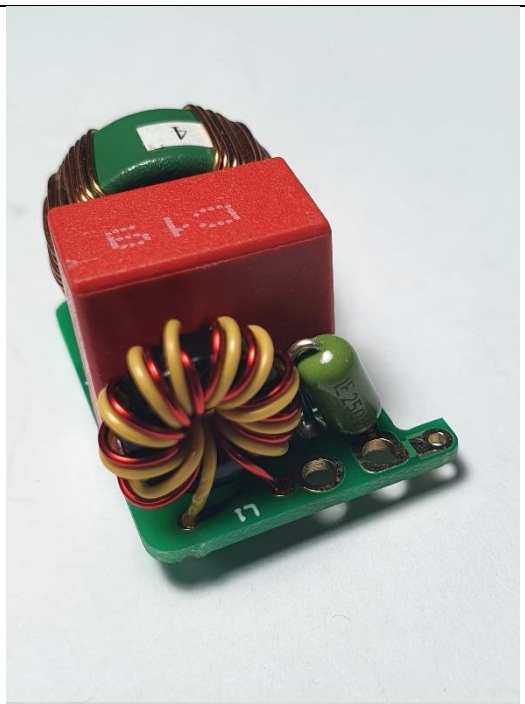
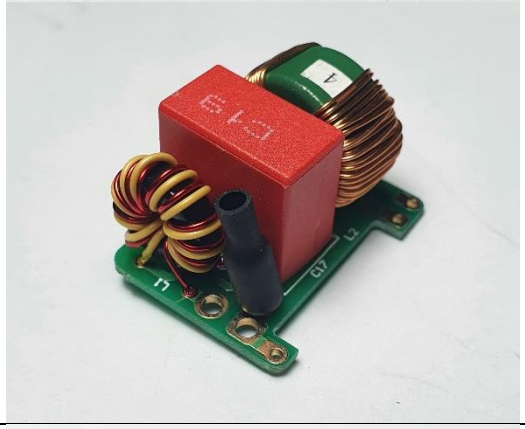
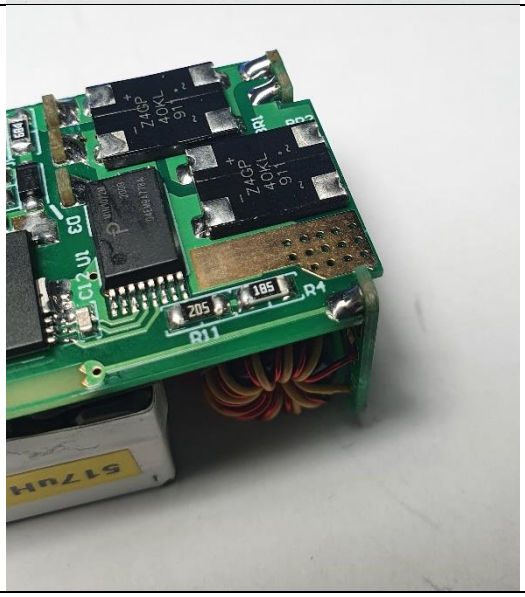




Insert the PD controller to the 7-pin header port in the main board. At the same time, insert the longer lead of the Y-capacitor to its corresponding pad found in the input capacitor board. Solder the PD controller board and Y-capacitor in place.

 	Insulate the fuse on the EMI board using a 5 mm diameter shrinkable tube.
	Position the EMI board to align with the pads located in the main board. Solder the EMI board in place. Make sure the EMI board is perpendicular to the main board.

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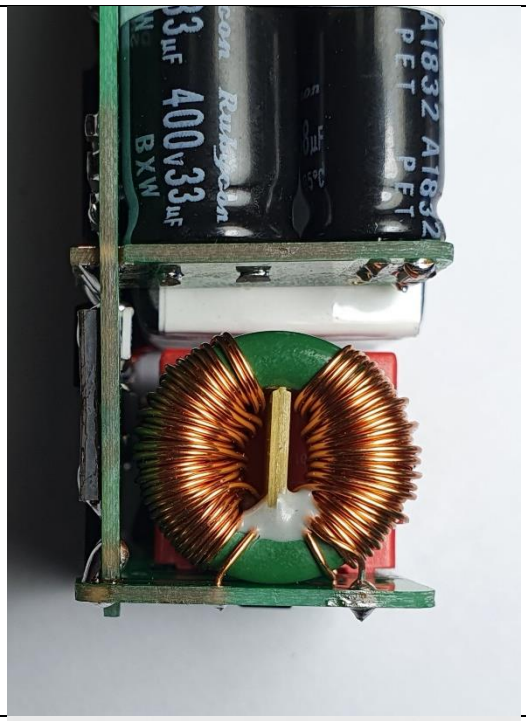
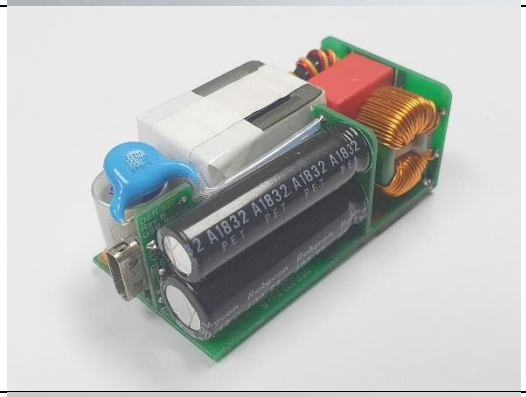
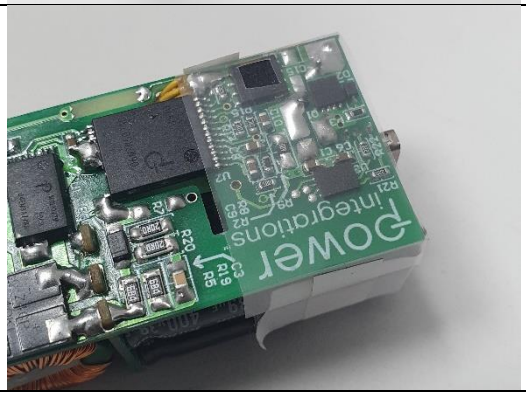
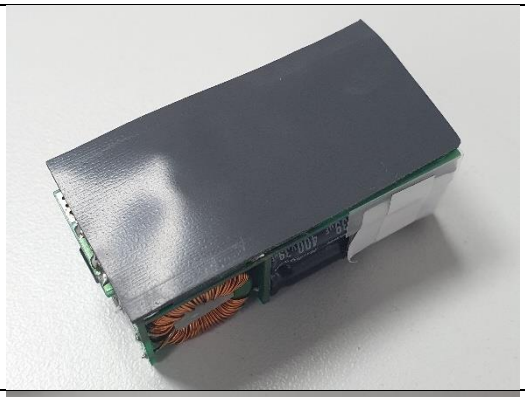
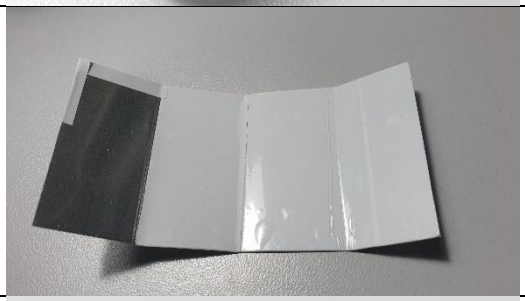
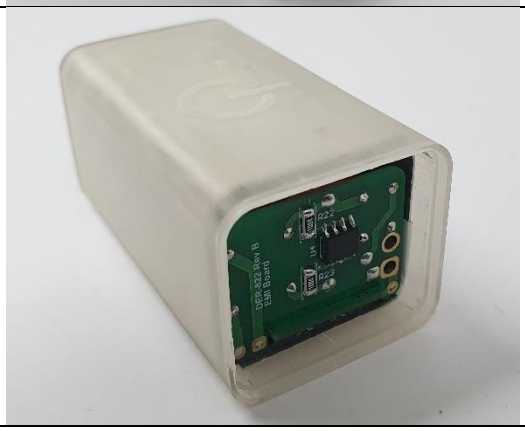
	
	Complete PCB assembly.
	Install insulator sheet on bottom to isolate secondary from the heat spreader. Align cutout with SR FET.

	Position a 50mm x 25 mm 1.5mm thick thermal pad on the bottom side of the unit.
	Prepare the heat spreader by placing tape for insulation. Refer to Figure 28 for tape location. Only one face of the heat spreader should be taped. Use two layers of 3M 1350-F, Polyester Film, 1 mil Thickness, 18.2 mm Width. Tape width greater than 18.2 mm can be also be used to minimize overlaps.
	Bend the heat spreader along the dashed lines indicated in Figure 28. Make sure the taped area is on the inner side (side facing the power supply unit) of the completed heat spreader. Carefully slip the unit inside the heat spreader. Ensure that the thermal pad remains in place.
	Install the PCB assembly with heat spreader inside the enclosure. The USB-C port must be flush against the enclosure front face.

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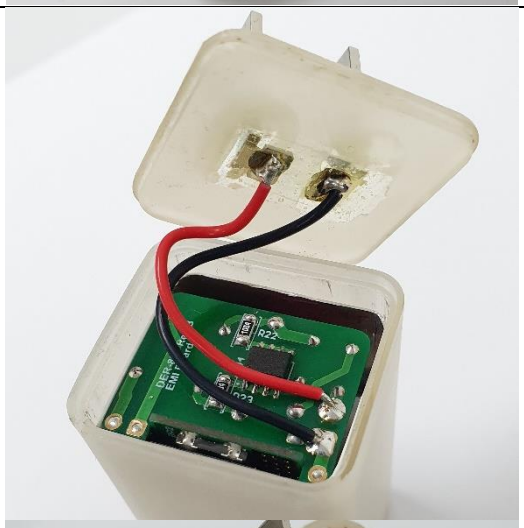 	Solder a pair of #22 AWG insulated stranded wires to the AC prongs and the input port of the unit. Insulate the prong connection.
	Close the unit enclosure by mating the cap to the enclosure body. Finished assembly.

12 Performance Data

Note: 1. Output voltage measured on the PCB unless otherwise specified.
2. Measurements taken at room temperature ambient (approximately 25 °C) unless otherwise specified.

12.1 *No-Load Input Power at 5 VOUT*

Note: 1. Unit tested without Type-C cable connected to output.
2. For each line voltage, soak time = 10 min and integration time = 5 min.

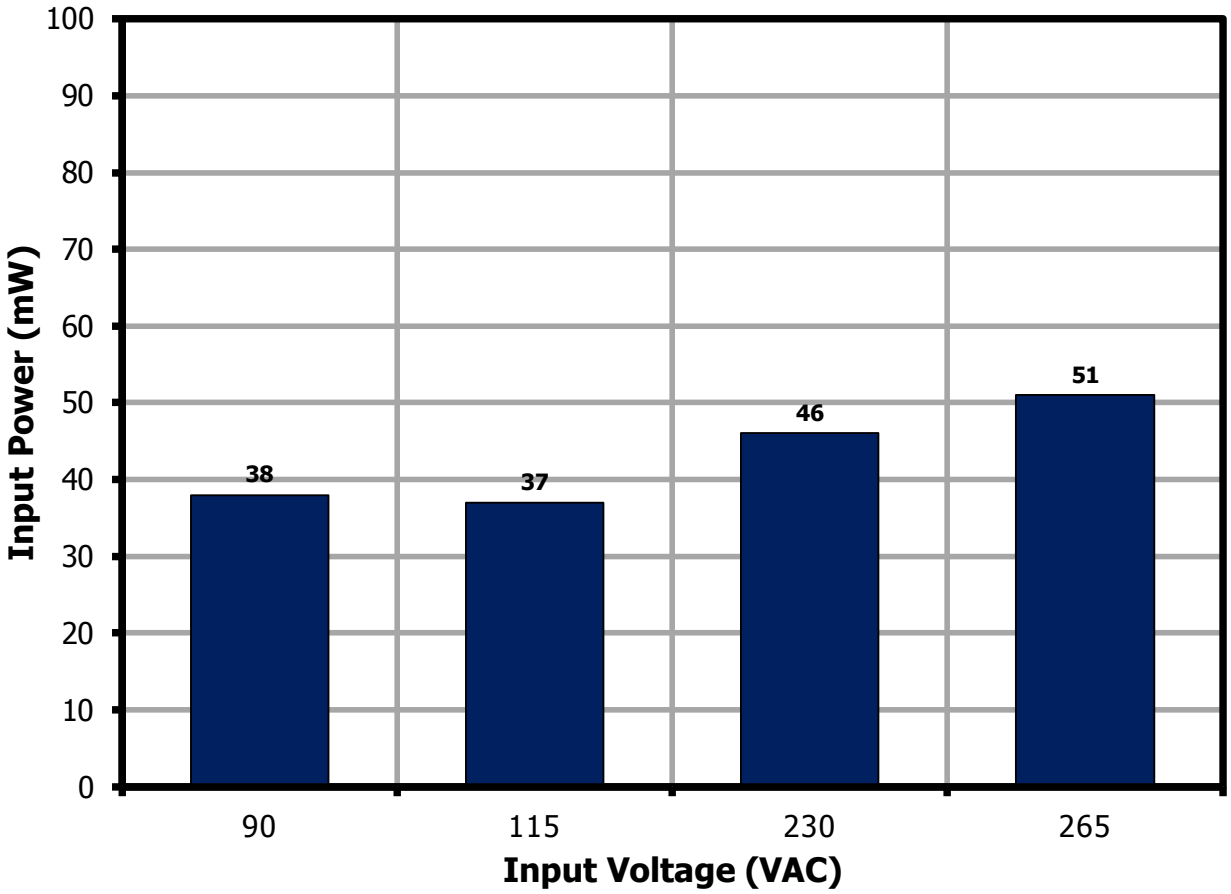

Figure 28 – No-Load Input Power vs. Input Line Voltage.

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12.2 *Full Load Efficiency*

V_{OUT} (V)	Load (A)	Power (W)	Full Load Efficiency (%)			
			90 VAC	115 VAC	230 VAC	265 VAC
5	3.0	15	91.16	91.54	91.29	90.94
9	3.0	27	91.98	92.10	92.89	92.69
15	3.0	45	91.80	92.45	93.70	93.59
20	3.0	60	90.85	91.85	93.93	93.84

12.3 *Average and 10% Load Efficiency*

12.3.1 Efficiency Requirements

		Test	Average	Average	10% Load
		Effective	2016	Jan-16	Jan-16
V_{OUT} (V)	Model (V)	Power (W)	New EISA2007	CoC v5 Tier 2	CoC v5 Tier 2
5	<6	15	81.4%	81.8%	72.5%
9	>6	27	86.6%	87.3%	77.3%
15	>6	45	87.7%	88.9%	78.9%
20	>6	60	88.0%	89.0%	79.0%

12.3.2 Efficiency Performance Summary (On Board)

V_{OUT} (V)	Power (W)	Average Efficiency (%)		10% Load Efficiency (%)	
		115 VAC	230 VAC	115 VAC	230 VAC
5	15	91.47	90.29	87.52	83.77
9	27	92.11	92.04	88.13	85.52
15	45	92.17	92.85	88.10	86.29
20	60	91.89	93.04	87.77	86.61

12.3.3 Average and 10% Load Efficiency Measurements

12.3.3.1 Output: 5 V / 3 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	14.96	91.58	**91.47**	81.4	81.8	PASS
	75	11.25	91.77				
	50	7.51	91.76				
	25	3.75	90.79				
	10	1.50	**87.52**			72.5	PASS
230	100	15.02	91.28	**90.29**	81.4	81.8	PASS
	75	11.28	91.15				
	50	7.52	90.42				
	25	3.76	88.30				
	10	1.50	**83.77**			72.5	PASS

12.3.3.2 Output: 9 V / 3 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	27.14	92.10	**92.11**	86.6%	87.3%	PASS
	75	20.40	92.14				
	50	13.62	92.55				
	25	6.81	91.66				
	10	2.73	**88.13**			77.3%	PASS
230	100	27.21	92.91	**92.04**	86.6%	87.3%	PASS
	75	20.43	92.67				
	50	13.63	92.21				
	25	6.81	90.37				
	10	2.73	**85.52**			77.3%	PASS

12.3.3.3 Output: 15 V / 3 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	45.06	92.32	**92.17**	88.0%	89.0%	PASS
	75	33.85	92.33				
	50	22.59	92.30				
	25	11.31	91.72				
	10	4.53	**88.10**			79.0%	PASS
230	100	45.17	93.72	**92.85**	88.0%	89.0%	PASS
	75	33.91	93.46				
	50	22.62	92.97				
	25	11.32	91.25				
	10	4.53	**86.29**			79.0%	PASS

12.3.3.4 Output: 20 V / 3 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	60.05	91.81	**91.89**			PASS
	75	45.10	92.30				
	50	30.10	92.12				
	25	15.06	91.32				
	10	6.03	**87.77**				PASS
230	100	60.22	93.93	**93.04**			PASS
	75	45.19	93.66				
	50	30.14	93.11				
	25	15.08	91.44				
	10	6.04	**86.61**				PASS

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12.4 *Efficiency Across Line at 100% Load (On Board)*

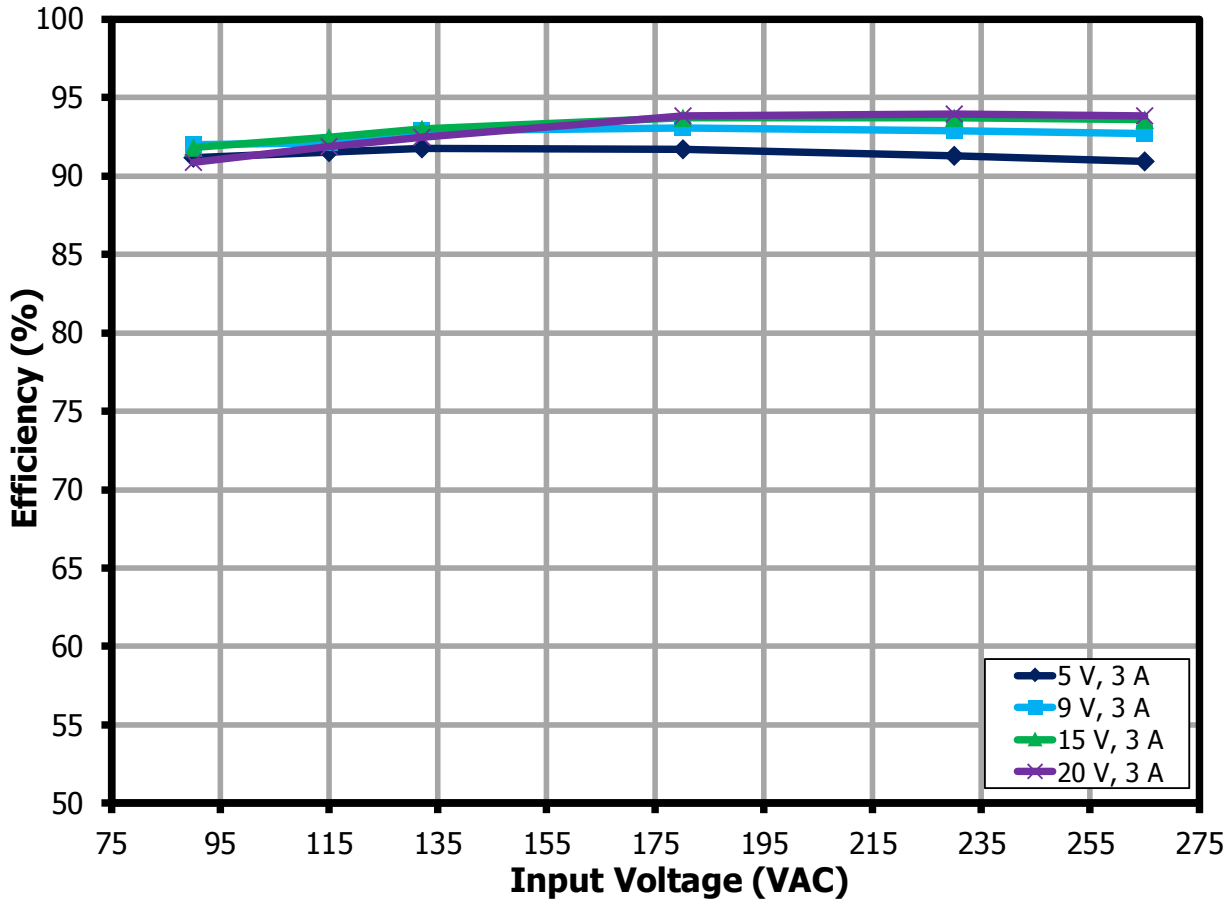

Figure 29 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 15 V, and 20 V Output, Room Temperature.

12.5 *Efficiency Across Load (On Board)*

12.5.1 Output: 5 V / 3 A

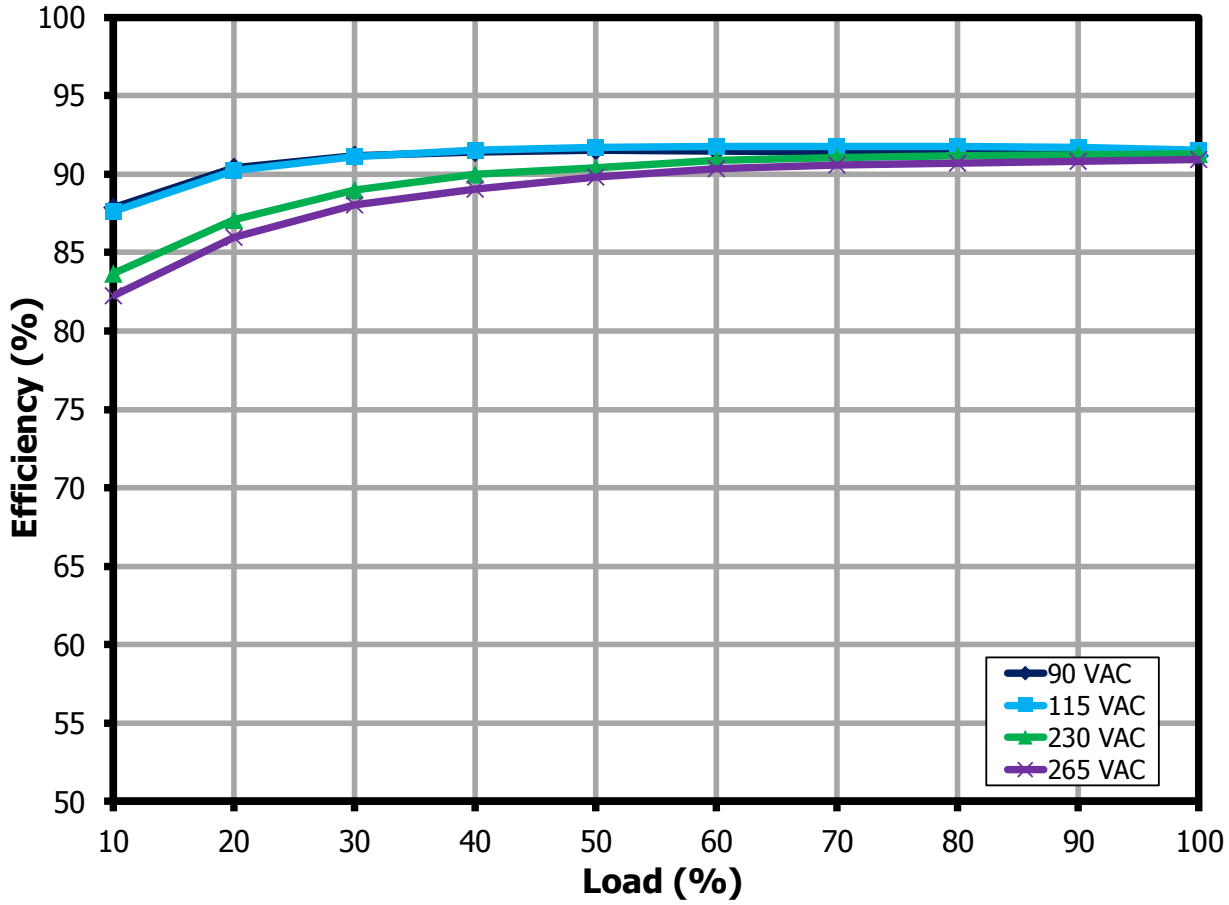

Figure 30 – Efficiency vs. Load for 5 V Output, Room Temperature.

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12.5.2 Output: 9 V / 3 A

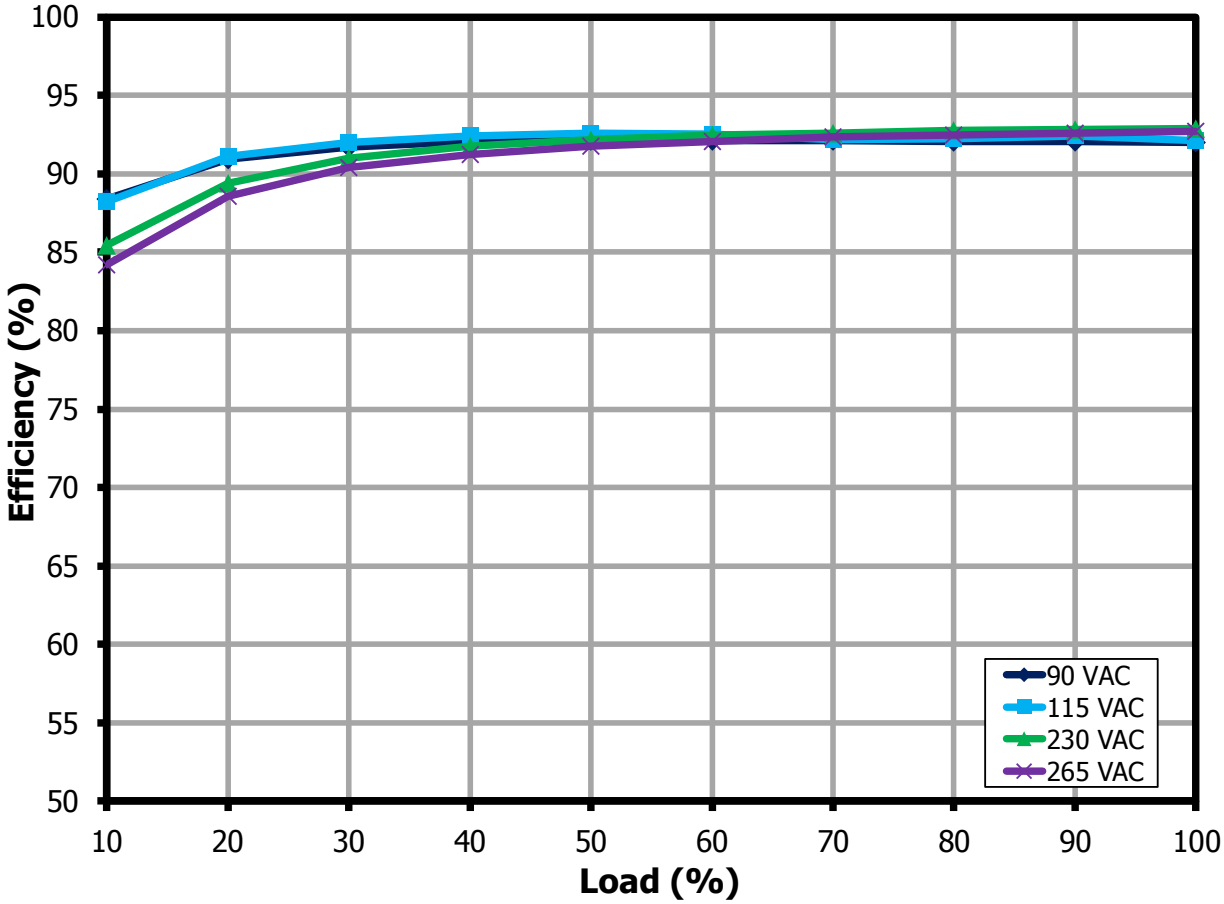

Figure 31 – Efficiency vs. Load for 9 V Output, Room Temperature.

12.5.3 Output: 15 V / 3 A

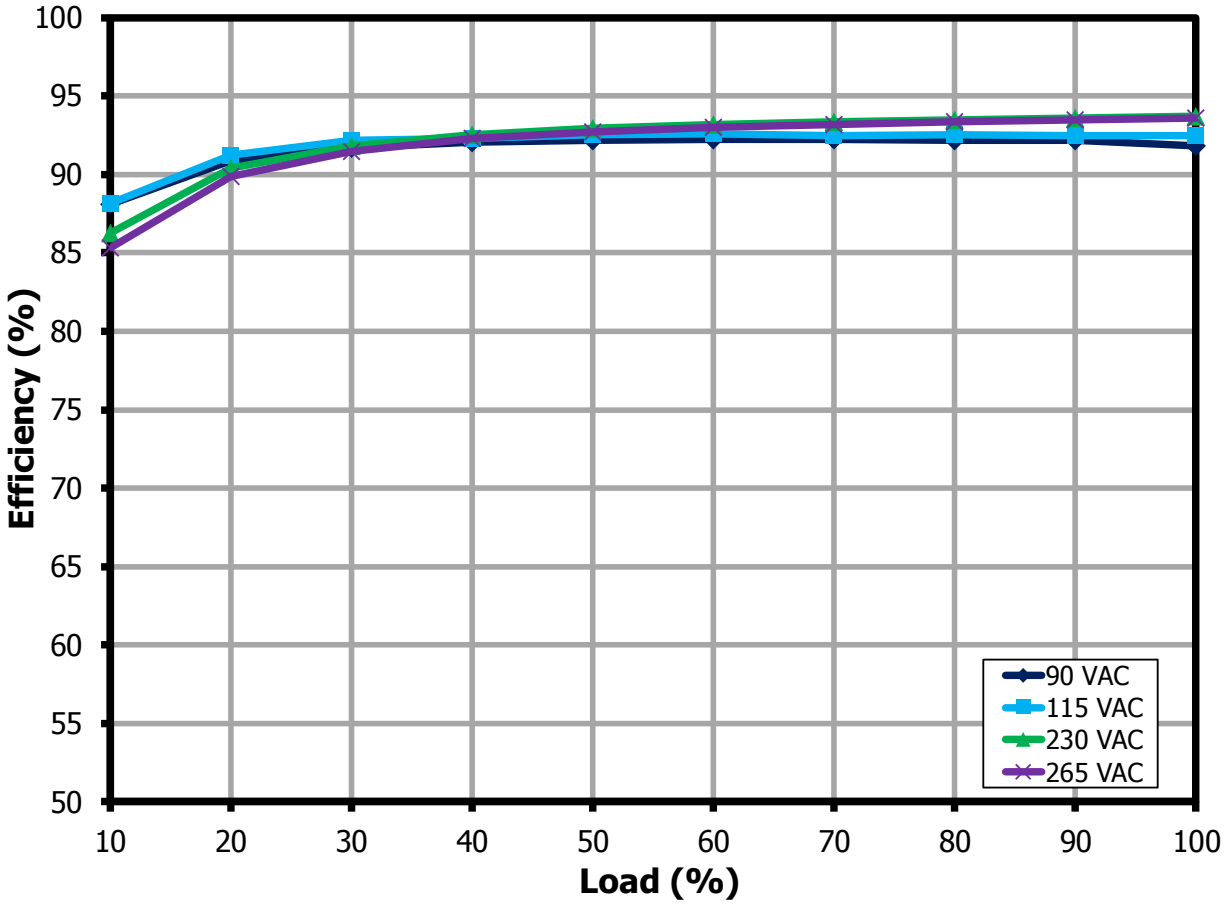

Figure 32 – Efficiency vs. Load for 15 V Output, Room Temperature.

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12.5.4 Output: 20 V / 3 A

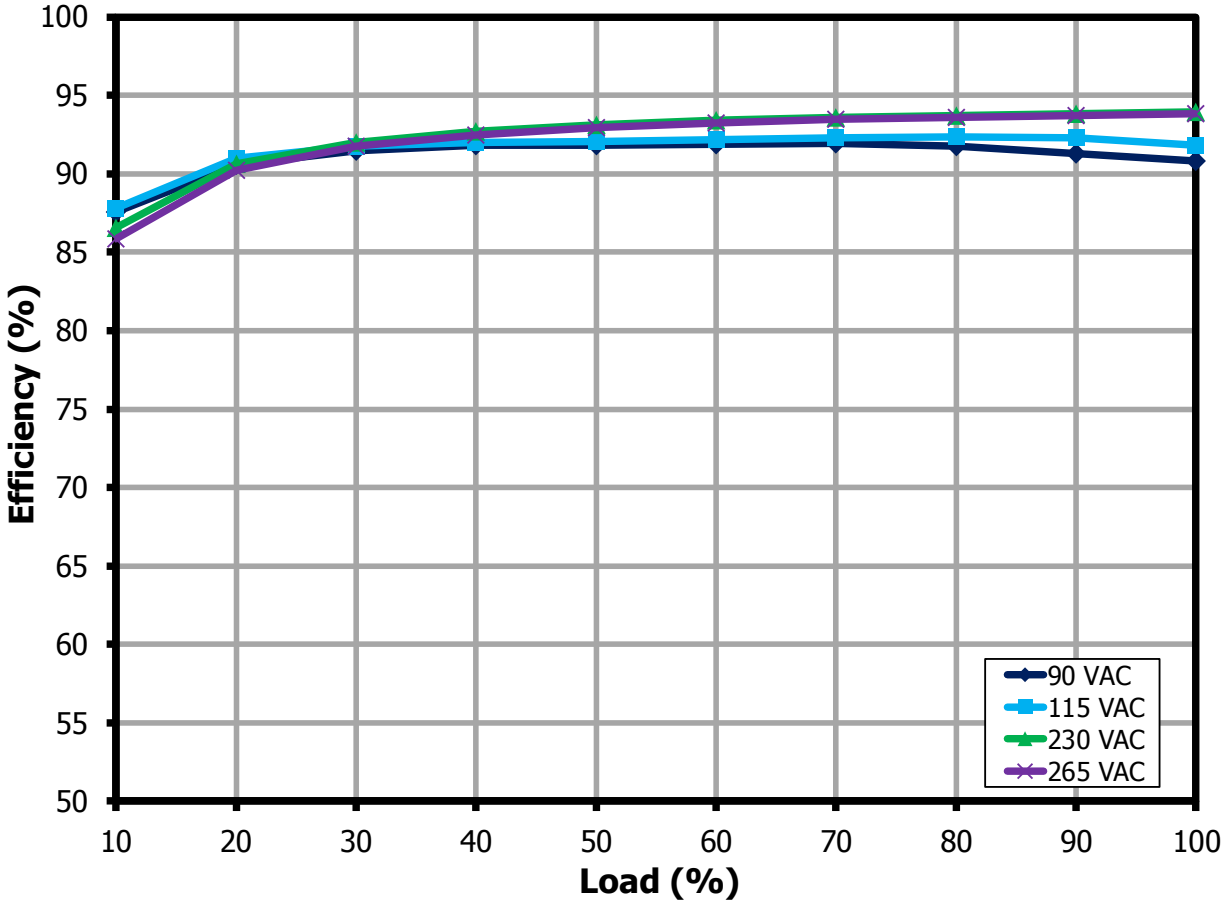

Figure 33 – Efficiency vs. Load for 20 V Output, Room Temperature.

12.6 *Load Regulation (On Board)*

12.6.1 Output: 5 V / 3 A

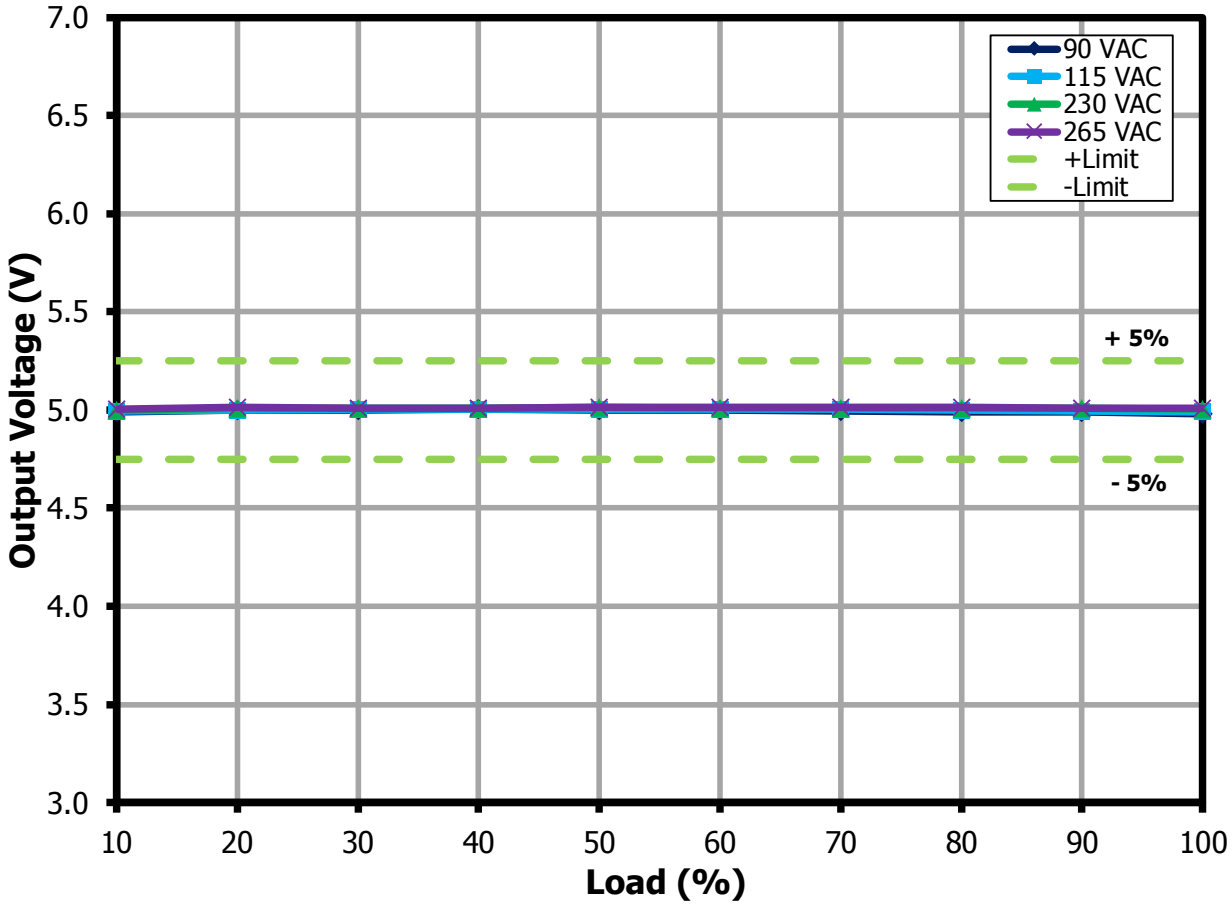

Figure 34 – Output Voltage vs. Output Load for 5 V Output, Room Temperature.

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12.6.2 Output: 9 V / 3 A

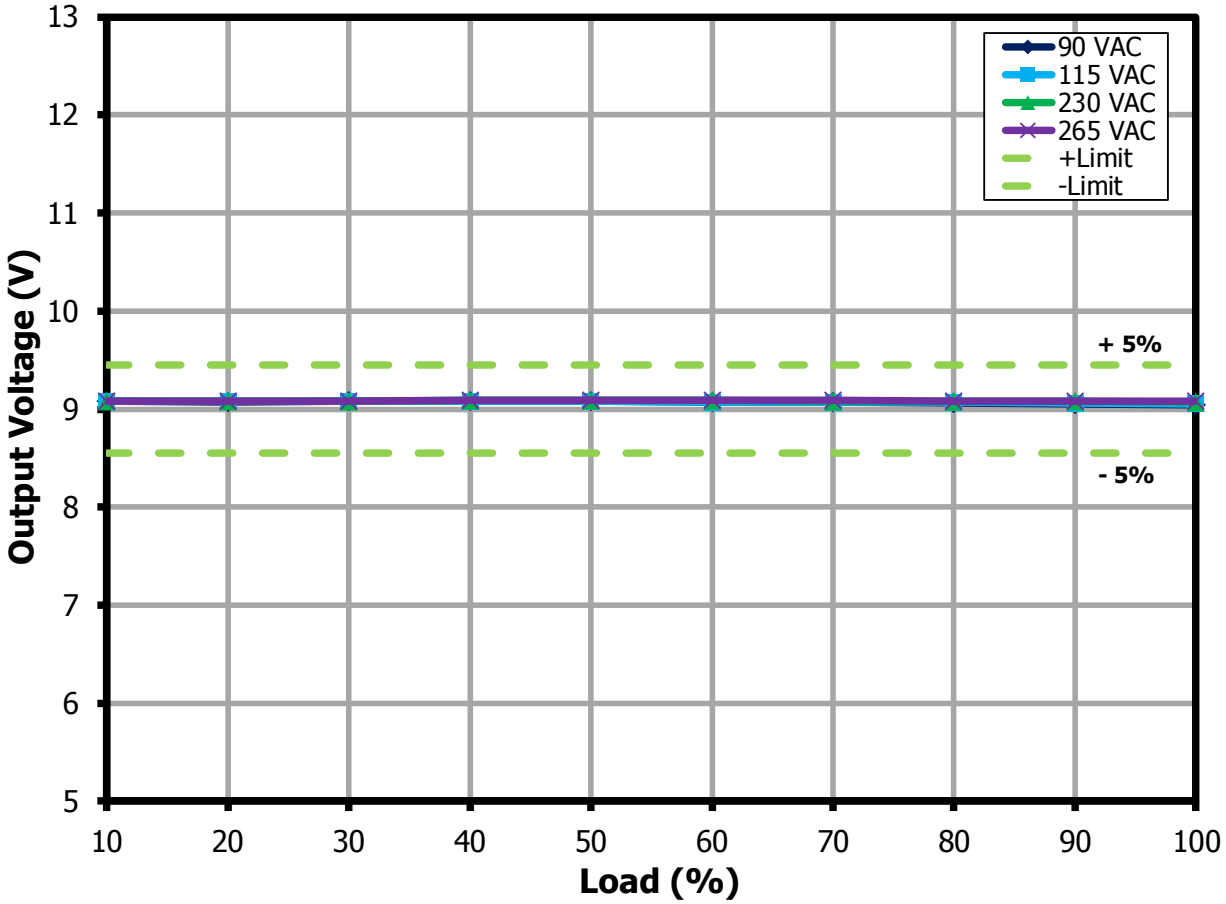

Figure 35 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.

12.6.3 Output: 15 V / 3 A

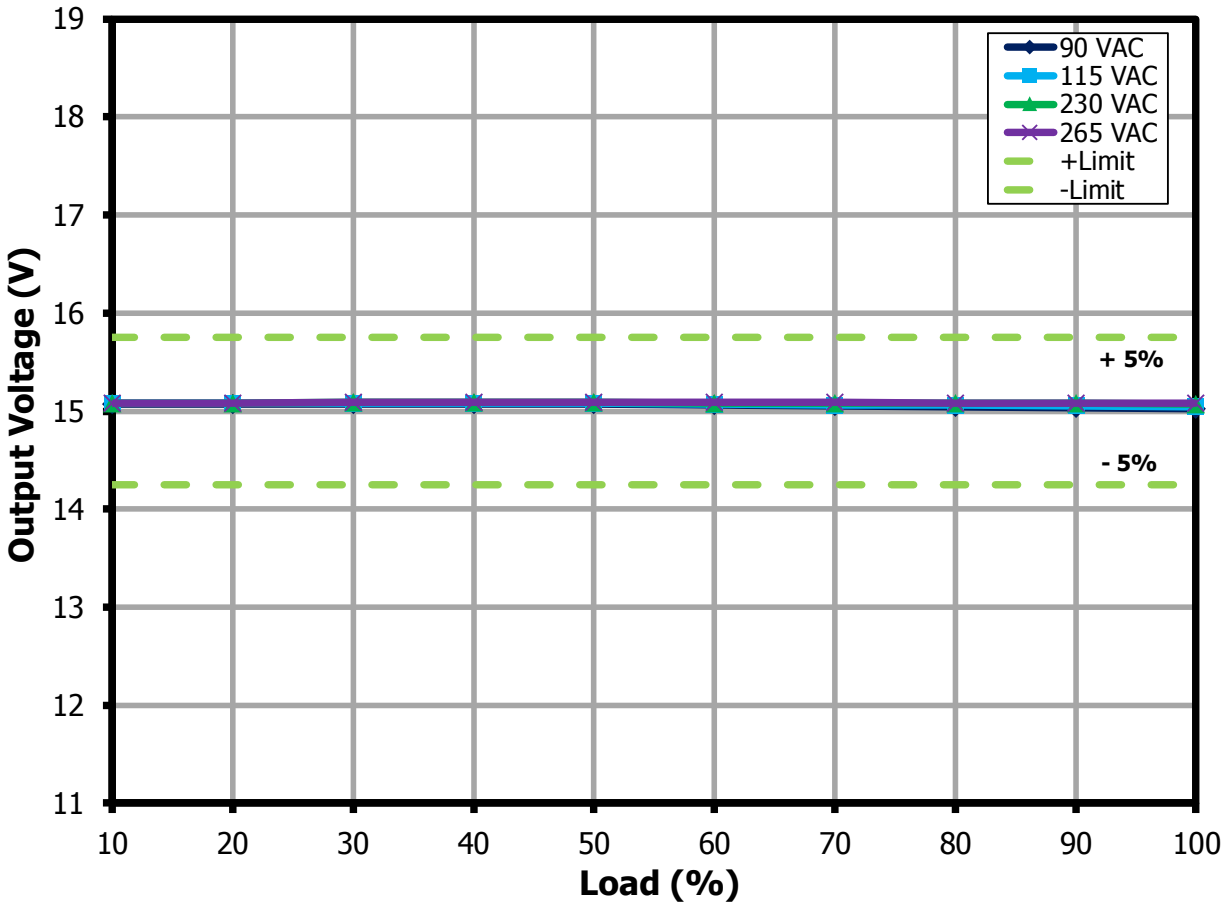

Figure 36 – Output Voltage vs. Output Load for 15 V Output, Room Temperature.

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12.6.4 Output: 20 V / 3 A

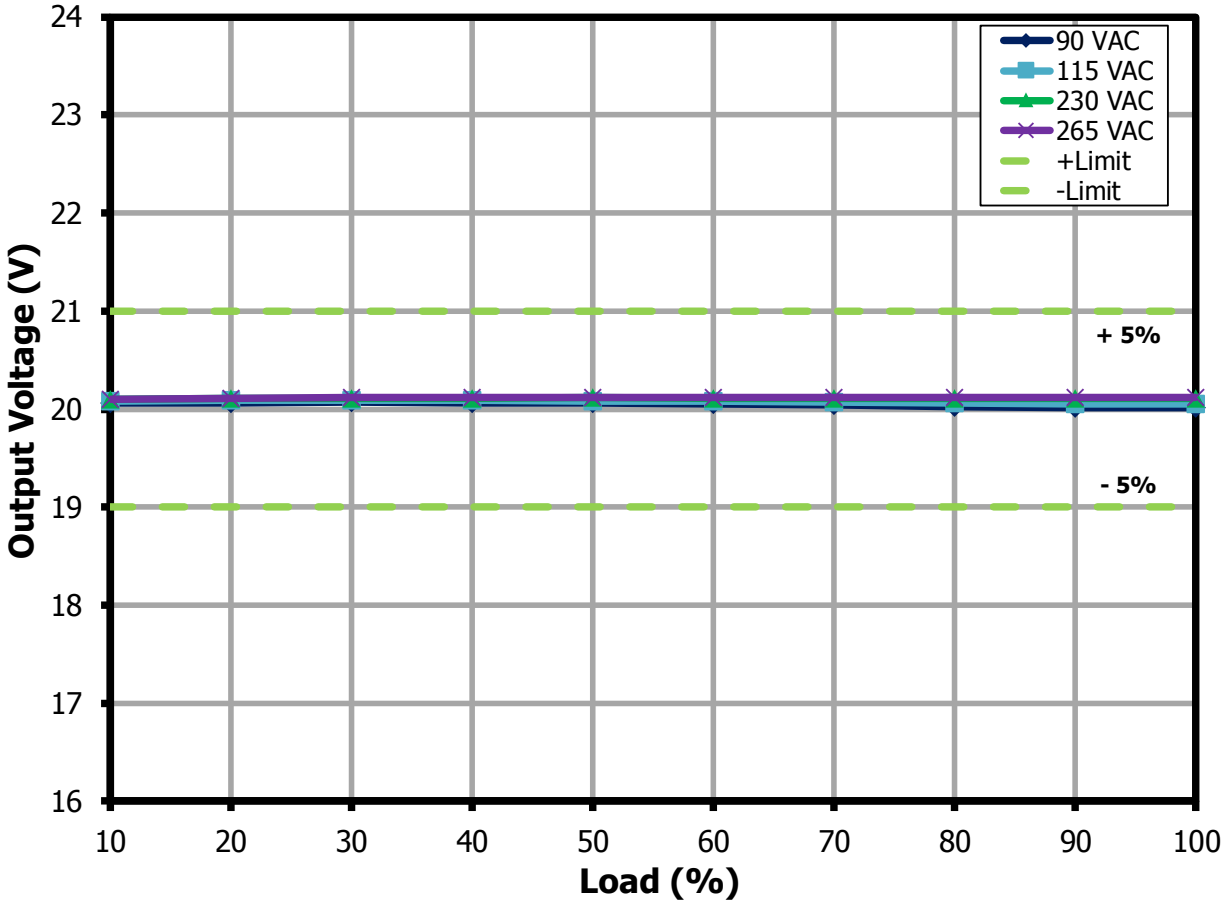

Figure 37 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.

Line Regulation (On Board)

12.6.5 Output: 5 V / 3 A

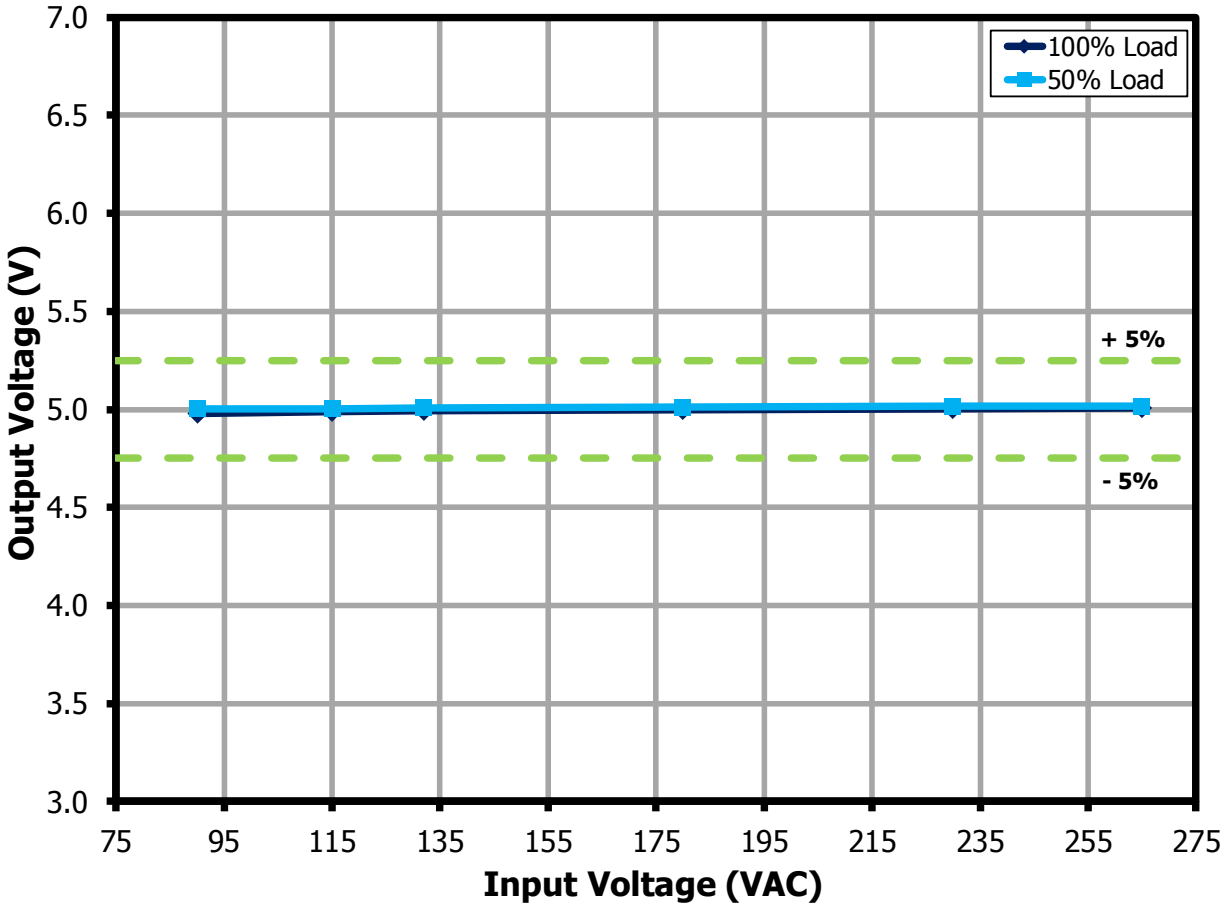

Figure 38 – Output Voltage vs. Input Line Voltage for 5 V Output, Room Temperature.

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12.6.6 Output: 9 V / 3 A

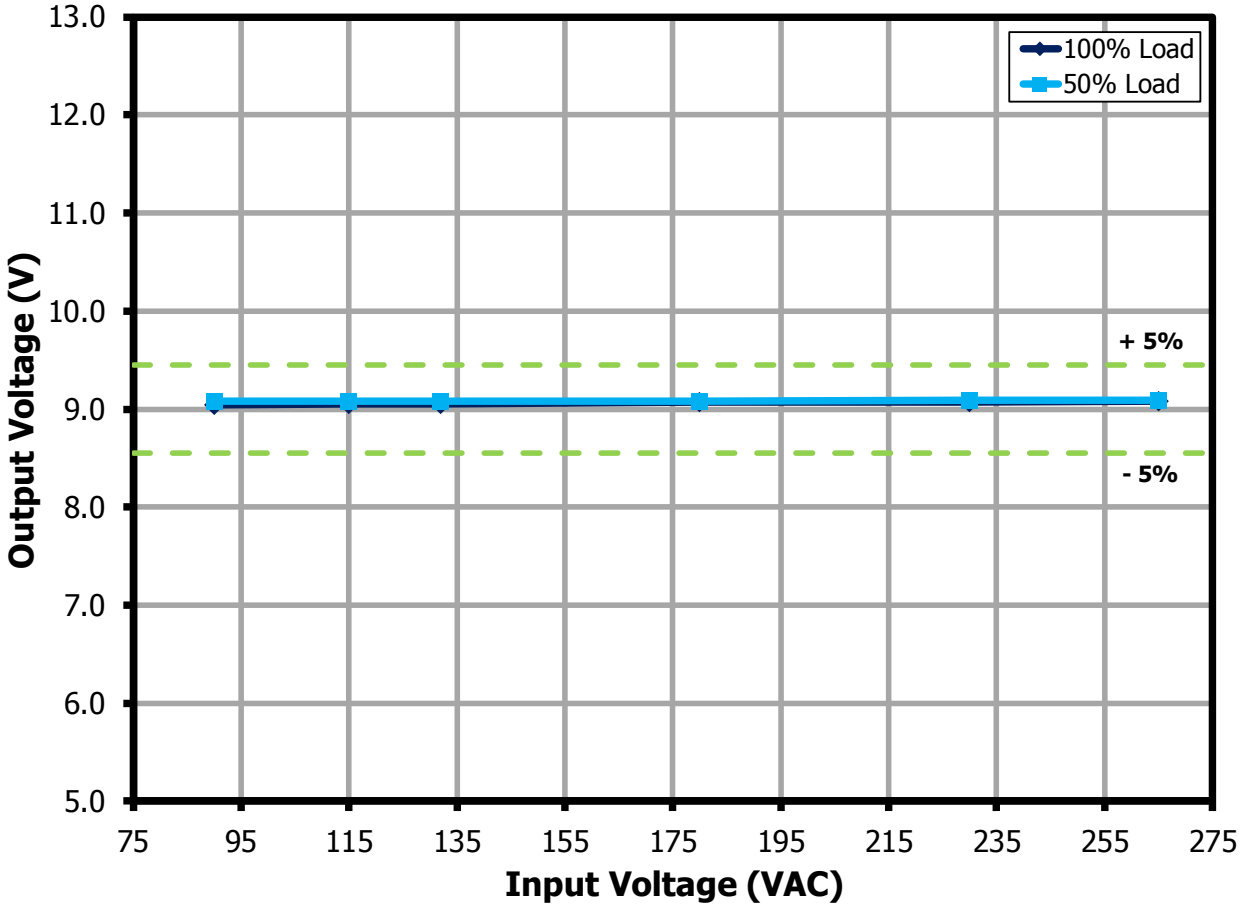

Figure 39 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.

12.6.7 Output: 15 V / 3 A

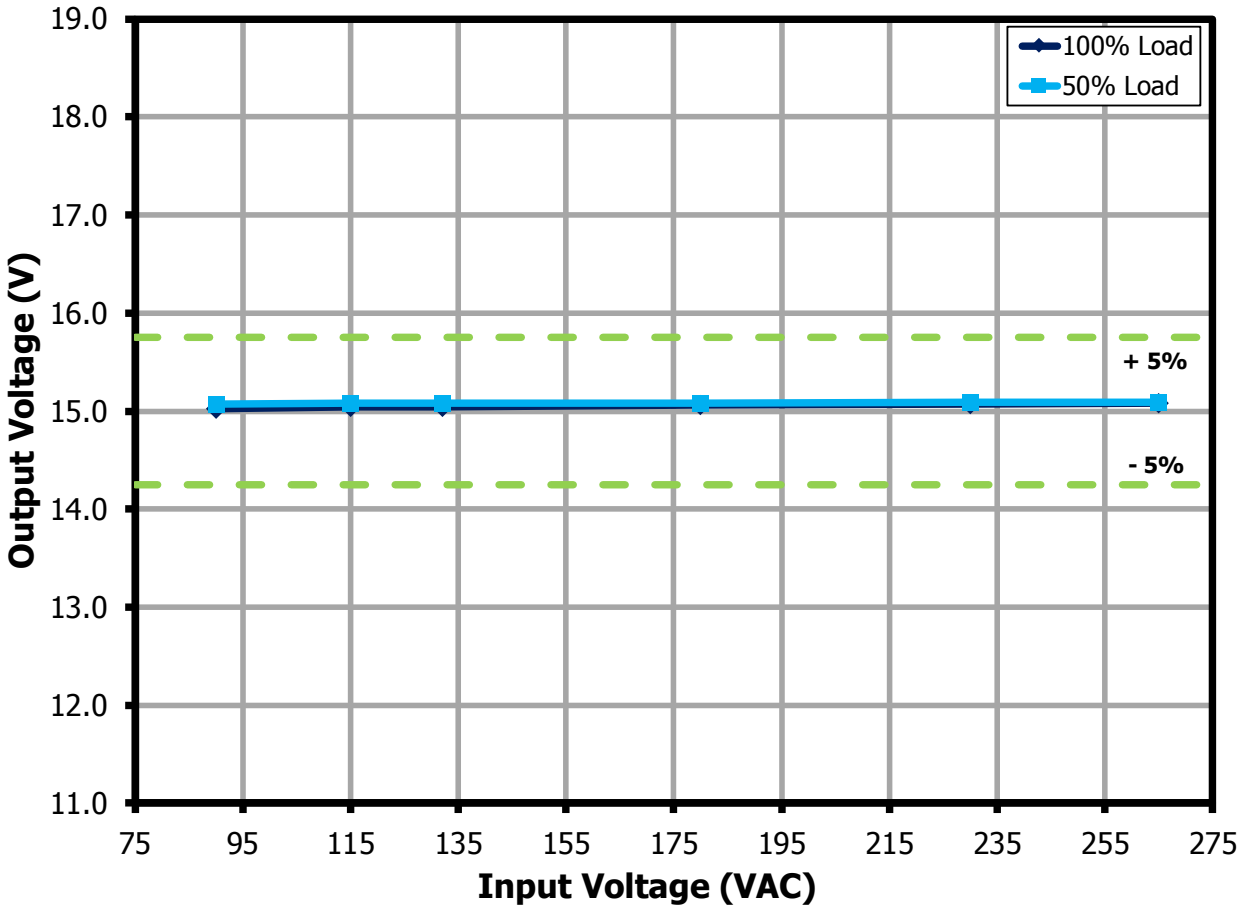

Figure 40 – Output Voltage vs. Input Line Voltage for 15 V Output, Room Temperature.

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12.6.8 Output: 20 V / 3 A

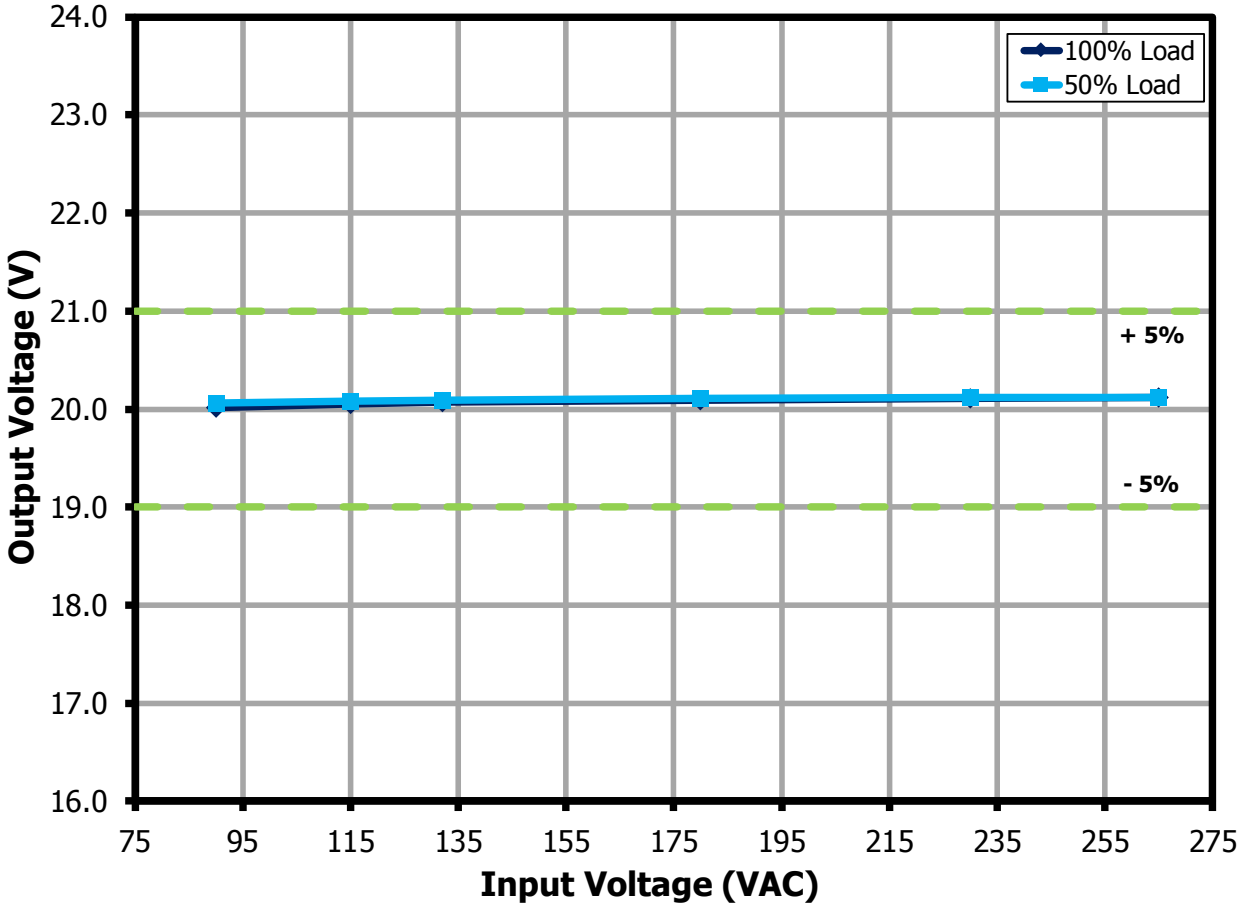

Figure 41 – Output Voltage vs. Input Line Voltage for 20 V Output, Room Temperature.

13 Thermal Performance

13.1 *Thermal Performance in Open Case, 25 ºC Ambient*

Note: Measurements taken at room temperature ambient (approximately 27.5 °C).

13.1.1 Output: 20 V / 3 A (90 VAC)

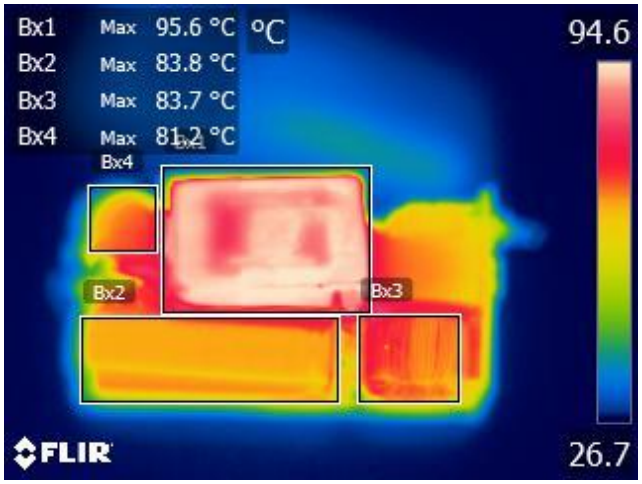

Figure 42 – Top Thermal Image.
Bx1: Transformer, T1 = 95.6 ºC.
Bx2: Input Capacitors, C2,C3 = 83.8 ºC.
Bx3: 18mH CMC, L2 = 83.7 ºC.
Bx4: Output Capacitor = 81.2 ºC.

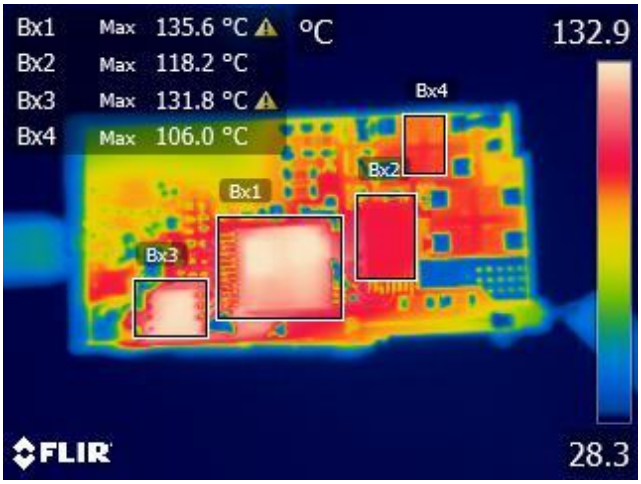

Figure 43 – Bottom Thermal Image.
Bx1: InnoSwitch3-Pro, U3 = 135.6 ºC.
Bx2: MinE-CAP, U2 = 118.2 ºC.
Bx3: SR FET = 131.8 ºC.
Bx4: Bridge Rectifier, BR1 = 106.0 ºC.

13.1.2 Output: 20 V / 3 A (265 VAC)

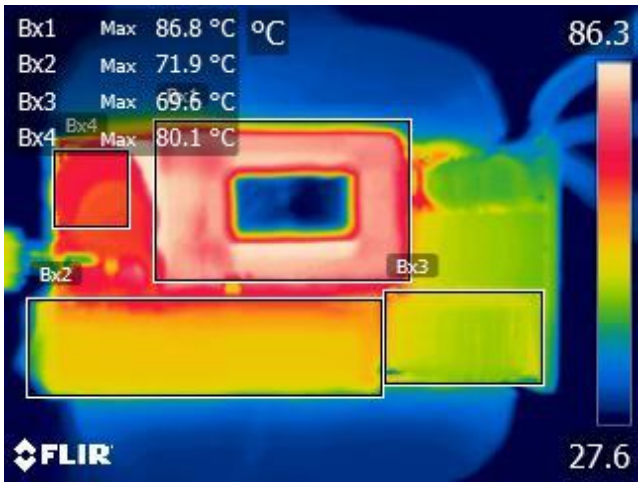

Figure 44 – Top Thermal Image.
Bx1: Transformer, T1 = 86.8 ºC.
Bx2: Input Capacitors, C2, C3 = 71.9 ºC.
Bx3: 18mH CMC, L2 = 69.6 ºC.
Bx4: Output Capacitor = 80.1 ºC.

Figure 45 – Bottom Thermal Image.
Bx1: InnoSwitch3-Pro, U3 = 111.6 ºC.
Bx2: SR FET, Q2 = 109.1 ºC.
Bx3: MinE-CAP, U2 = 81.2 ºC.
Bx4: Bridge Rectifier, BR1 = 76.1 ºC.

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13.2 *Thermal Performance with Enclosure, 40 ºC Ambient*

Note: Measurements taken using Type-T thermocouple and with the unit inside a thermal chamber.

13.2.1 Components Temperature Summary

Condition	Component	Temperature (°C)	
		20 V / 3 A (90 VAC)	20 V / 3 A (265 VAC)
Enclosed Unit 40 ºC Ambient Temperature	InnoSwitch3-Pro, U2	114.5	88
	MinE-CAP, U3	109.6	83.9
	SR FET, Q1	113.5	95.4
	Transformer, T1	106.1	89.7
	Bridge Rectifier, BR1	104.7	81.8
	Pass FET, Q2	108	90.9
	18mH CMC, L2	105.8	80.6
	LV Capacitor, C2	101.8	83.4
	HV Cap, C3	102.2	82.3
	Output Capacitor, C5	105.3	89.7
	Enclosure	82.7	69.5
	Ambient	43.3	41.6

13.2.2 Output: 20 V / 3 A (90 VAC)

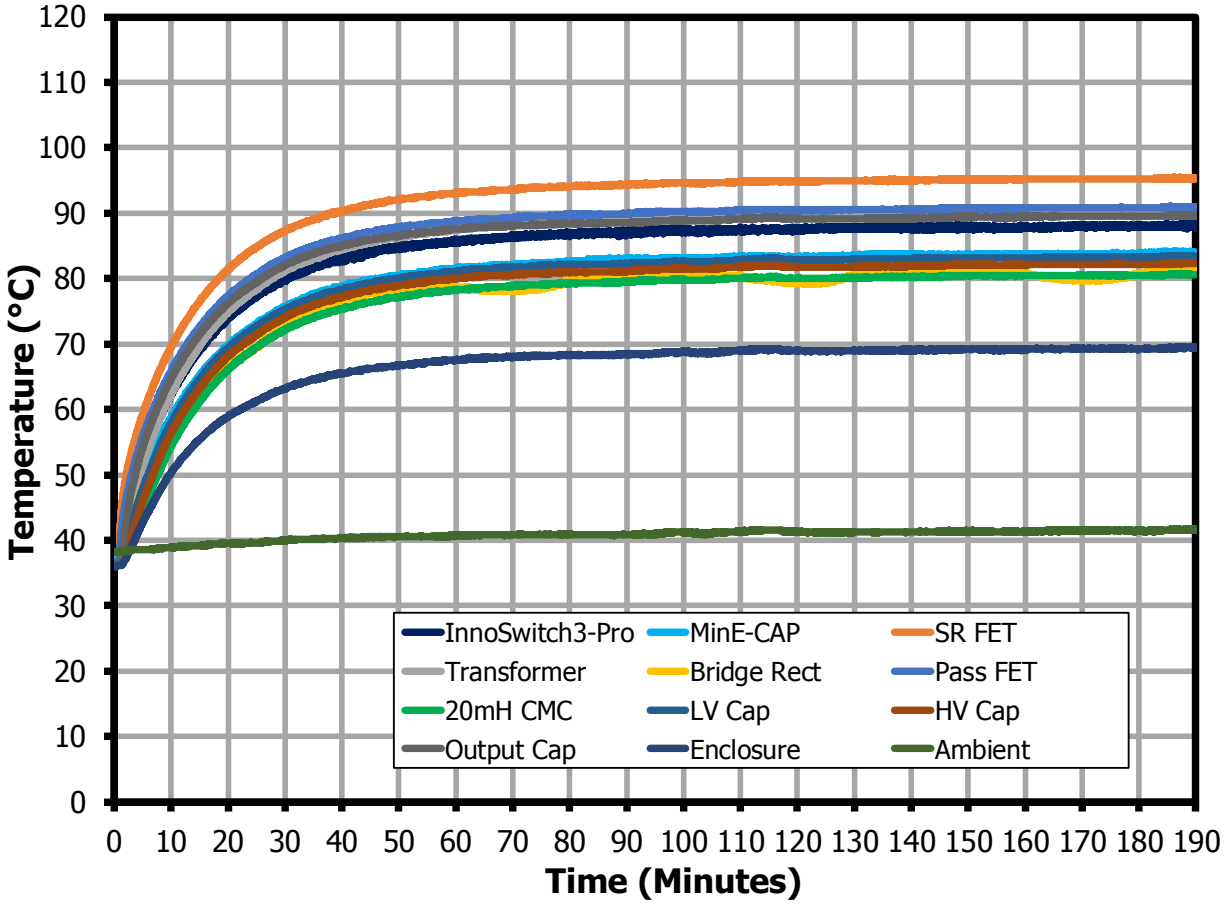

Figure 46 – Enclosed Unit Thermal Performance at 20 V / 3 A Output, 90 VAC, 40 °C Ambient.

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13.2.3 Output: 20 V / 3 A (265 VAC)

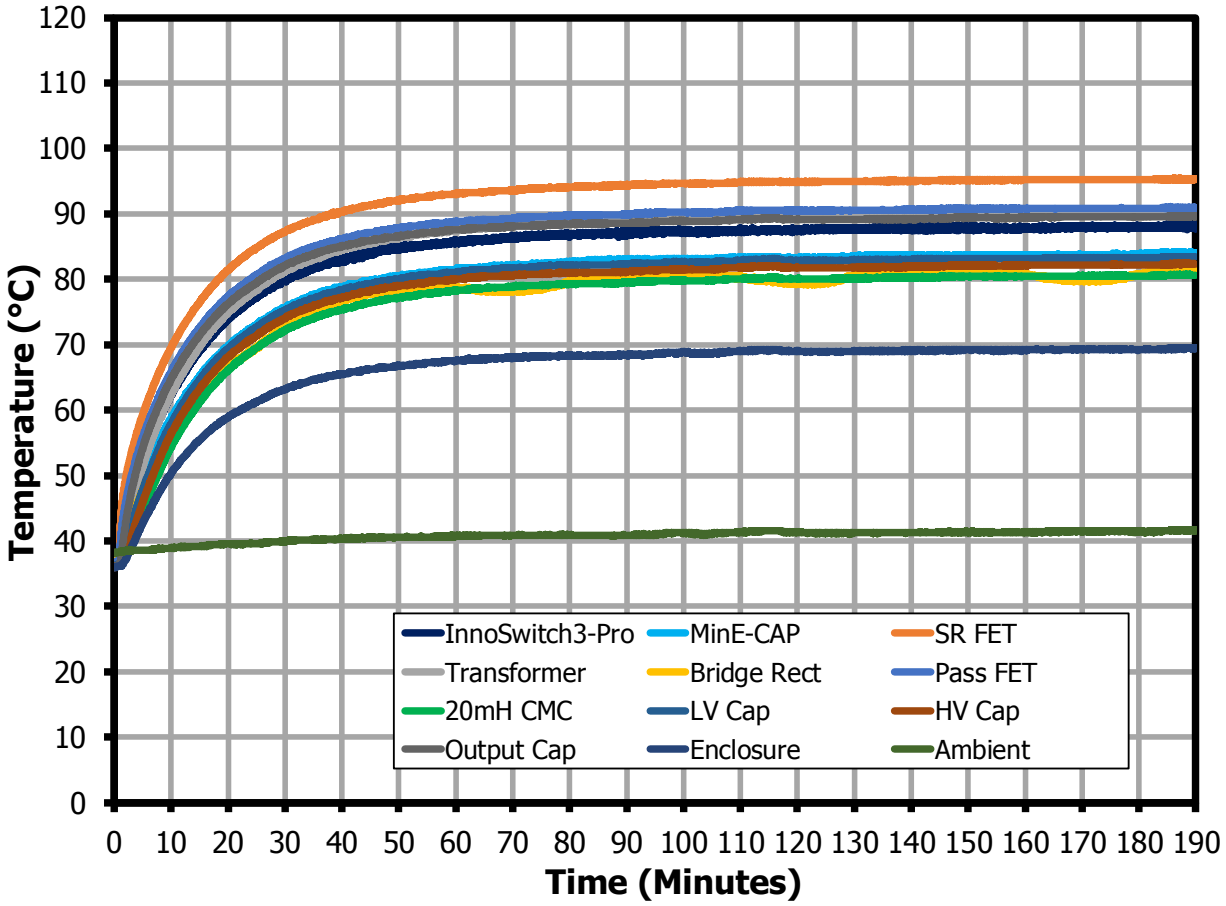

Figure 47 – Enclosed Unit Thermal Performance at 20 V / 3 A Output, 265 VAC, 40 °C Ambient.

14 Waveforms

Note: Waveforms taken at room temperature ambient (approximately 25 °C)

14.1 *Start-up Waveforms*

14.1.1 Output Voltage and Current

Note: Output voltage waveforms captured at the end of 100 mΩ cable.

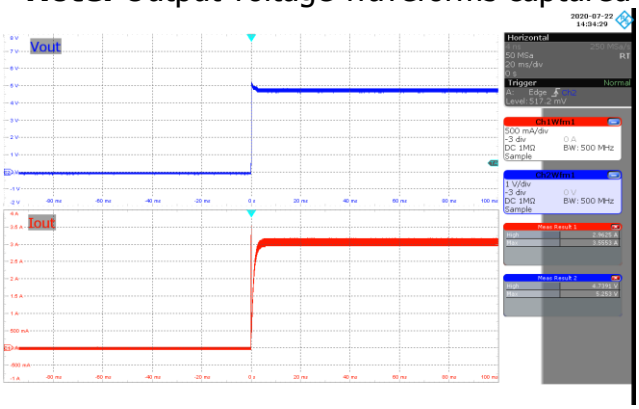

Figure 48 – Output Voltage and Current.
90 VAC, 5.0 V, 3 A Load (CR mode).
V_{OUT} = 5.253 V Maximum.
CH1: I_{LOAD}, 0.5 A / div.
CH2: V_{OUT}, 1 V / div.
Time: 20 ms / div.

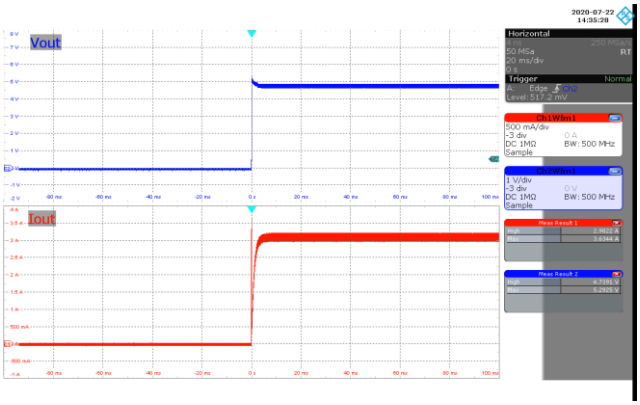

Figure 49 – Output Voltage and Current.
265 VAC, 5.0 V, 3 A Load (CR mode).
V_{OUT} = 5.293 V Maximum.
CH1: I_{LOAD}, 0.5 A / div.
CH2: V_{OUT}, 1 V / div.
Time: 20 ms / div.

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14.1.2 Primary Drain Voltage and Current

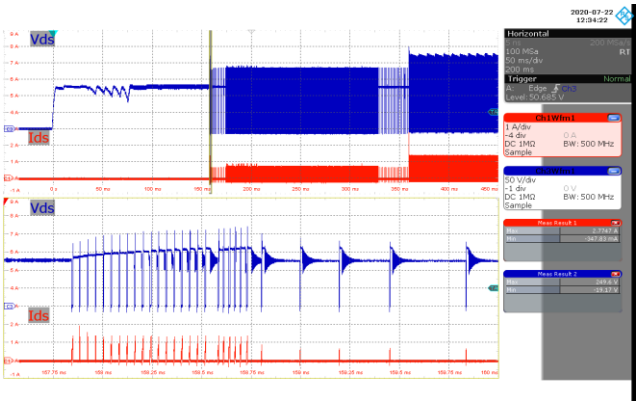

Figure 50 – Primary Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load.
V_{DS_PRI} = 249.6 V Maximum.
CH1: I_{DS_PRI}, 1 A / div.
CH3: V_{DS_PRI}, 50 V / div.
Time: 50 ms / div. (250 μs / div. Zoom)

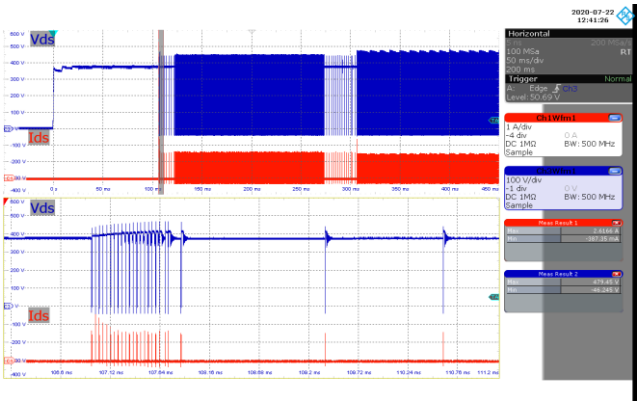

Figure 51 – Primary Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load.
V_{DS_PRI} = 479.45 V Maximum.
CH1: I_{DS_PRI}, 1 A / div.
CH3: V_{DS_PRI}, 100 V / div.
Time: 50 ms / div. (250 μs / div. Zoom)

14.1.3 SR FET Drain Voltage and Current

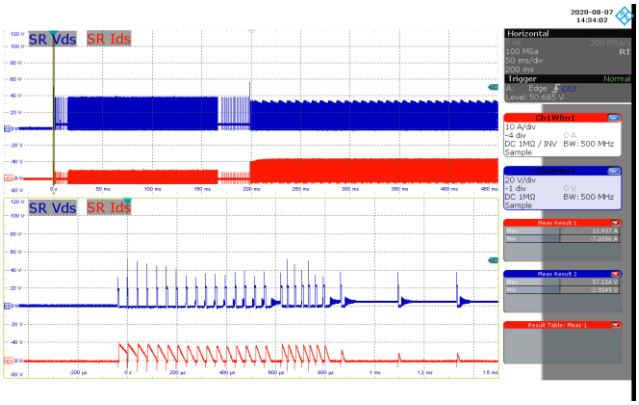

Figure 52 – SR FET Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load.
V_{DS_SRFET} = 57.154 V Maximum.
CH1: I_{DS_SRFET}, 10 A / div.
CH3: V_{DS_SRFET}, 20 V / div.
Time: 50 ms / div. (250 μs / div. Zoom)

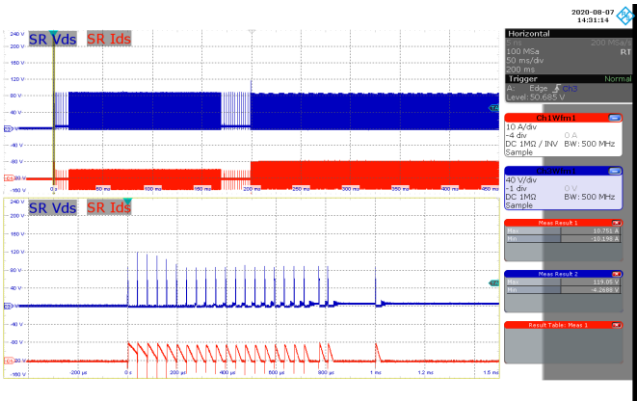

Figure 53 – SR FET Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load.
V_{DS_SRFET} = 119.05 V Maximum.
CH1: I_{DS_SRFET}, 10 A / div.
CH3: V_{DS_SRFET}, 40 V / div.
Time: 50 ms / div. (250 μs / div. Zoom)

14.1.4 MinE-CAP Startup Waveforms

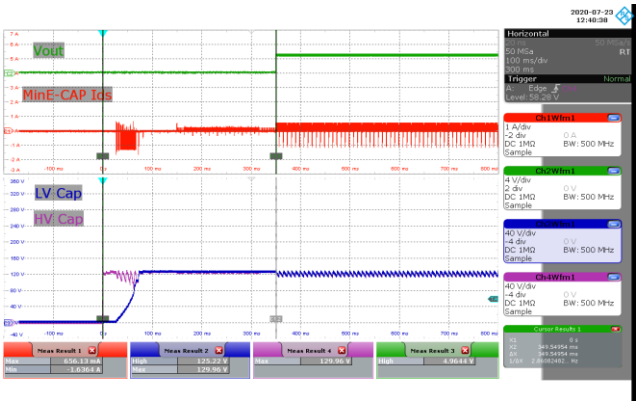

Figure 54 – MinE-CAP Waveforms.
90 VAC, 5.0 V, 3 A Load.
V_{LV_CAP} = 129.96 V Maximum.
CH1: MinE-CAP I_{DS}, 1 A / div.
CH2: V_{OUT}, 4 V / div.
CH3: V_{LV_CAP}, 40 V / div.
CH4: V_{HV_CAP}, 40 V / div.
Time: 100 ms / div.

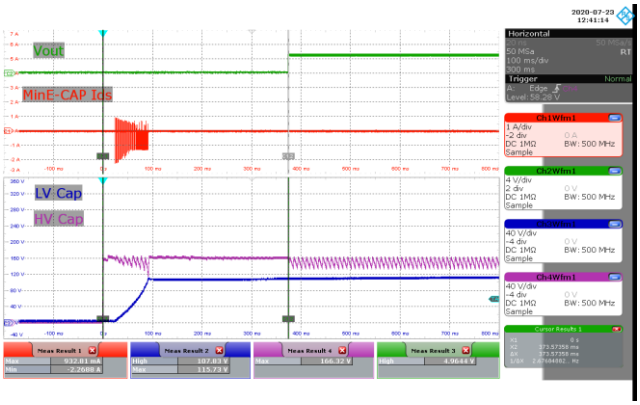

Figure 55 – MinE-CAP Waveforms.
115 VAC, 5.0 V, 3 A Load.
V_{LV_CAP} = 115.73 V Maximum.
CH1: MinE-CAP I_{DS}, 1 A / div.
CH2: V_{OUT}, 4 V / div.
CH3: V_{LV_CAP}, 40 V / div.
CH4: V_{HV_CAP}, 40 V / div.
Time: 100 ms / div.

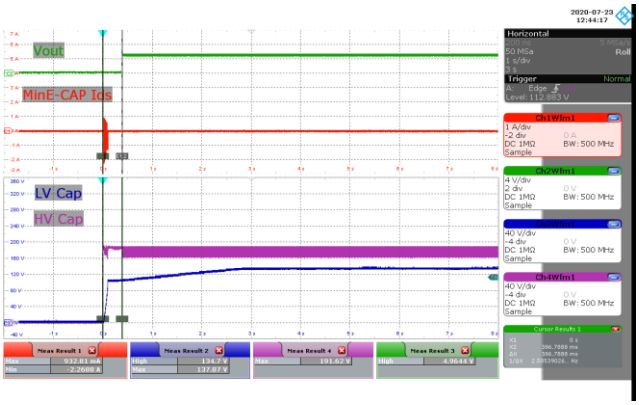

Figure 56 – MinE-CAP Waveforms.
132 VAC, 5.0 V, 3 A Load.
V_{LV_CAP} = 137.87 V Maximum.
CH1: MinE-CAP I_{DS}, 1 A / div.
CH2: V_{OUT}, 4 V / div.
CH3: V_{LV_CAP}, 40 V / div.
CH4: V_{HV_CAP}, 40 V / div.
Time: 1 s / div.

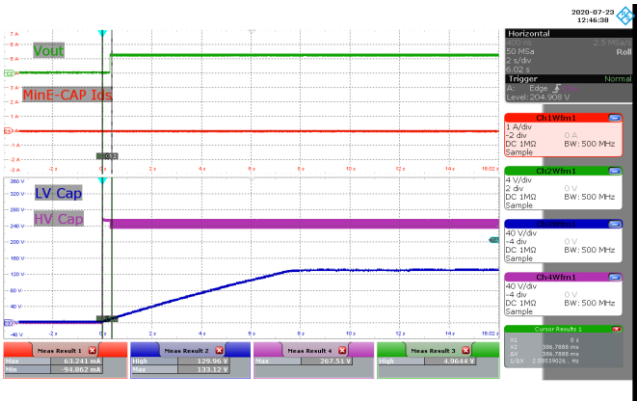

Figure 57 – MinE-CAP Waveforms.
180 VAC, 5.0 V, 3 A Load.
V_{LV_CAP} = 133.12 V Maximum.
CH1: MinE-CAP I_{DS}, 1 A / div.
CH2: V_{OUT}, 4 V / div.
CH3: V_{LV_CAP}, 40 V / div.
CH4: V_{HV_CAP}, 40 V / div.
Time: 2 s / div.

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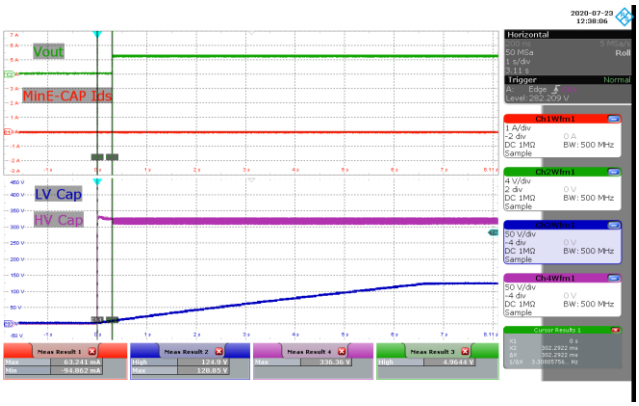

Figure 58 – MinE-CAP Waveforms.
230 VAC, 5.0 V, 3 A Load.
V_{LV_CAP} = 128.85 V Maximum.
CH1: MinE-CAP I_{DS}, 1 A / div.
CH2: V_{OUT}, 4 V / div.
CH3: V_{LV_CAP}, 40 V / div.
CH4: V_{HV_CAP}, 40 V / div.
Time: 1 s / div.

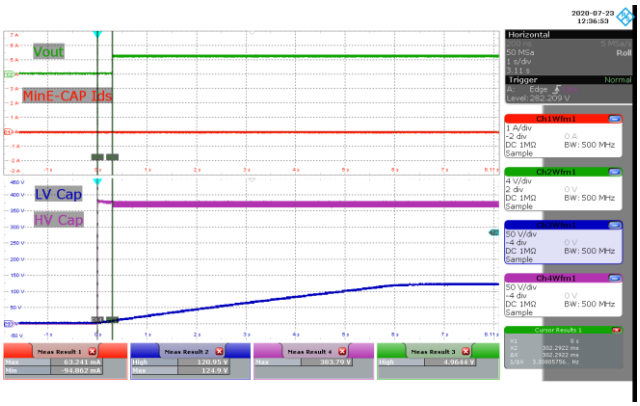

Figure 59 – MinE-CAP Waveforms.
265 VAC, 5.0 V, 3 A Load.
V_{LV_CAP} = 124.9 V Maximum.
CH1: MinE-CAP I_{DS}, 1 A / div.
CH2: V_{OUT}, 4 V / div.
CH3: V_{LV_CAP}, 40 V / div.
CH4: V_{HV_CAP}, 40 V / div.
Time: 1 s / div.

14.2 *Primary Drain Voltage and Current (Steady-State)*

14.2.1 Output: 5 V / 3 A

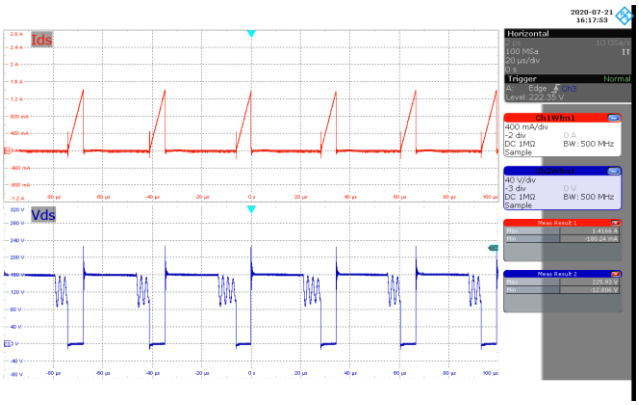

Figure 60 – Primary Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load.
V_{DS_PRI} = 225.93 V Maximum.
CH1: I_{DS_PRI}, 0.4 A / div.
CH3: V_{DS_PRI}, 40 V / div.
Time: 20 µs / div.

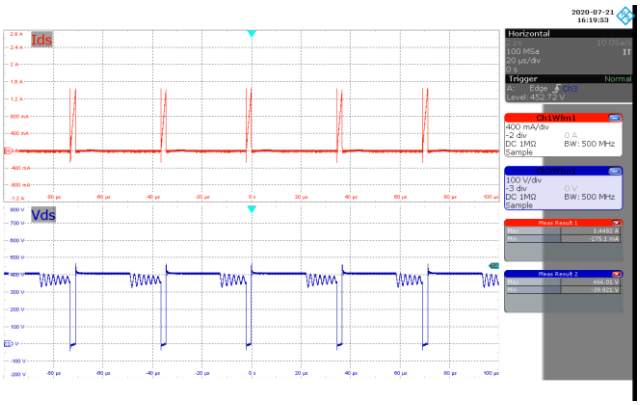

Figure 61 – Primary Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load.
V_{DS_PRI} = 466.01 V Maximum.
CH1: I_{DS_PRI}, 0.4 A / div.
CH3: V_{DS_PRI}, 100 V / div.
Time: 20 µs / div.

14.2.2 Output: 9 V / 3 A

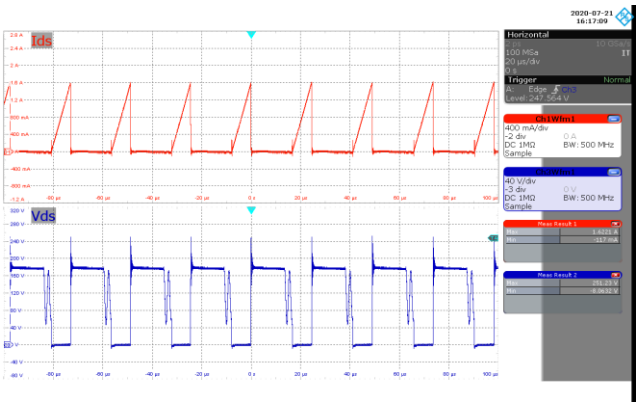

Figure 62 – Primary Drain Voltage and Current.
90 VAC, 9.0 V, 3 A Load.
V_{DS_PRI} = 251.23 V Maximum.
CH1: I_{DS_PRI}, 0.4 A / div.
CH3: V_{DS_PRI}, 40 V / div.
Time: 20 µs / div.

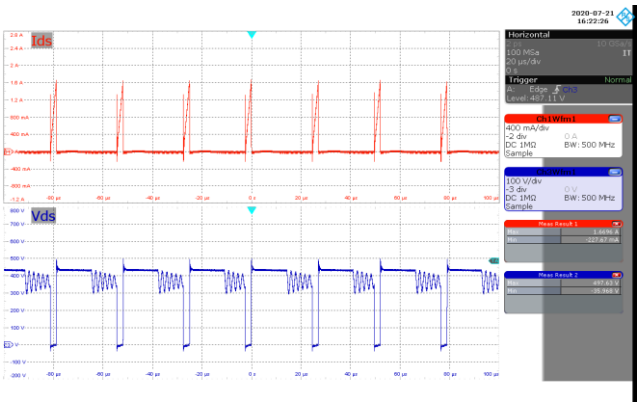

Figure 63 – Primary Drain Voltage and Current.
265 VAC, 9.0 V, 3 A Load.
V_{DS_PRI} = 497.63 V Maximum.
CH1: I_{DS_PRI}, 0.4 A / div.
CH3: V_{DS_PRI}, 100 V / div.
Time: 20 µs / div.

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14.2.3 Output: 15 V / 3 A

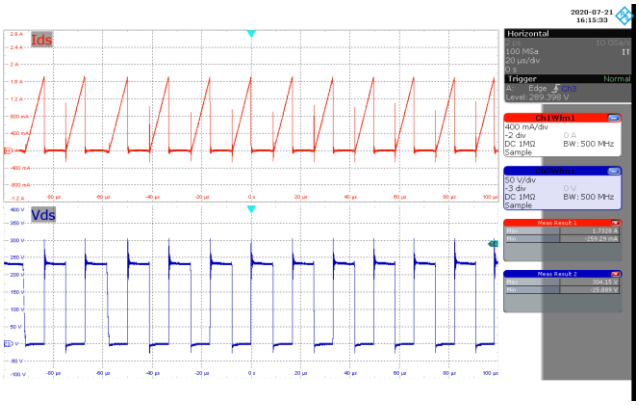

Figure 64 – Primary Drain Voltage and Current.
90 VAC, 15.0 V, 3 A Load.
V_{DS_PRI} = 304.15 V Maximum.
CH1: I_{DS_PRI}, 0.4 A / div.
CH3: V_{DS_PRI}, 50 V / div.
Time: 20 µs / div.

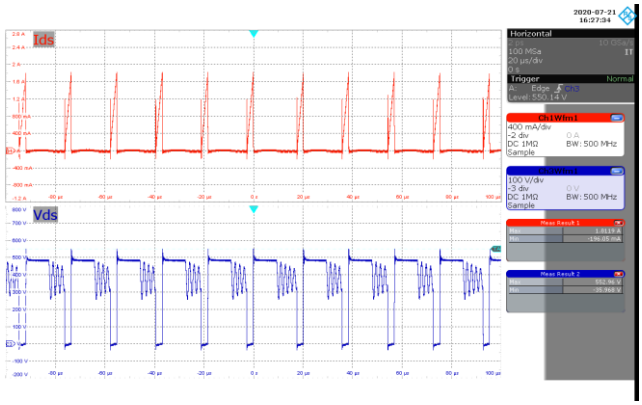

Figure 65 – Primary Drain Voltage and Current.
265 VAC, 15.0 V, 3 A Load.
V_{DS_PRI} = 552.96 V Maximum.
CH1: I_{DS_PRI}, 0.4 A / div.
CH3: V_{DS_PRI}, 100 V / div.
Time: 20 µs / div.

14.2.4 Output: 20 V / 3 A

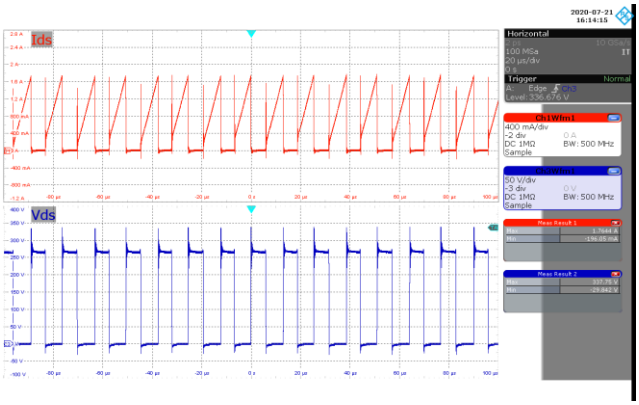

Figure 66 – Primary Drain Voltage and Current.
90 VAC, 20.0 V, 3 A Load.
V_{DS_PRI} = 337.75 V Maximum.
CH1: I_{DS_PRI}, 0.4 A / div.
CH3: V_{DS_PRI}, 50 V / div.
Time: 20 µs / div.

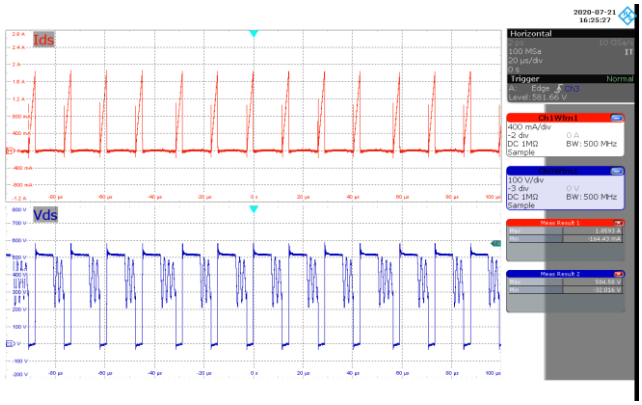

Figure 67 – Primary Drain Voltage and Current.
265 VAC, 20.0 V, 3 A Load.
V_{DS_PRI} = 584.58 V Maximum.
CH1: I_{DS_PRI}, 0.4 A / div.
CH3: V_{DS_PRI}, 100 V / div.
Time: 20 µs / div.

14.3 *SR FET Drain Voltage and Current (Steady-State)*

14.3.1 Output: 5 V / 3 A

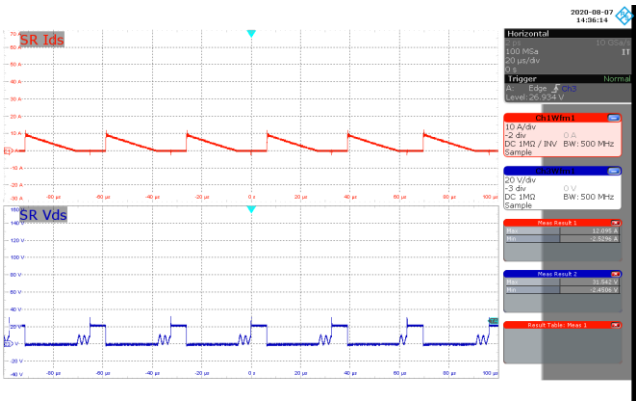

Figure 68 – SR FET Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load.
V_{DS_SRFET} = 31.542 V Maximum.
CH1: I_{DS_SRFET}, 10 A / div.
CH3: V_{DS_SRFET}, 20 V / div.
Time: 20 µs / div.

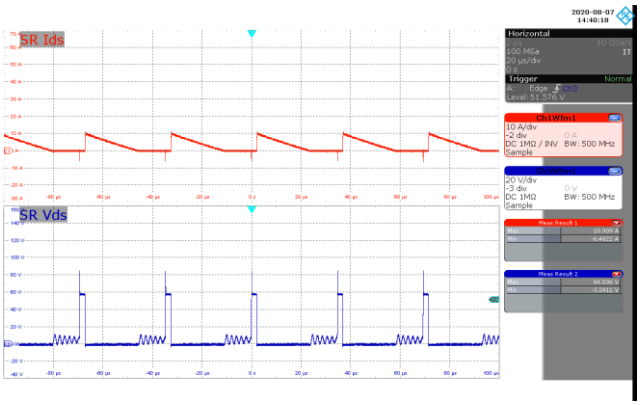

Figure 69 – SR FET Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load.
V_{DS_SRFET} = 84.506 V Maximum.
CH1: I_{DS_SRFET}, 10 A / div.
CH3: V_{DS_SRFET}, 20 V / div.
Time: 20 µs / div.

14.3.2 Output: 9 V / 3 A

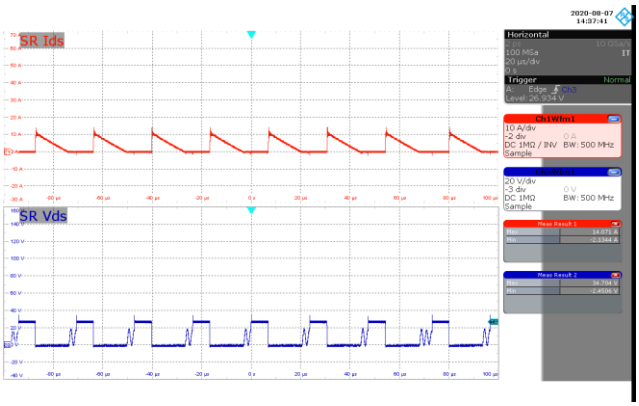

Figure 70 – SR FET Drain Voltage and Current.
90 VAC, 9.0 V, 3 A Load.
V_{DS_SRFET} = 34.704 V Maximum.
CH1: I_{DS_SRFET}, 10 A / div.
CH3: V_{DS_SRFET}, 20 V / div.
Time: 20 µs / div.

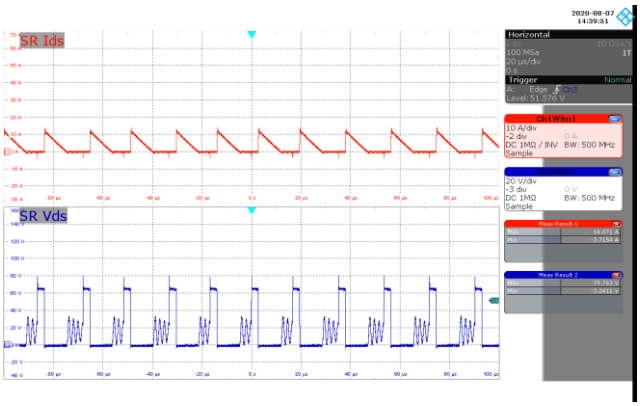

Figure 71 – SR FET Drain Voltage and Current.
265 VAC, 9.0 V, 3 A Load.
V_{DS_SRFET} = 79.763 V Maximum.
CH1: I_{DS_SRFET}, 10 A / div.
CH3: V_{DS_SRFET}, 20 V / div.
Time: 20 µs / div.

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14.3.3 Output: 15 V / 3 A

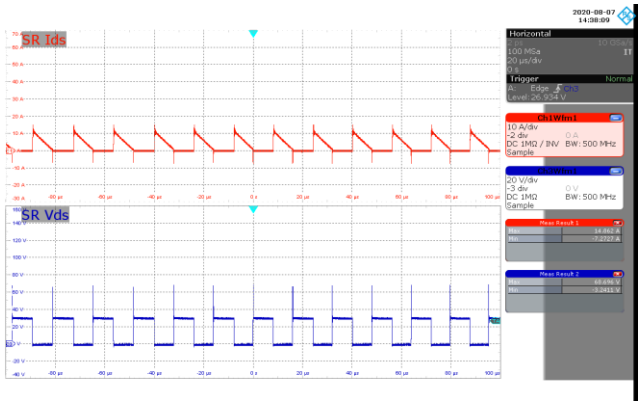

Figure 72 – SR FET Drain Voltage and Current.
90 VAC, 15.0 V, 3 A Load.
V_{DS_SRFET} = 68.696 V Maximum.
CH1: I_{DS_SRFET}, 10 A / div.
CH3: V_{DS_SRFET}, 20 V / div.
Time: 20 µs / div.

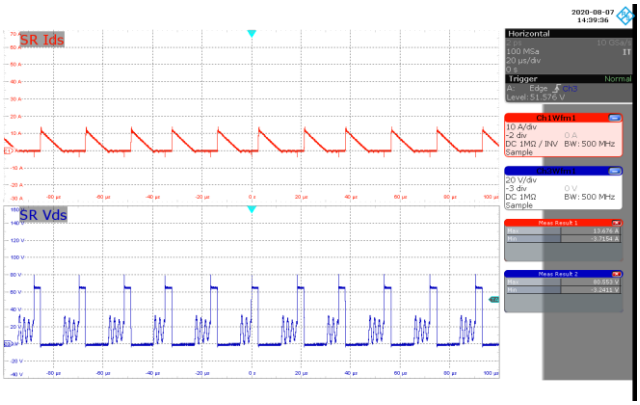

Figure 73 – SR FET Drain Voltage and Current.
265 VAC, 15.0 V, 3 A Load.
V_{DS_SRFET} = 80.553 V Maximum.
CH1: I_{DS_SRFET}, 10 A / div.
CH3: V_{DS_SRFET}, 20 V / div.
Time: 20 µs / div.

14.3.4 Output: 20 V / 3 A

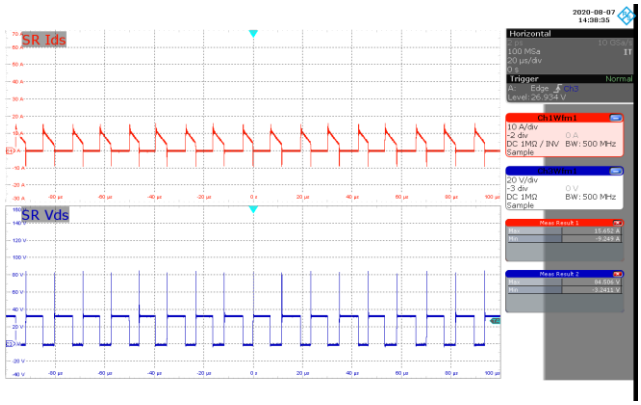

Figure 74 – SR FET Drain Voltage and Current.
90 VAC, 20.0 V, 3 A Load.
V_{DS_SRFET} = 84.506 V Maximum.
CH1: I_{DS_SRFET}, 10 A / div.
CH3: V_{DS_SRFET}, 20 V / div.
Time: 20 µs / div.

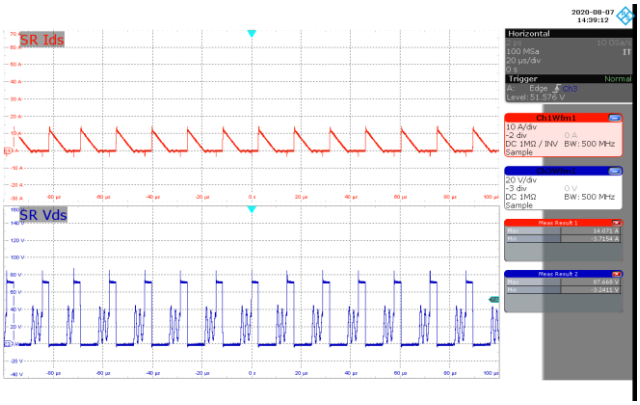

Figure 75 – SR FET Drain Voltage and Current.
265 VAC, 20.0 V, 3 A Load.
V_{DS_SRFET} = 87.668 V Maximum.
CH1: I_{DS_SRFET}, 10 A / div.
CH3: V_{DS_SRFET}, 20 V / div.
Time: 20 µs / div.

14.4 *MinE-CAP Waveforms at Steady-State*

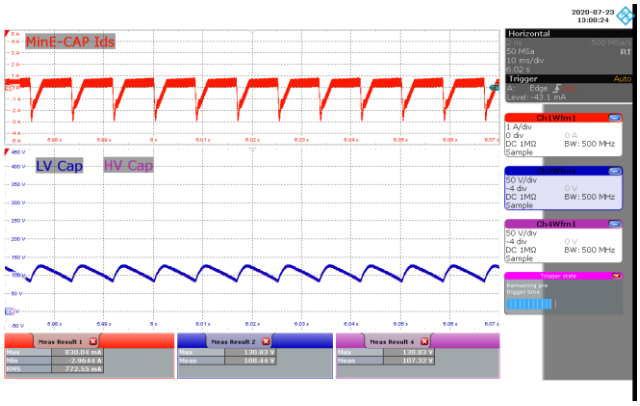

Figure 76 – MinE-CAP Waveforms.
90 VAC, 20.0 V, 3 A Load.
V_{LV_CAP} = 130.83 V Maximum.
CH1: MinE-CAP I_{DS}, 1 A / div.
CH3: V_{LV_CAP}, 50 V / div.
CH4: V_{HV_CAP}, 50 V / div.
Time: 10 ms / div.

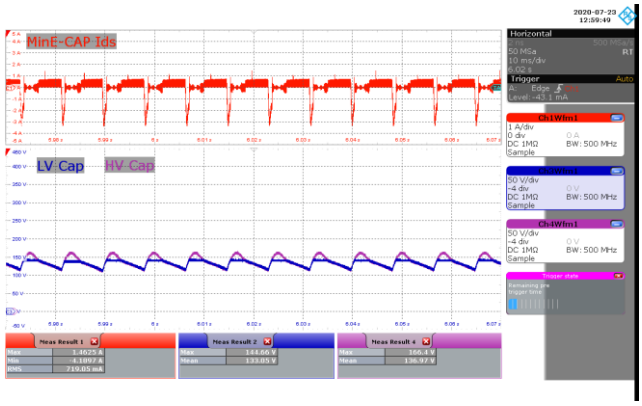

Figure 77 – MinE-CAP Waveforms.
115 VAC, 20.0 V, 3 A Load.
V_{LV_CAP} = 144.66 V Maximum.
CH1: MinE-CAP I_{DS}, 1 A / div.
CH3: V_{LV_CAP}, 50 V / div.
CH4: V_{HV_CAP}, 50 V / div.
Time: 10 ms / div.

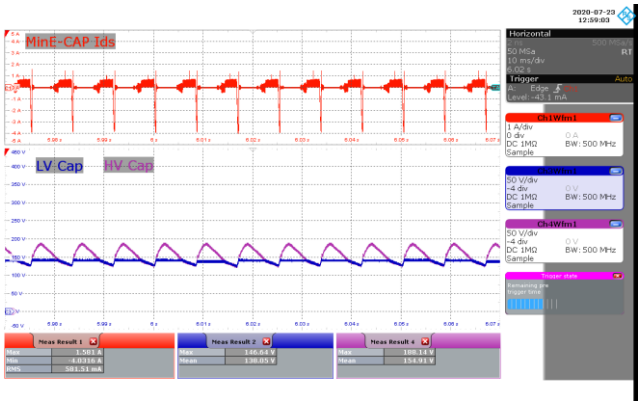

Figure 78 – MinE-CAP Waveforms.
132 VAC, 20.0 V, 3 A Load.
V_{LV_CAP} = 146.64 V Maximum.
CH1: MinE-CAP I_{DS}, 1 A / div.
CH3: V_{LV_CAP}, 50 V / div.
CH4: V_{HV_CAP}, 50 V / div.
Time: 10 ms / div.

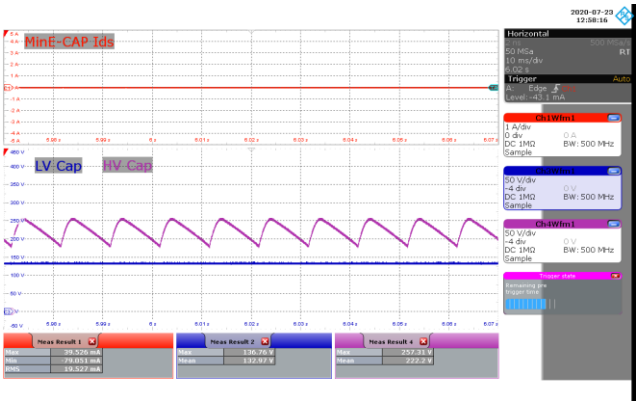

Figure 79 – MinE-CAP Waveforms.
180 VAC, 20.0 V, 3 A Load.
V_{LV_CAP} = 136.76 V Maximum.
CH1: MinE-CAP I_{DS}, 1 A / div.
CH3: V_{LV_CAP}, 50 V / div.
CH4: V_{HV_CAP}, 50 V / div.
Time: 10 ms / div.

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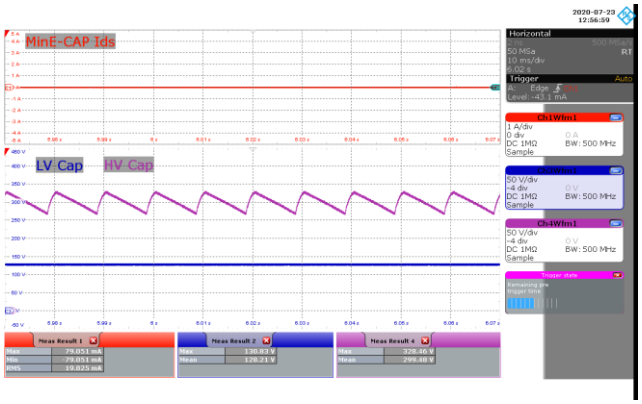

Figure 80 – MinE-CAP Waveforms.
230 VAC, 20.0 V, 3 A Load.
V_{LV_CAP} = 130.83 V Maximum.
CH1: MinE-CAP I_{DS}, 1 A / div.
CH3: V_{LV_CAP}, 50 V / div.
CH4: V_{HV_CAP}, 50 V / div.
Time: 10 ms / div.

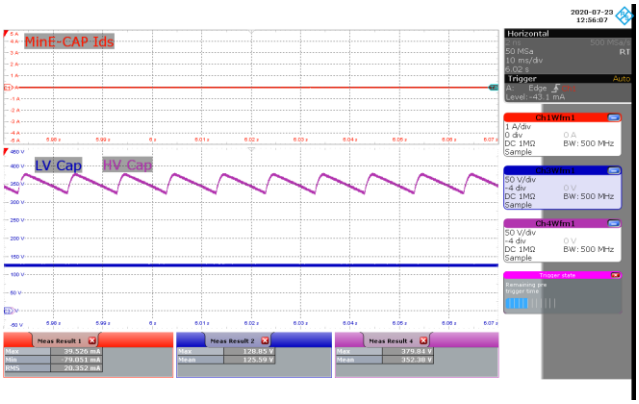

Figure 81 – MinE-CAP Waveforms.
265 VAC, 20.0 V, 3 A Load.
V_{LV_CAP} = 128.85 V Maximum.
CH1: MinE-CAP I_{DS}, 1 A / div.
CH3: V_{LV_CAP}, 50 V / div.
CH4: V_{HV_CAP}, 50 V / div.
Time: 10 ms / div.

14.5 *Primary and SR FET Drain Voltage and Current (during Output Voltage Transition)*

14.5.1 Primary Drain Voltage and Current, 3.3 V to 21 V Transition / 3 A Load

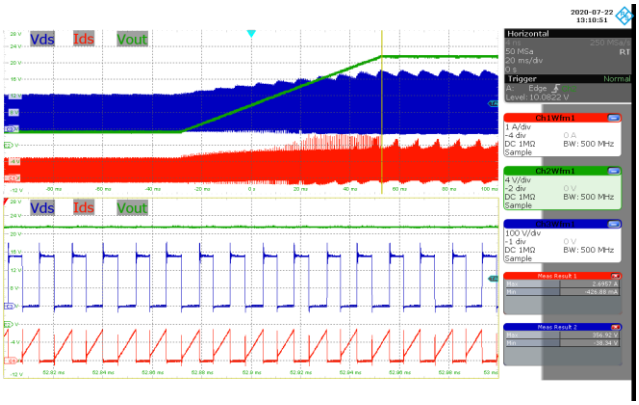

Figure 82 – Primary Drain Voltage and Current.
90 VAC, 3.3 V to 21 V V_{OUT} Transition, 3 A Load.
V_{DS_PRI} = 356.92 V Maximum.
CH1: I_{DS_PRI}, 1 A / div.
CH2: V_{OUT}, 4 V / div.
CH3: V_{DS_PRI}, 100 V / div.
Time: 20 ms / div. (20 μs / div. Zoom)

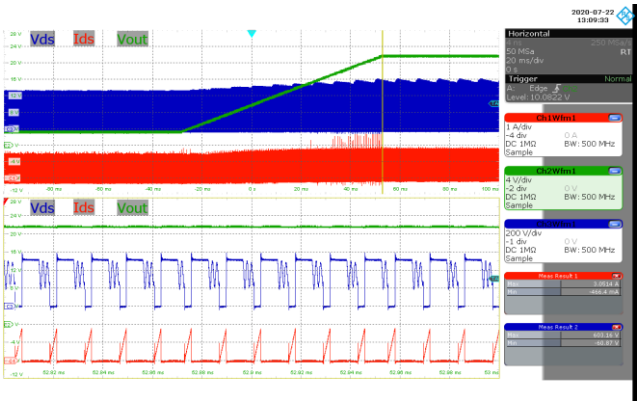

Figure 83 – Primary Drain Voltage and Current.
265 VAC, 3.3 V to 21 V V_{OUT} Transition, 3 A Load.
V_{DS_PRI} = 603.16 V Maximum.
CH1: I_{DS_PRI}, 1 A / div.
CH2: V_{OUT}, 4 V / div.
CH3: V_{DS_PRI}, 200 V / div.
Time: 20 ms / div. (20 μs / div. Zoom)

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14.5.2 SR FET Drain Voltage and Current, 3.3 V to 21 V Transition / 3 A Load

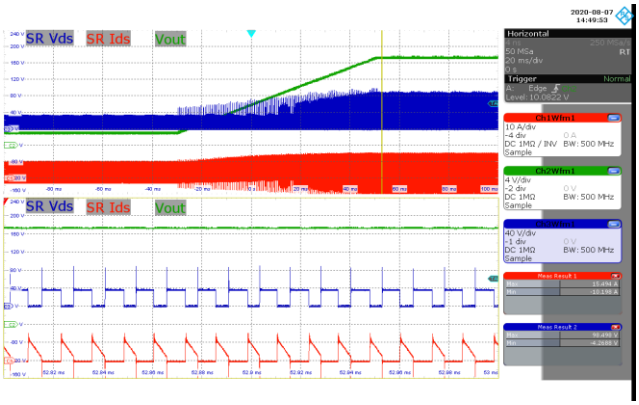

Figure 84 – Primary Drain Voltage and Current.
90 VAC, 3.3 V to 21 V V_{OUT} Transition, 3 A Load.
V_{DS_SRFET} = 98.498 V Maximum.
CH1: I_{DS_SRFET}, 10 A / div.
CH2: V_{OUT}, 4 V / div.
CH3: V_{DS_SRFET}, 40 V / div.
Time: 20 ms / div. (20 µs / div. Zoom)

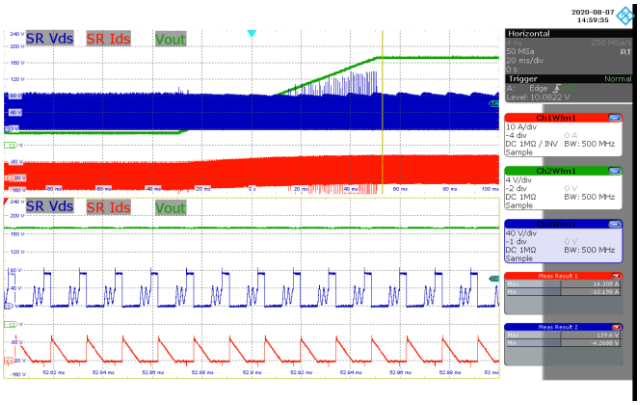

Figure 85 – Primary Drain Voltage and Current.
265 VAC, 3.3 V to 21 V V_{OUT} Transition, 3 A Load.
V_{DS_SRFET} = 139.6 V Maximum.
CH1: I_{DS_SRFET}, 10 A / div.
CH2: V_{OUT}, 4 V / div.
CH3: V_{DS_SRFET}, 40 V / div.
Time: 20 ms / div. (20 µs / div. Zoom)

14.6 *MinE-CAP Waveforms during Output Voltage Transition (3.3 V to 21 V, 3 A)*

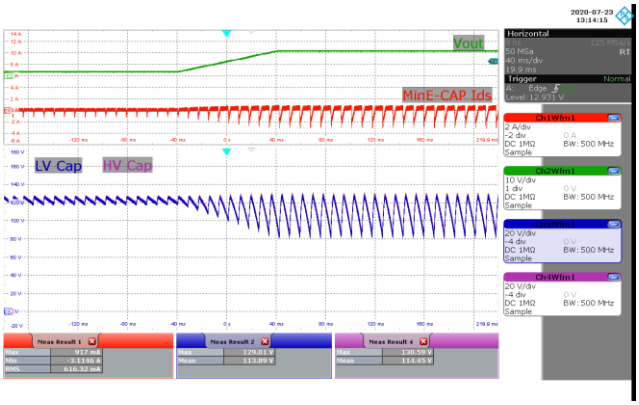

Figure 86 – MinE-CAP Waveforms.
90 VAC, 20.0 V, 3 A Load.
V_{LV_CAP} = 129.01 V Maximum.
CH1: MinE-CAP I_{DS}, 2 A / div.
CH2: V_{OUT}, 10 V / div.
CH3: V_{LV_CAP}, 20 V / div.
CH4: V_{HV_CAP}, 20 V / div.
Time: 40 ms / div.

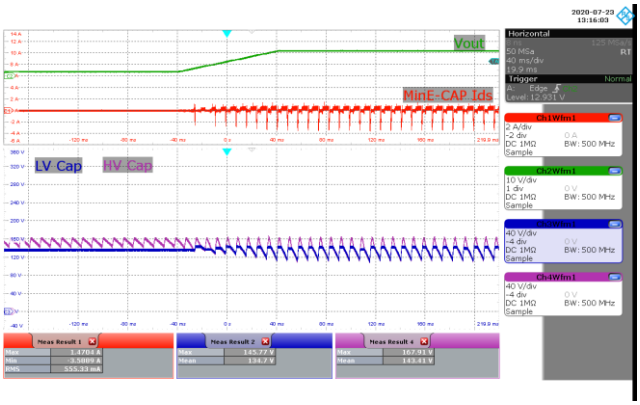

Figure 87 – MinE-CAP Waveforms.
115 VAC, 20.0 V, 3 A Load.
V_{LV_CAP} = 145.77 V Maximum.
CH1: MinE-CAP I_{DS}, 2 A / div.
CH2: V_{OUT}, 10 V / div.
CH3: V_{LV_CAP}, 40 V / div.
CH4: V_{HV_CAP}, 40 V / div.
Time: 40 ms / div.

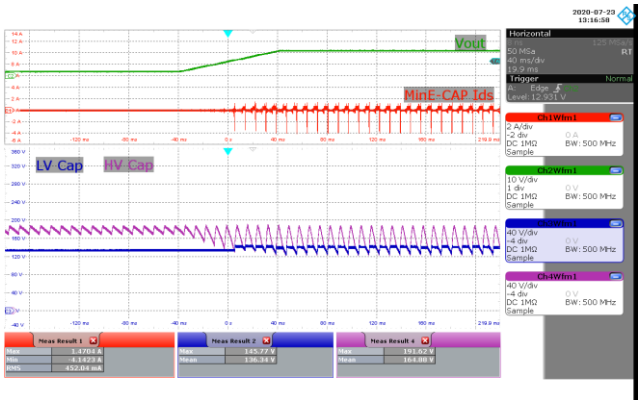

Figure 88 – MinE-CAP Waveforms.
132 VAC, 20.0 V, 3 A Load.
V_{LV_CAP} = 145.77 V Maximum.
CH1: MinE-CAP I_{DS}, 2 A / div.
CH2: V_{OUT}, 10 V / div.
CH3: V_{LV_CAP}, 40 V / div.
CH4: V_{HV_CAP}, 40 V / div.
Time: 40 ms / div.

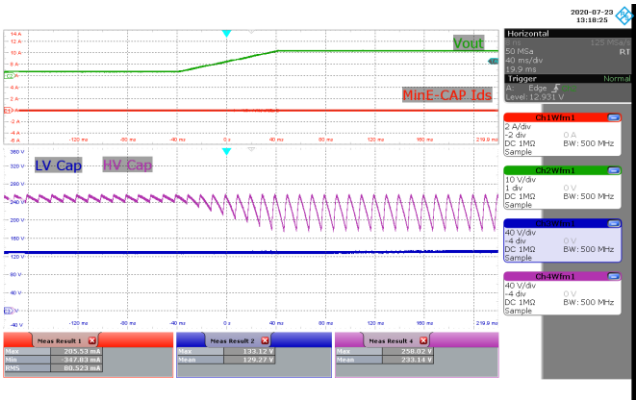

Figure 89 – MinE-CAP Waveforms.
180 VAC, 20.0 V, 3 A Load.
V_{LV_CAP} = 133.12 V Maximum.
CH1: MinE-CAP I_{DS}, 2 A / div.
CH2: V_{OUT}, 10 V / div.
CH3: V_{LV_CAP}, 40 V / div.
CH4: V_{HV_CAP}, 40 V / div.
Time: 40 ms / div.

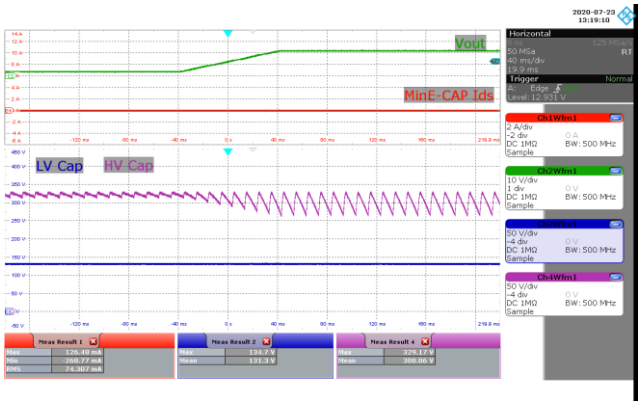

Figure 90 – MinE-CAP Waveforms.
230 VAC, 20.0 V, 3 A Load.
V_{LV_CAP} = 134.7 V Maximum.
CH1: MinE-CAP I_{DS}, 2 A / div.
CH2: V_{OUT}, 10 V / div.
CH3: V_{LV_CAP}, 50 V / div.
CH4: V_{HV_CAP}, 50 V / div.
Time: 40 ms / div.

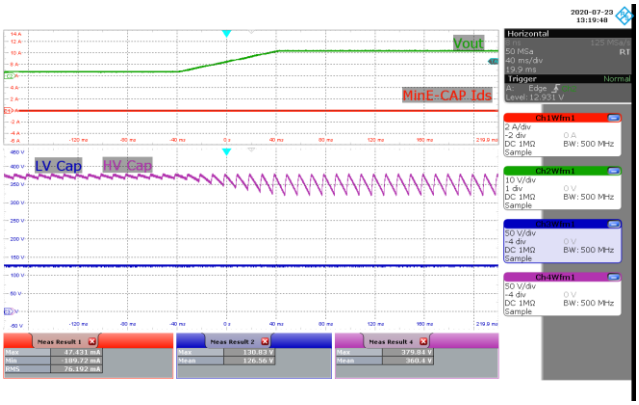

Figure 91 – MinE-CAP Waveforms.
265 VAC, 20.0 V, 3 A Load.
V_{LV_CAP} = 130.83 V Maximum.
CH1: MinE-CAP I_{DS}, 2 A / div.
CH2: V_{OUT}, 10 V / div.
CH3: V_{LV_CAP}, 50 V / div.
CH4: V_{HV_CAP}, 50 V / div.
Time: 40 ms / div.

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14.7 *Load Transient and Output Ripple Measurements*

14.7.1 Ripple Measurement Technique

For load transient response and DC output ripple measurements, a filtered oscilloscope probe is used to reduce spurious signals due to pick-up. Details of the probe modification are provided in the figures below.

A 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so it must be connected to match the polarity of the DC output (see below).

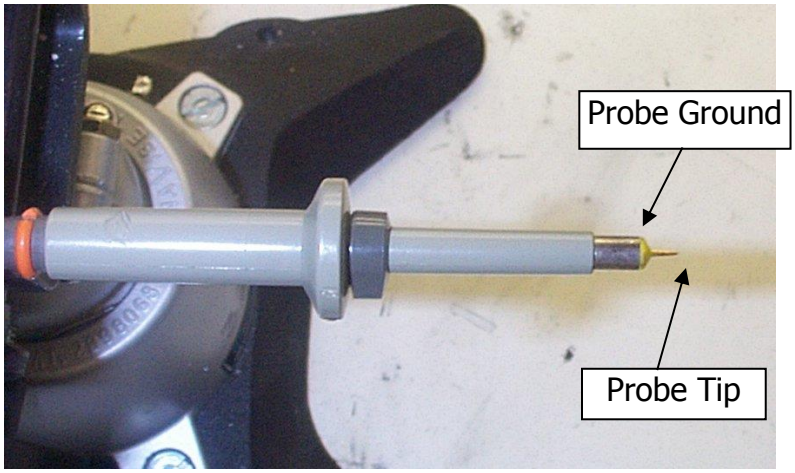

Figure 92 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

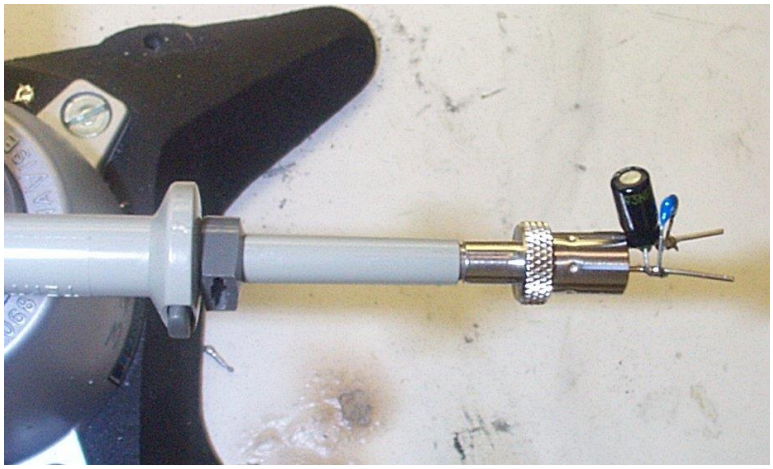

Figure 93 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

14.8 *Load Transient Response*

Note: 1. Output voltage waveforms captured at the end of 100 mΩ cable
2. Dynamic load settings: High = 50 ms; Low = 50 ms.
3. Load slew rate (150 mA / μs) is based on USB PD 3.0 PPS specification.

14.8.1 Output: 5 V / 3 A

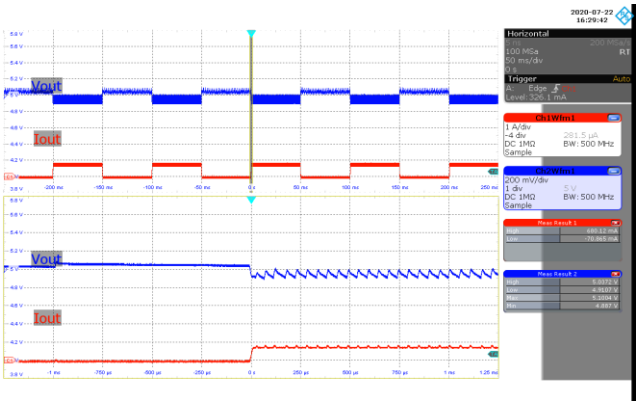

Figure 94 – Transient Response.
90 VAC, 5.0 V, 0 to 25% Load.
V_{OUT} = 5.10V max, 4.89 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

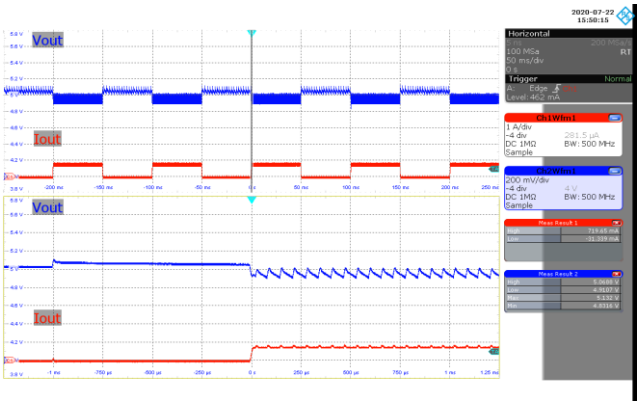

Figure 95 – Transient Response.
265 VAC, 5.0 V, 0 to 25% Load.
V_{OUT} = 5.13 V max, 4.83 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

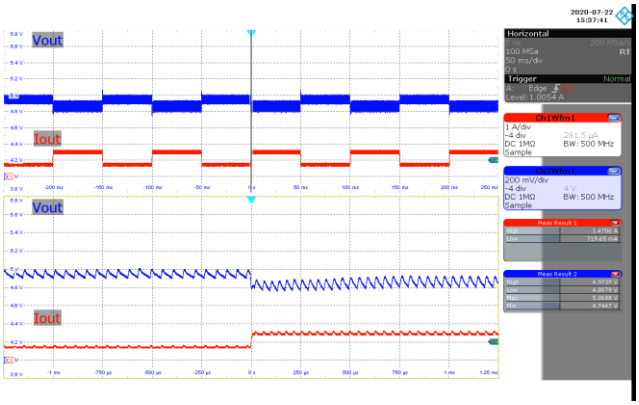

Figure 96 – Transient Response.
90 VAC, 5.0 V, 25% to 50% Load.
V_{OUT} = 5.07 V max, 4.74 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

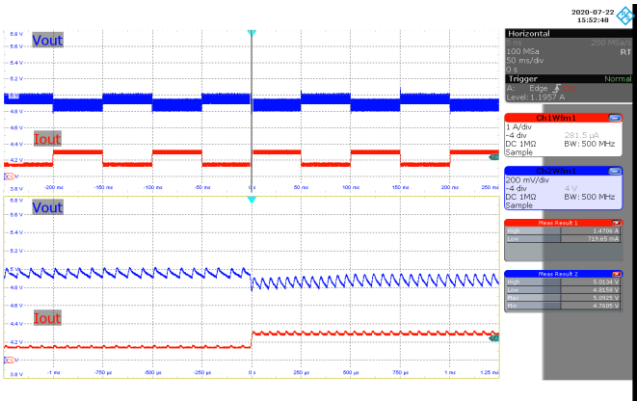

Figure 97 – Transient Response.
265 VAC, 5.0 V, 25% to 50% Load.
V_{OUT} = 5.09 V max, 4.76 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

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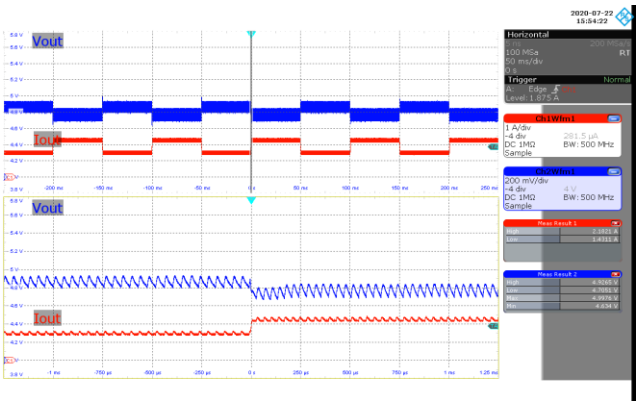

Figure 98 – Transient Response.
90 VAC, 5.0 V, 50% to 75% Load.
V_{OUT} = 4.99 V max, 4.63 V Min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 μs / div. Zoom).

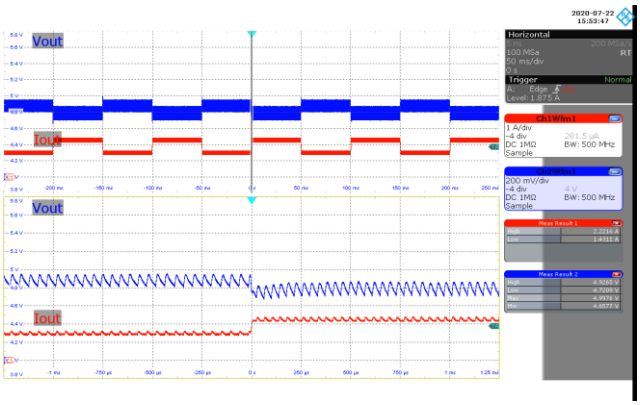

Figure 99 – Transient Response.
265 VAC, 5.0 V, 50% to 75% Load.
V_{OUT} = 4.99 V max, 4.65 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

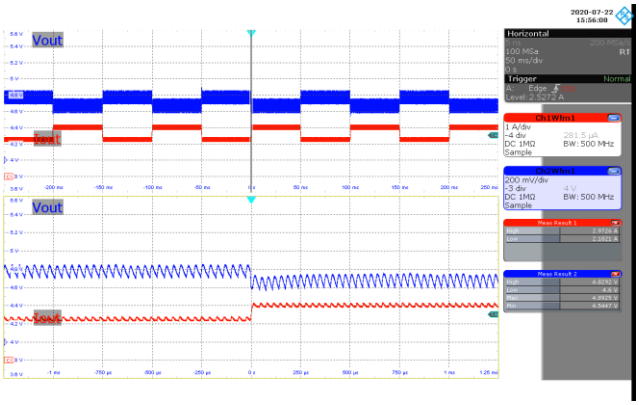

Figure 100 – Transient Response.
90 VAC, 5.0 V, 75% to 100% Load.
V_{OUT} = 4.89 V max, 4.54 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

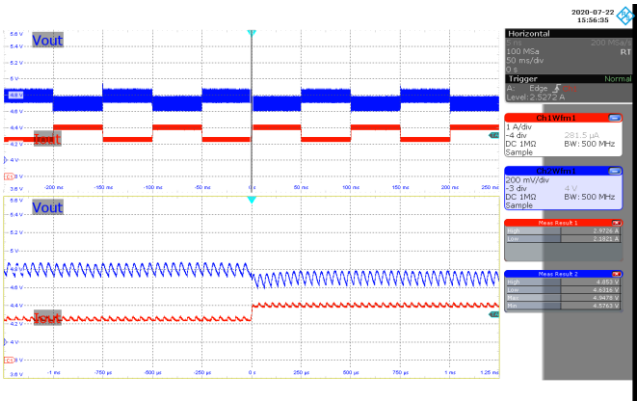

Figure 101 – Transient Response.
265 VAC, 5.0 V, 75% to 100% Load.
V_{OUT} = 4.95 V max, 4.58 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

14.8.2 Output: 9 V / 3 A

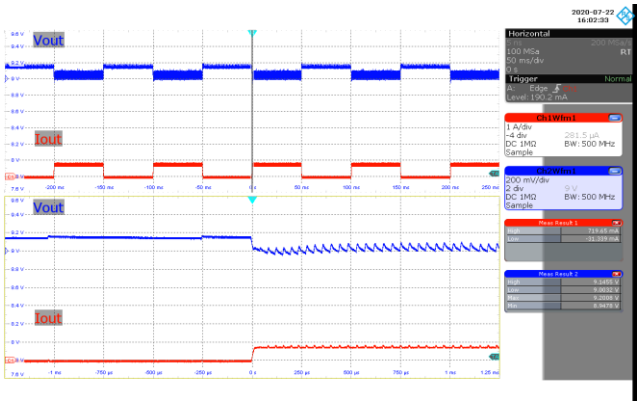

Figure 102 – Transient Response.
90 VAC, 9.0 V, 0 to 25% Load.
V_{OUT} = 9.20 V max, 8.95 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

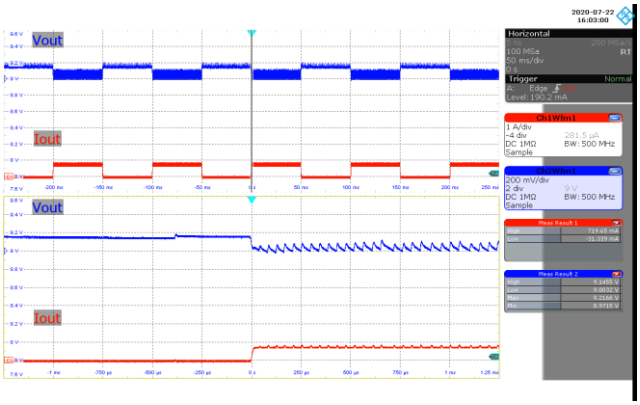

Figure 103 – Transient Response.
265 VAC, 9.0 V, 0 to 25% Load.
V_{OUT} = 9.22 V max, 8.97 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

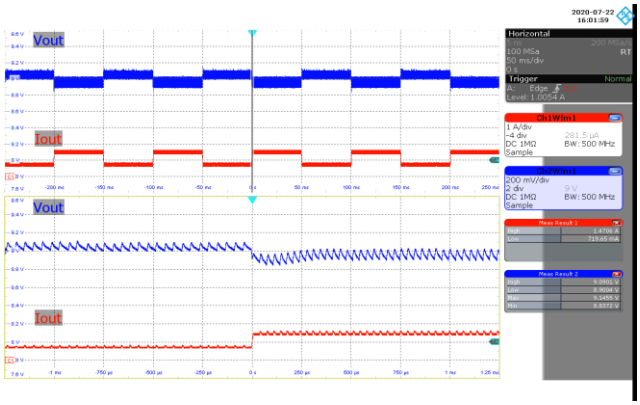

Figure 104 – Transient Response.
90 VAC, 9.0 V, 25% to 50% Load.
V_{OUT} = 9.15 V max, 8.84 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

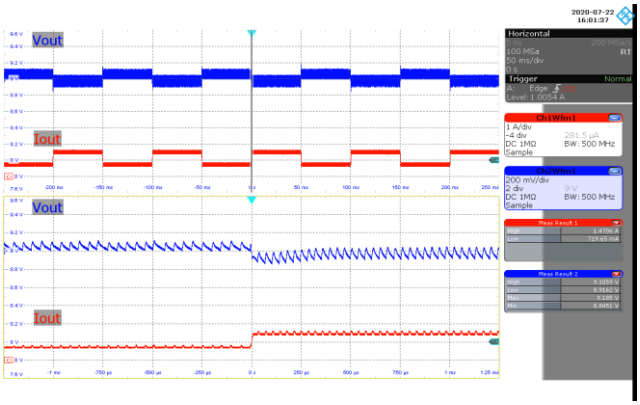

Figure 105 – Transient Response.
265 VAC, 9.0 V, 25% to 50% Load.
V_{OUT} = 9.19 V max, 8.85 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

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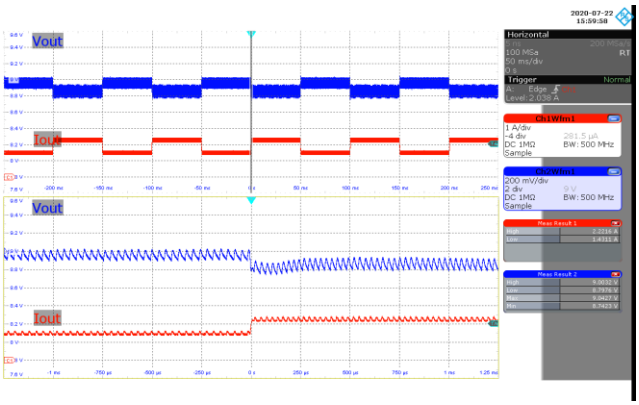

Figure 106 – Transient Response.
90 VAC, 9.0 V, 50% to 75% Load.
V_{OUT} = 9.04 V max, 8.74 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

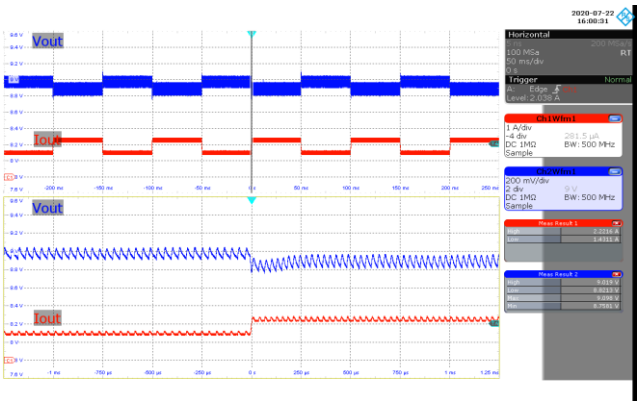

Figure 107 – Transient Response.
265 VAC, 9.0 V, 50% to 75% Load.
V_{OUT} = 9.1 V max, 8.76 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

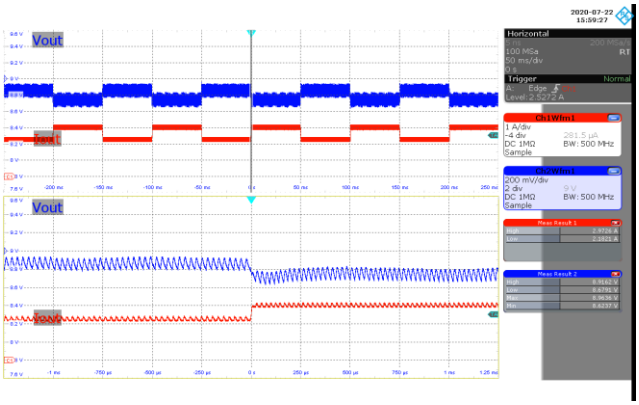

Figure 108 – Transient Response.
90 VAC, 9.0 V, 75% to 100% Load.
V_{OUT} = 8.96 V max, 8.62 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

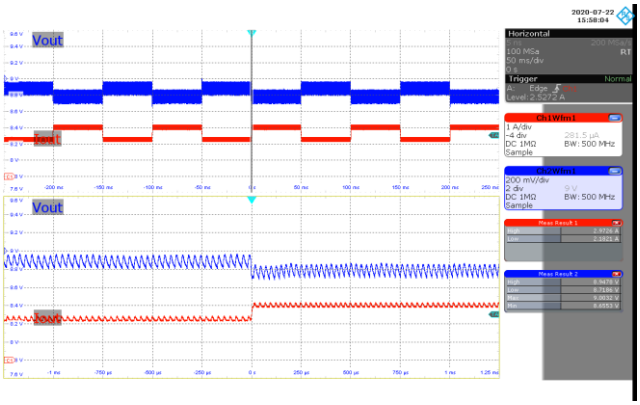

Figure 109 – Transient Response.
265 VAC, 9.0 V, 75% to 100% Load.
V_{OUT} = 9.00 V max, 8.66 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

14.8.3 Output: 15 V / 3 A

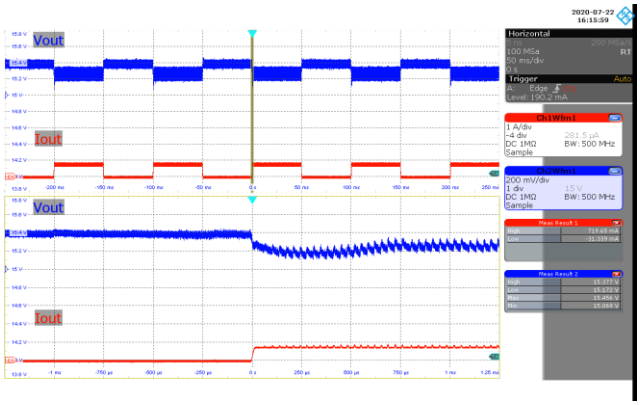

Figure 110 – Transient Response.
90 VAC, 15.0 V, 0 to 25% Load.
V_{OUT} = 15.46 V max, 15.07 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 µs / div. Zoom).

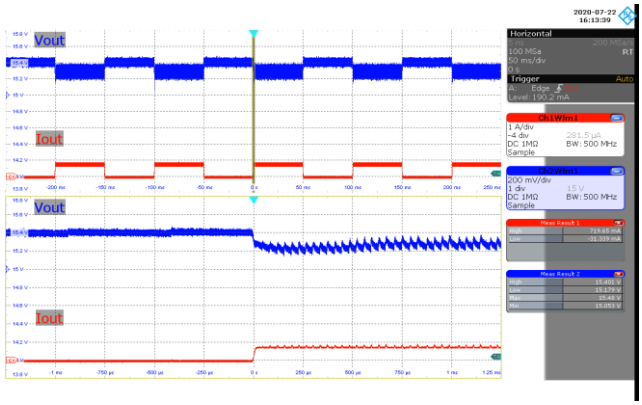

Figure 111 – Transient Response.
265 VAC, 15.0 V, 0 to 25% Load.
V_{OUT} = 15.48 V max, 15.05 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 µs / div. Zoom).

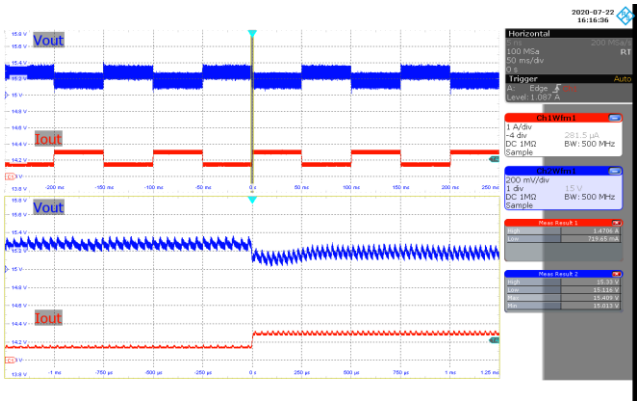

Figure 112 – Transient Response.
90 VAC, 15.0 V, 25% to 50% Load.
V_{OUT} = 15.41 V max, 15.01 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 µs / div. Zoom).

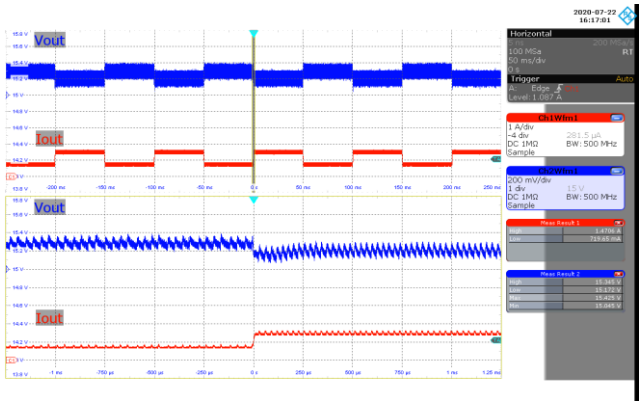

Figure 113 – Transient Response.
265 VAC, 15.0 V, 25% to 50% Load.
V_{OUT} = 15.43 V max, 15.05 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 µs / div. Zoom).

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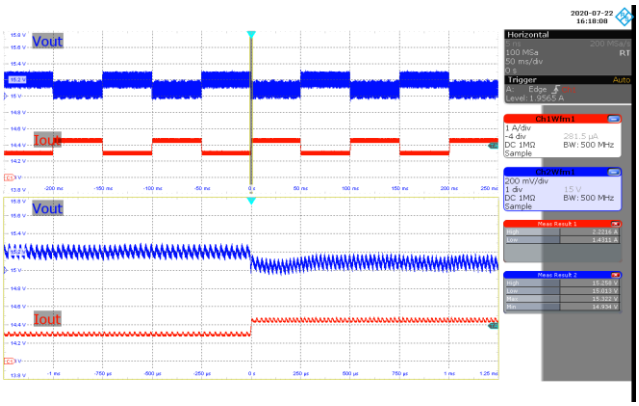

Figure 114 – Transient Response.
90 VAC, 15.0 V, 50% to 75% Load.
V_{OUT} = 15.32 V max, 14.93 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

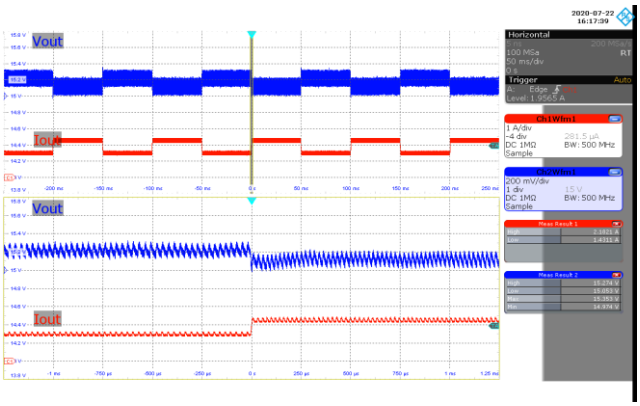

Figure 115 – Transient Response.
265 VAC, 15.0 V, 50% to 75% Load.
V_{OUT} = 15.35 V max, 14.97 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

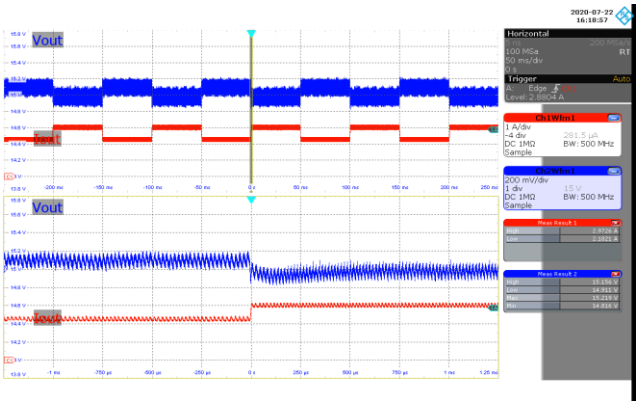

Figure 116 – Transient Response.
90 VAC, 15.0 V, 75% to 100% Load.
V_{OUT} = 15.22 V max, 14.82 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

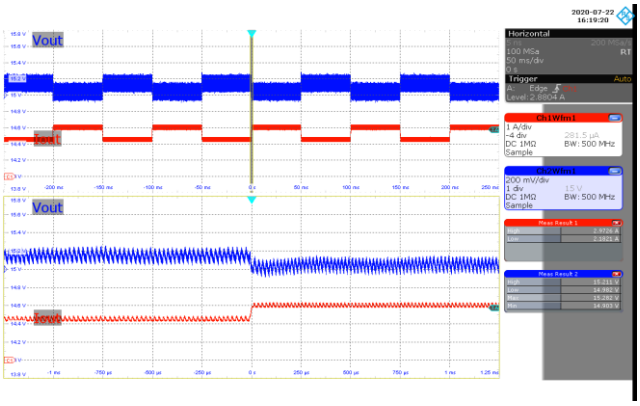

Figure 117 – Transient Response.
265 VAC, 15.0 V, 75% to 100% Load.
V_{OUT} = 15.28 V max, 14.90 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

14.8.4 Output: 20 V / 3 A

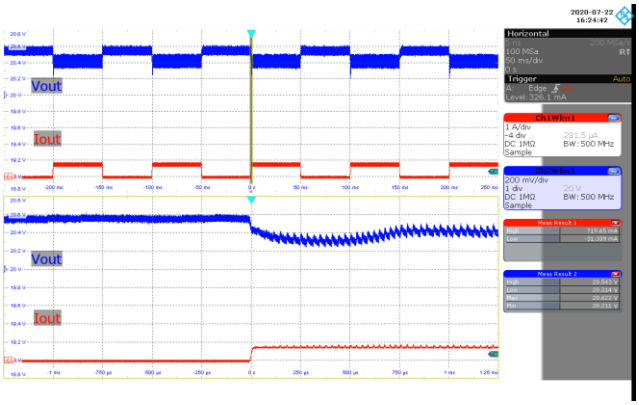

Figure 118 – Transient Response.
90 VAC, 20.0 V, 0 to 25% Load.
V_{OUT} = 20.62 V max, 20.21 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 µs / div. Zoom).

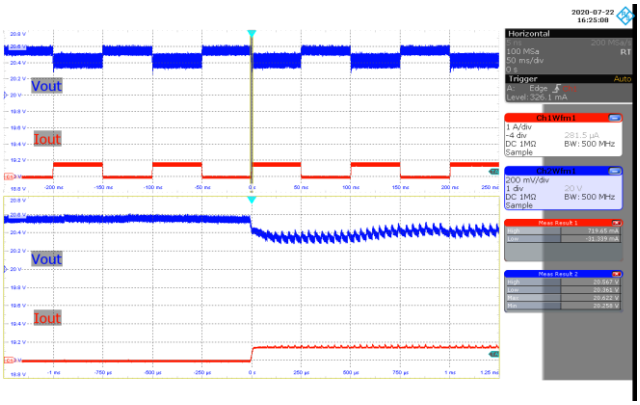

Figure 119 – Transient Response.
265 VAC, 20.0 V, 0 to 25% Load.
V_{OUT} = 20.62 V max, 20.26 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 µs / div. Zoom).

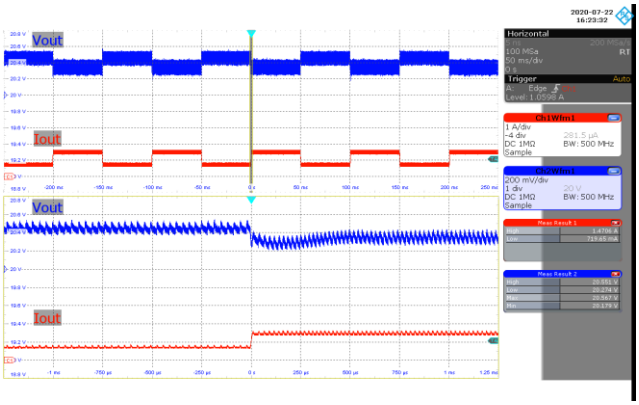

Figure 120 – Transient Response.
90 VAC, 20.0 V, 25% to 50% Load.
V_{OUT} = 20.57 V max, 20.18 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 µs / div. Zoom).

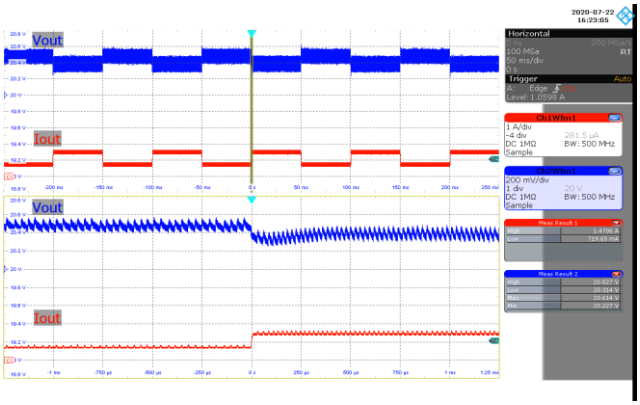

Figure 121 – Transient Response.
265 VAC, 20.0 V, 25% to 50% Load.
V_{OUT} = 20.61 V max, 20.23 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 µs / div. Zoom).

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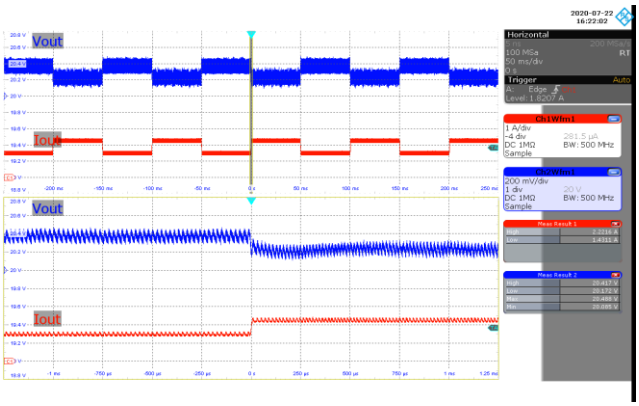

Figure 122 – Transient Response.
90 VAC, 20.0 V, 50% to 75% Load.
V_{OUT} = 20.49 V max, 20.09 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

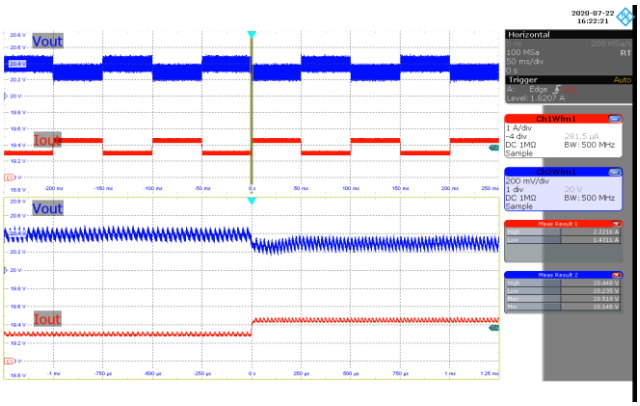

Figure 123 – Transient Response.
265 VAC, 20.0 V, 50% to 75% Load.
V_{OUT} = 20.52 V max, 20.15 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

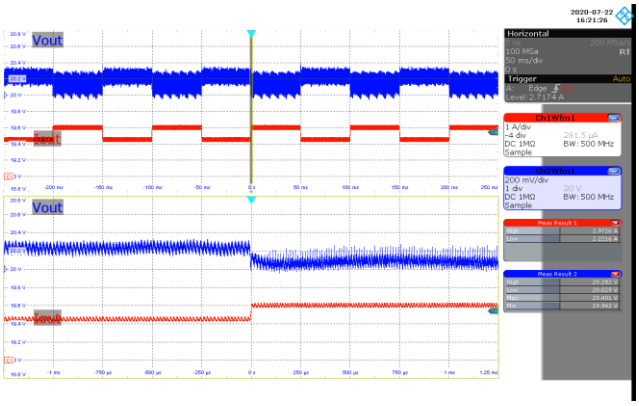

Figure 124 – Transient Response.
90 VAC, 20.0 V, 75% to 100% Load.
V_{OUT} = 20.40 V max, 19.94 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

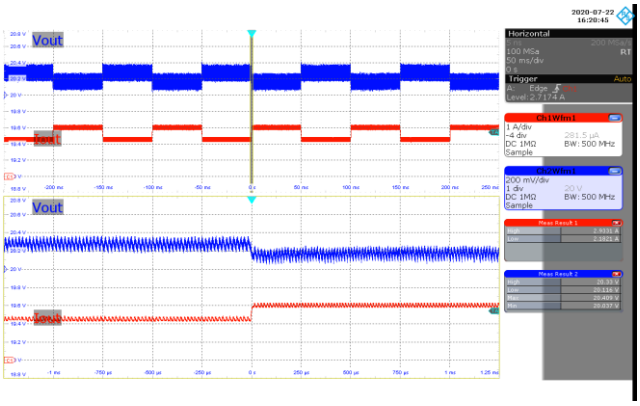

Figure 125 – Transient Response.
265 VAC, 20.0 V, 75% to 100% Load.
V_{OUT} = 20.41 V max, 20.04 V Min.
CH1: I_{OUT}, 1 A / div.
CH2: V_{OUT}, 200 mV / div.
Time: 50 ms / div. (250 μs / div. Zoom).

14.9 *Output Voltage Ripple Waveforms*

Note: 1. Output voltage waveforms captured at the end of 100 mΩ cable using the ripple measurement probe with decoupling capacitors.

14.9.1 Output: 5 V / 3 A

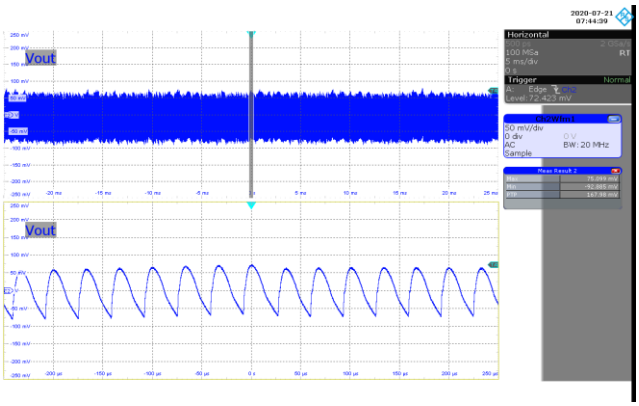

Figure 126 – Output Voltage Ripple.
90 VAC, 5.0 V, 3 A Load.
$V_{OUT(AC)}$ = 167.98 mV peak-to-peak.
CH2: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 μs / div. Zoom).

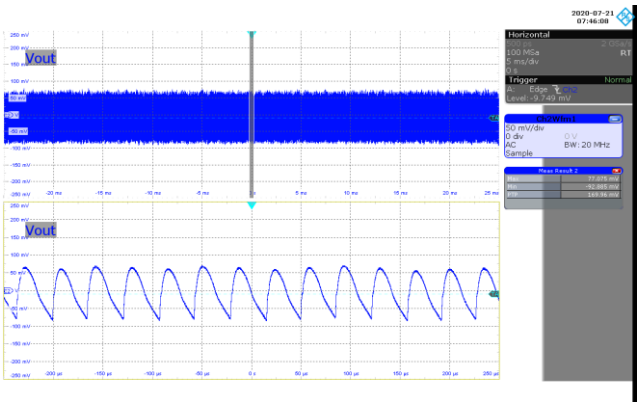

Figure 127 – Output Voltage Ripple.
265 VAC, 5.0 V, 3 A Load.
$V_{OUT(AC)}$ = 169.96 mV peak-to-peak.
CH2: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 μs / div. Zoom).

14.9.2 Output: 9 V / 3 A

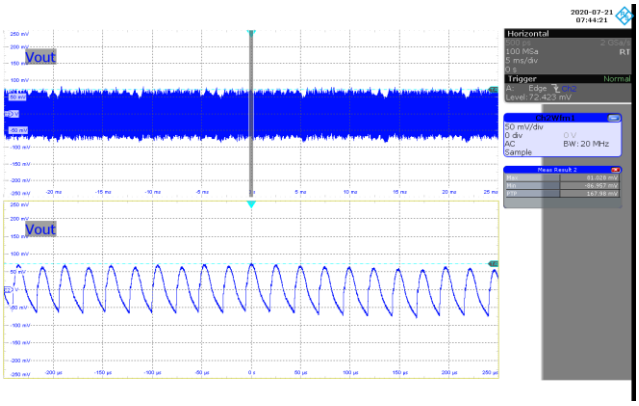

Figure 128 – Output Voltage Ripple.
90 VAC, 9.0 V, 3 A Load.
$V_{OUT(AC)}$ = 167.98 mV peak-to-peak.
CH2: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 μs / div. Zoom).

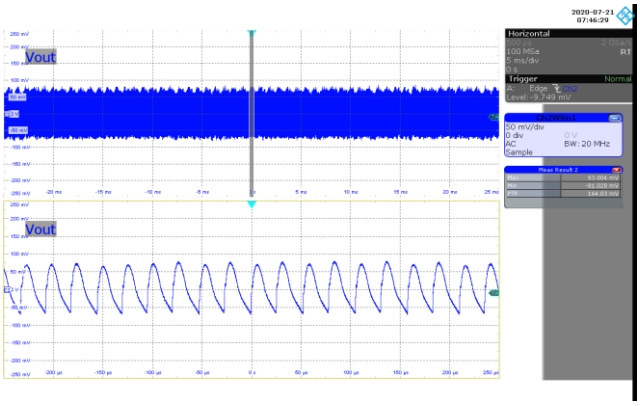

Figure 129 – Output Voltage Ripple.
265 VAC, 9.0 V, 3 A Load.
$V_{OUT(AC)}$ = 164.03 mV peak-to-peak.
CH2: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 μs / div. Zoom).

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14.9.3 Output: 15 V / 3 A

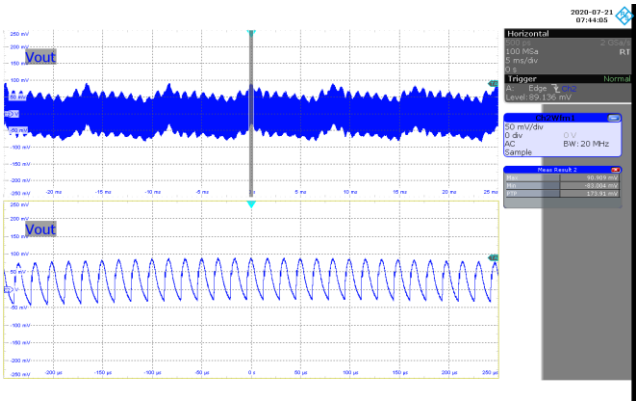

Figure 130 – Output Voltage Ripple.
90 VAC, 15.0 V, 3 A Load.
$V_{OUT(AC)}$ = 173.91 mV peak-to-peak.
CH2: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 μs / div. Zoom).

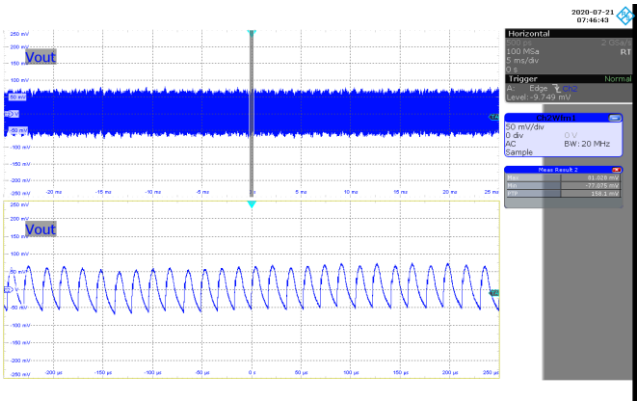

Figure 131 – Output Voltage Ripple.
265 VAC, 15.0 V, 3 A Load.
$V_{OUT(AC)}$ = 158.1 mV peak-to-peak.
CH2: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 μs / div. Zoom).

14.9.4 Output: 20 V / 3 A

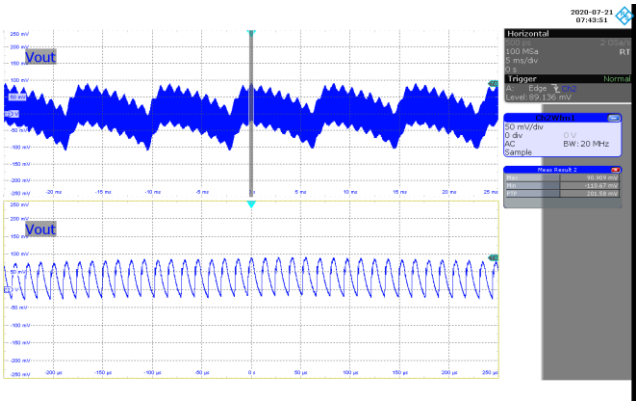

Figure 132 – Output Voltage Ripple.
90 VAC, 20.0 V, 3 A Load.
$V_{OUT(AC)}$ = 201.58 mV peak-to-peak.
CH2: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 μs / div. Zoom).

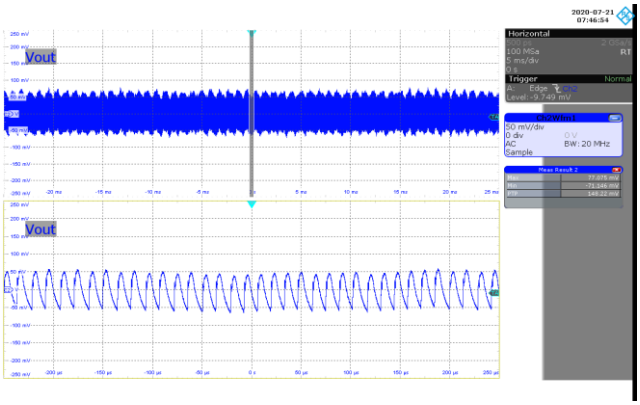

Figure 133 – Output Voltage Ripple.
265 VAC, 20.0 V, 3 A Load.
$V_{OUT(AC)}$ = 148.22 mV peak-to-peak.
CH2: $V_{OUT(AC)}$, 200 mV / div.
Time: 5 ms / div. (50 μs / div. Zoom).

14.10 *Output Voltage Ripple Amplitude vs. Load*

14.10.1 Output: 5 V / 3 A

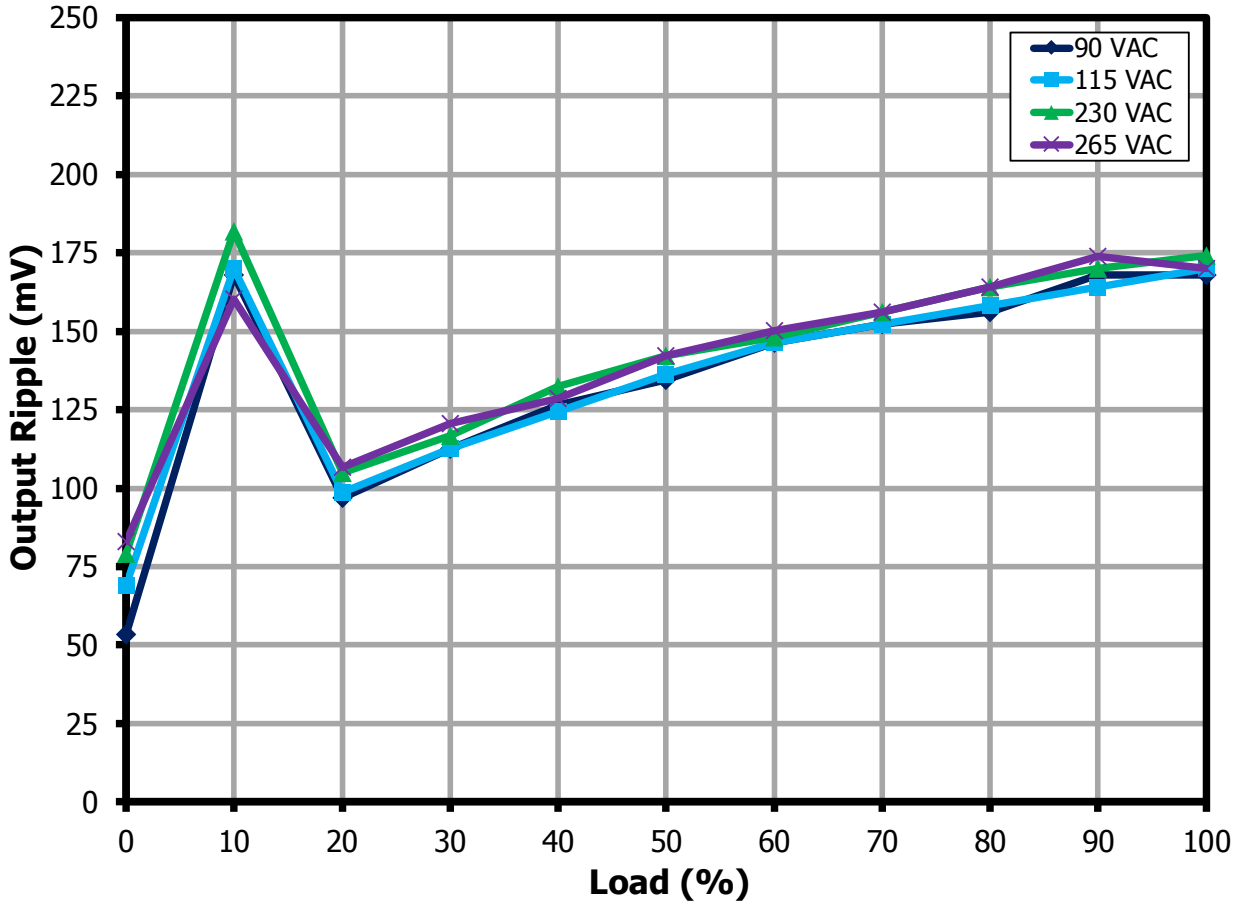

Figure 134 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 5 V Output.

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14.10.2 Output: 9 V / 3 A

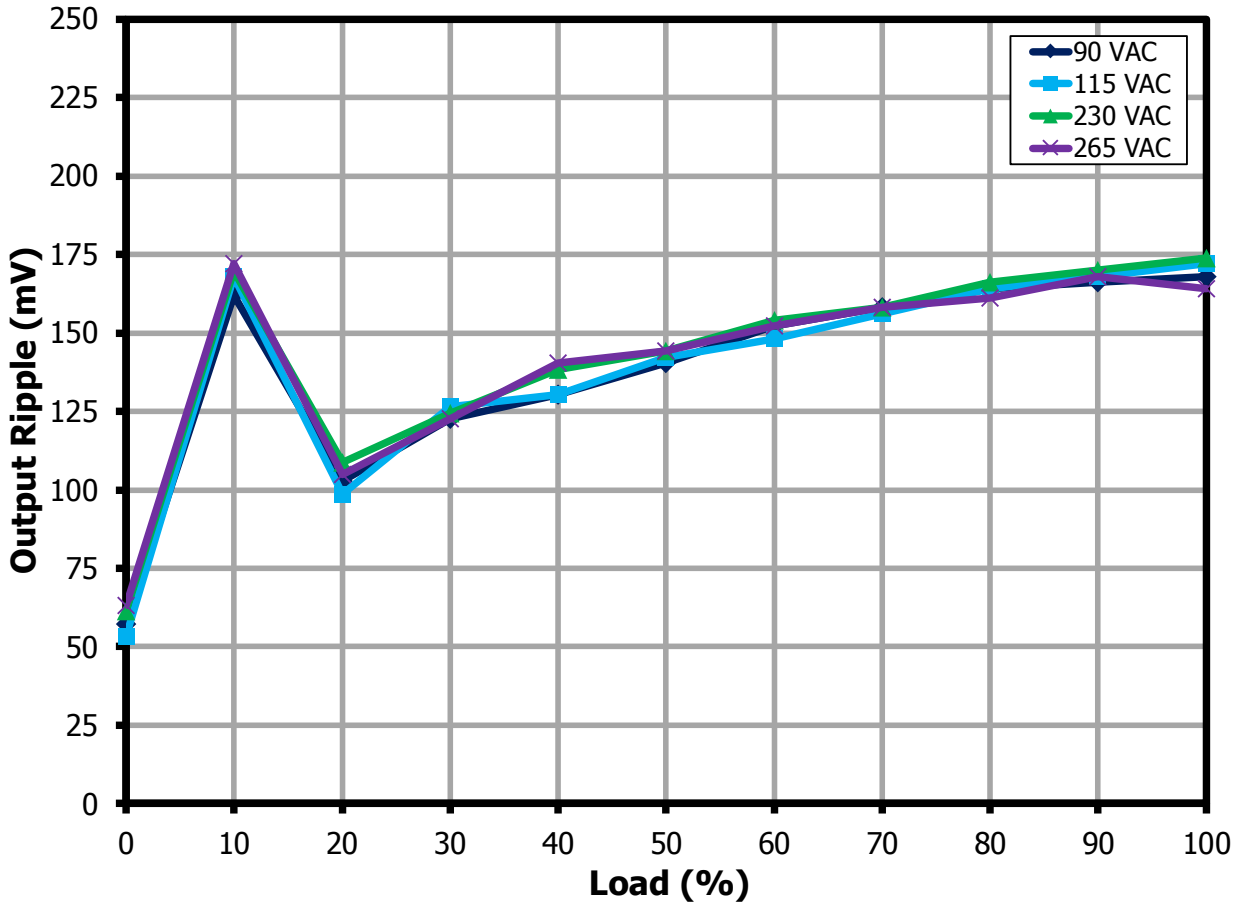

Figure 135 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 9 V Output.

14.10.3 Output: 15 V / 3 A

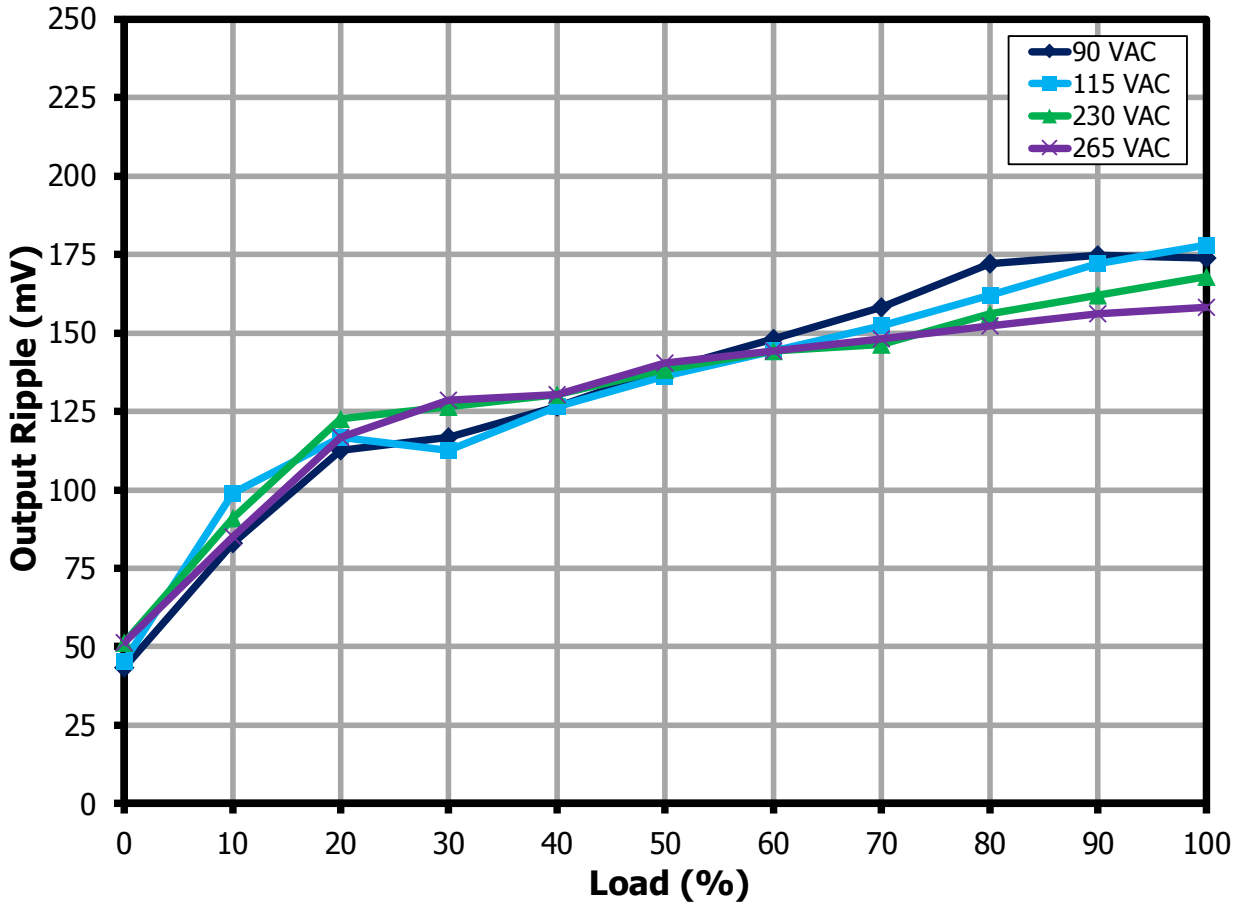

Figure 136 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 15 V Output.

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14.10.4 Output: 20 V / 3 A

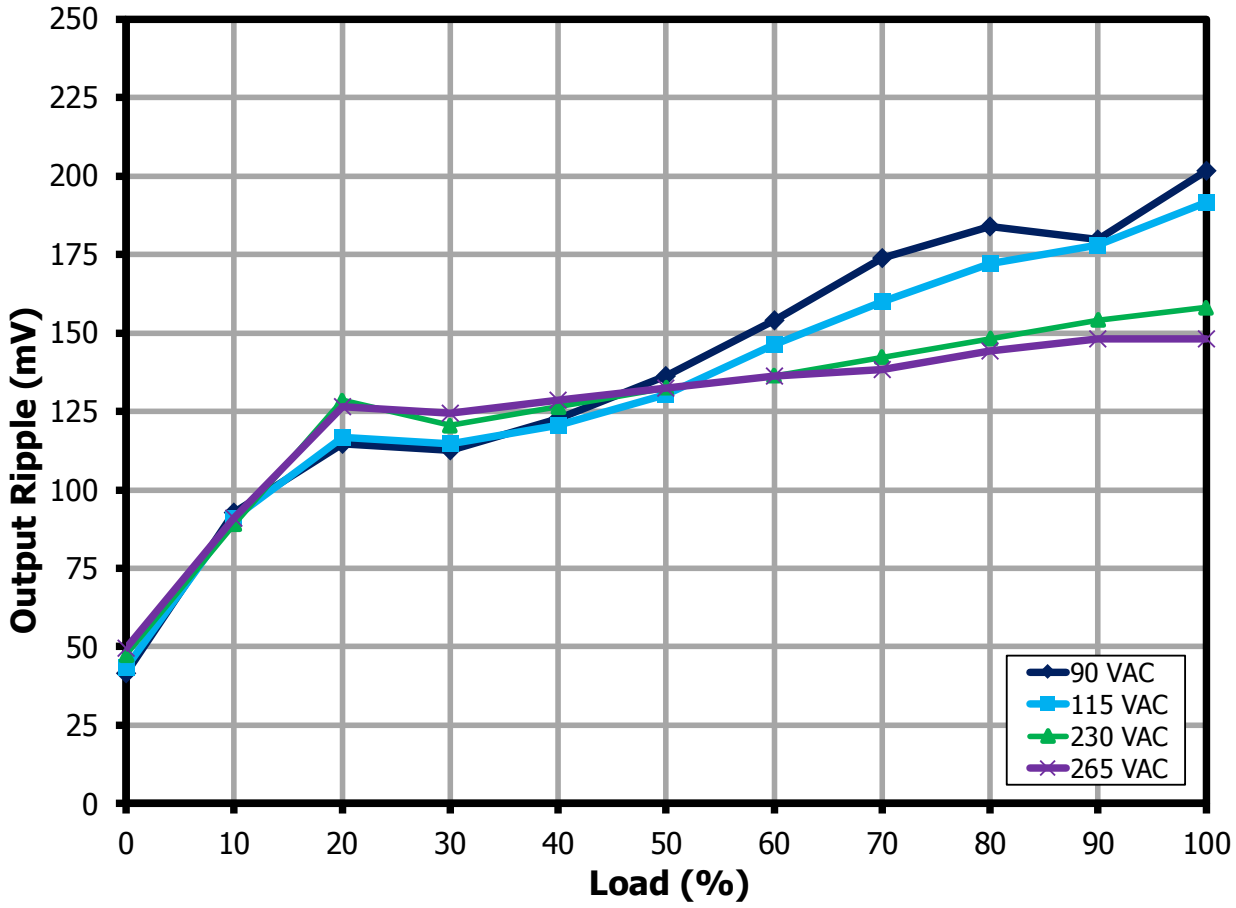

Figure 137 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 20 V Output.

15 CV/CC Profile

Note: 1. One Programmable Power Supply (PPS) Augmented Power Data Objects (APDO) is supported in this design:

- PDO5: 3.3 V – 21 V / 3 A PPS

15.1 *Output: 21 V / 3 A PPS Request, PDO5*

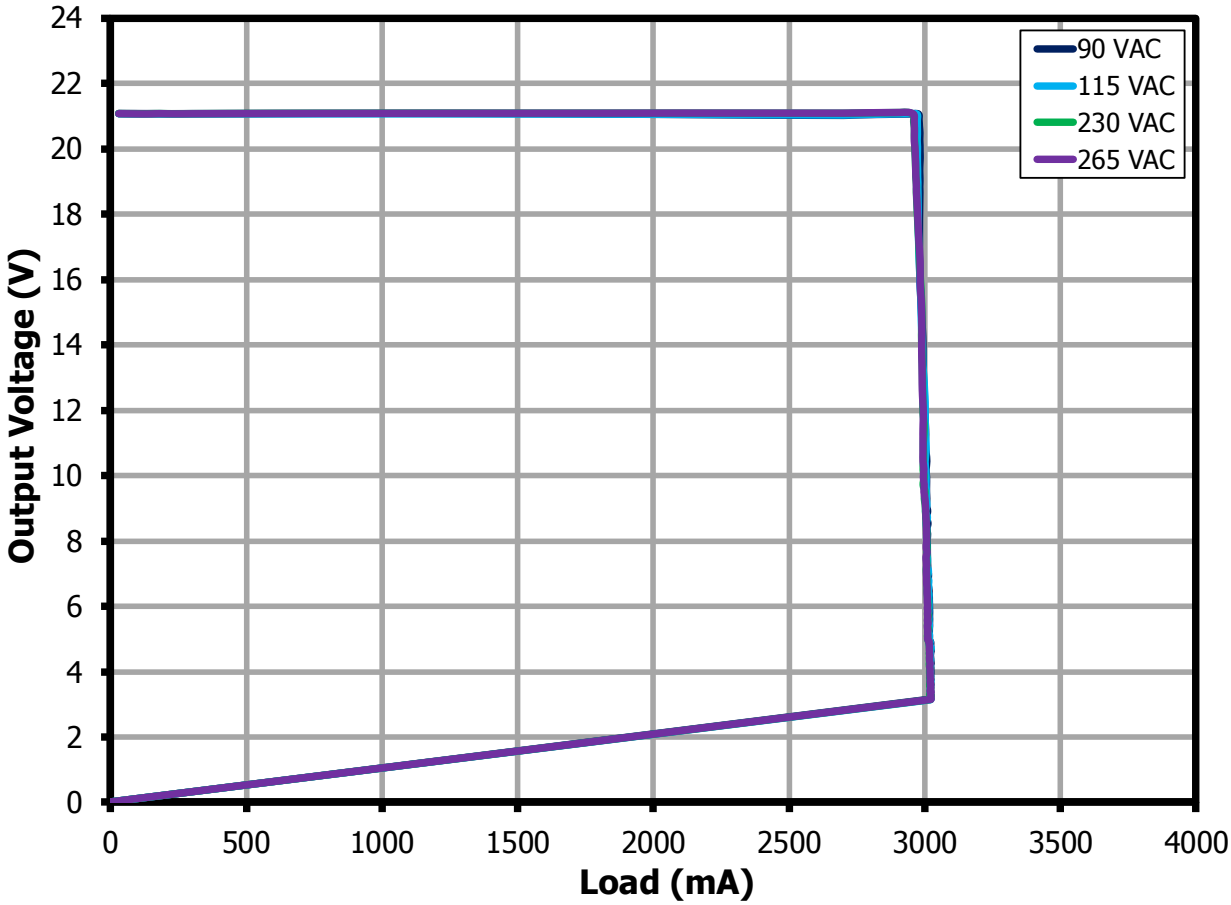

Figure 138 – CV/CC Profile for 21 V / 3 A PPS Request.

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16 Voltage Step and Current Limit Test using Quadramax and Total Phase Analyzer

16.1 *Voltage Step Test (VST)*

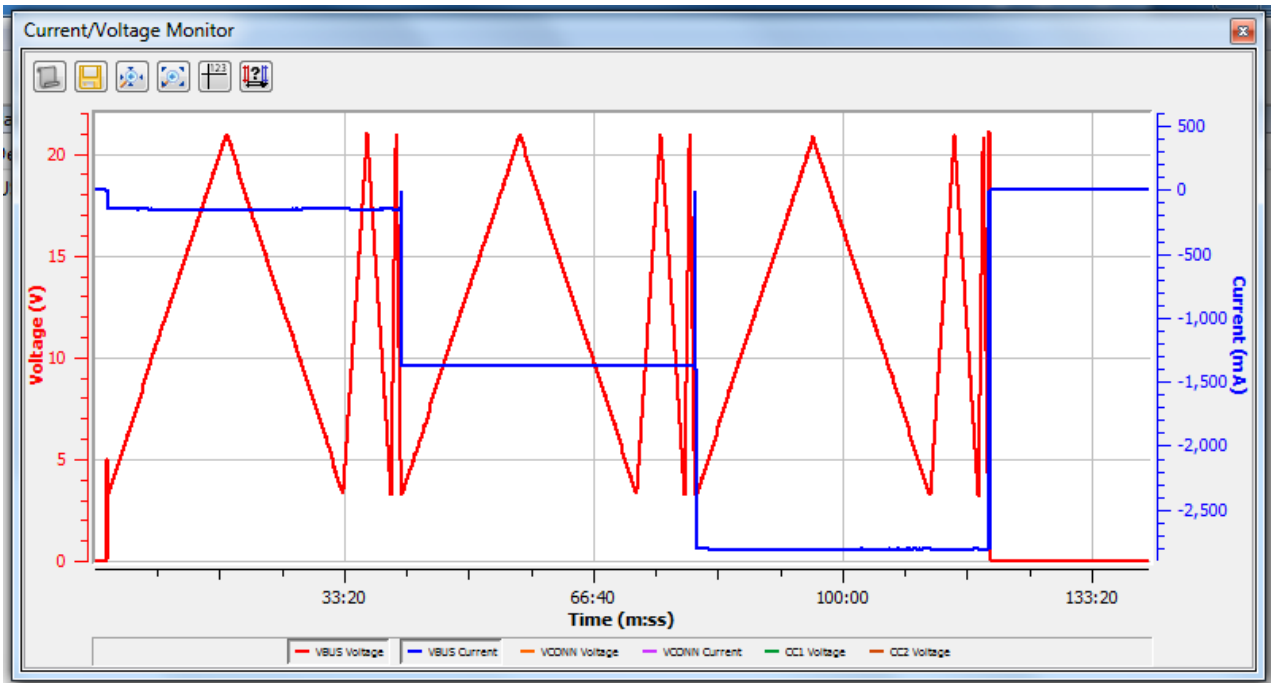

Figure 139 – Plot of SPT.6 VST from Total Phase Analyzer.

16.2 *Current Limit Test (CLT)*

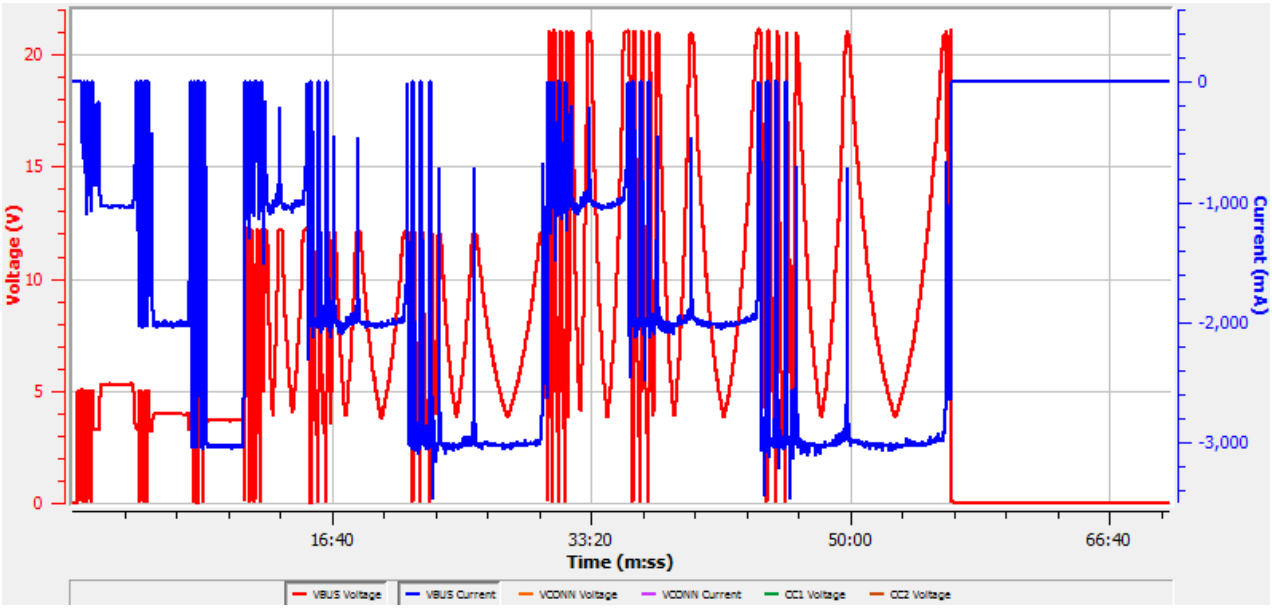

Figure 140 – Plot of SPT.7 CLT from Total Phase Analyzer.

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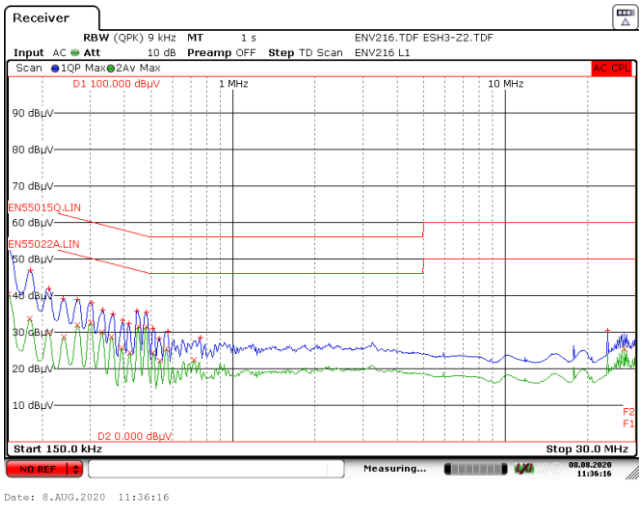
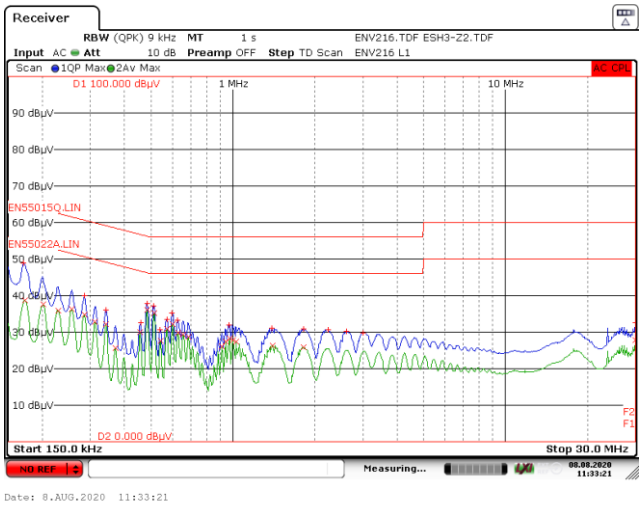
17 Conducted EMI

17.1 *Floating Ground (QPK / AV)*

17.1.1 Output: 5 V / 3 A

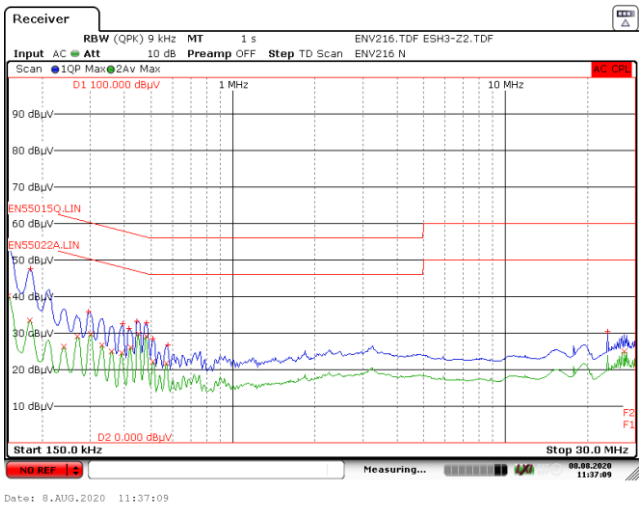


115 VAC.

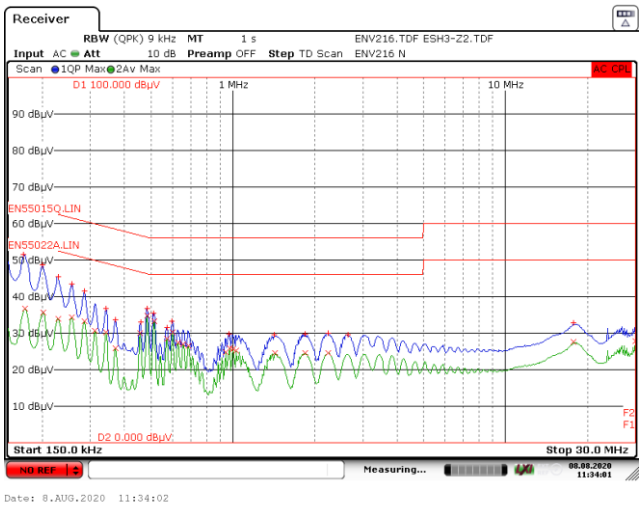


230 VAC.

Figure 141 – Floating Ground EMI, 5 V / 3 A Load [Line Scan].



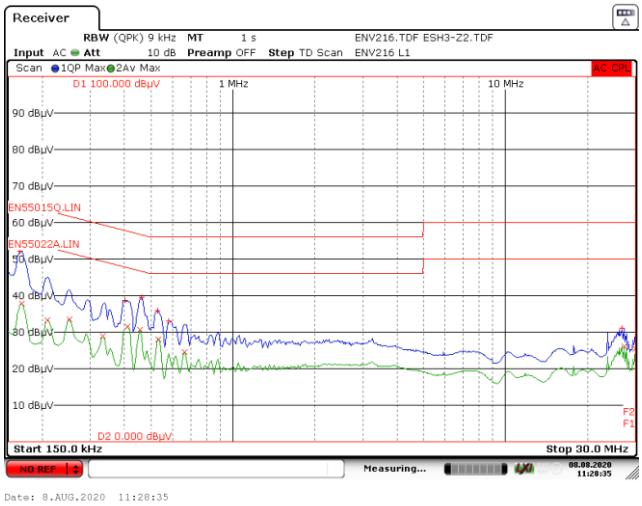
115 VAC.



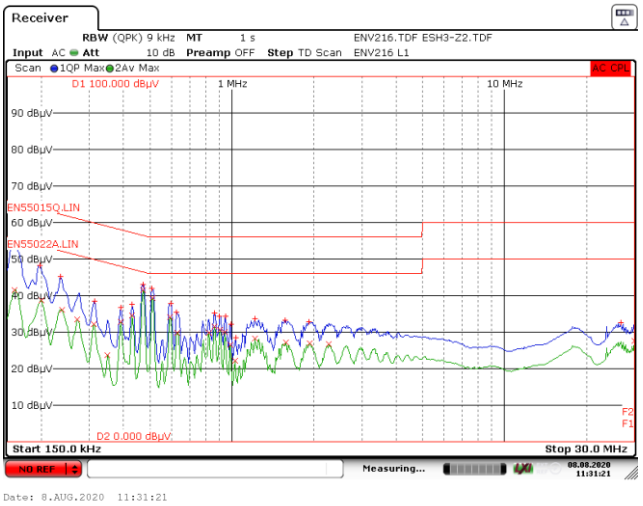
230 VAC.

Figure 142 – Floating Ground EMI, 5 V / 3 A Load [Neutral Scan].

17.1.2 Output: 9 V / 3 A

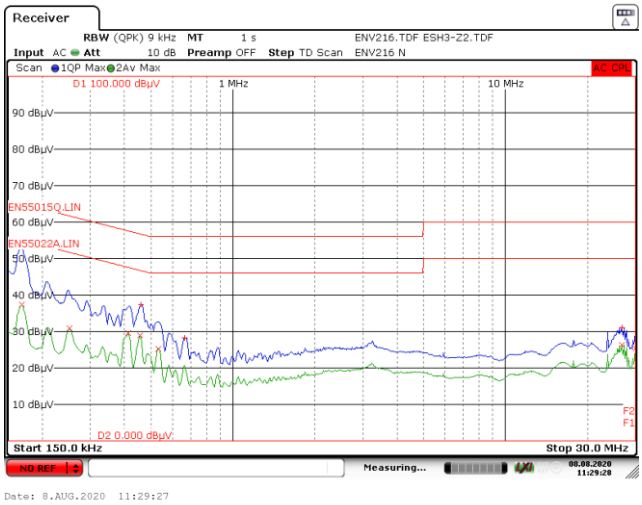


115 VAC.

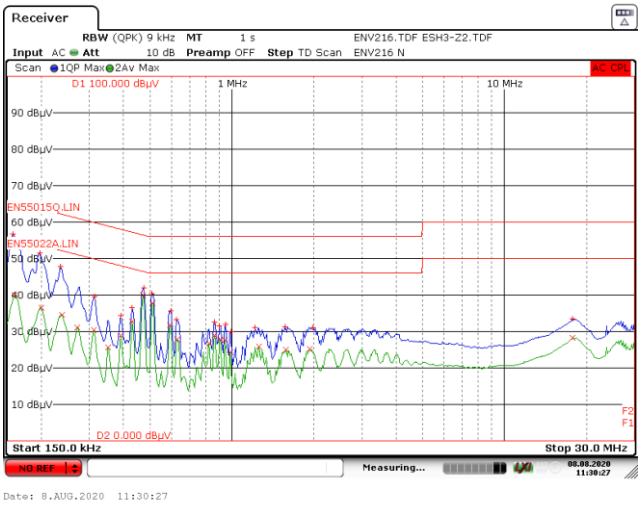


230 VAC.

Figure 143 – Floating Ground EMI, 9 V / 3 A Load [Line Scan].



115 VAC.



230 VAC.

Figure 144 – Floating Ground EMI, 9 V / 3 A Load [Neutral Scan].

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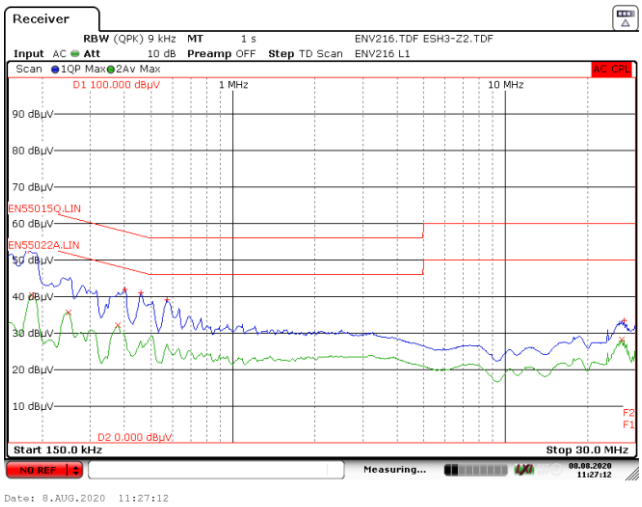
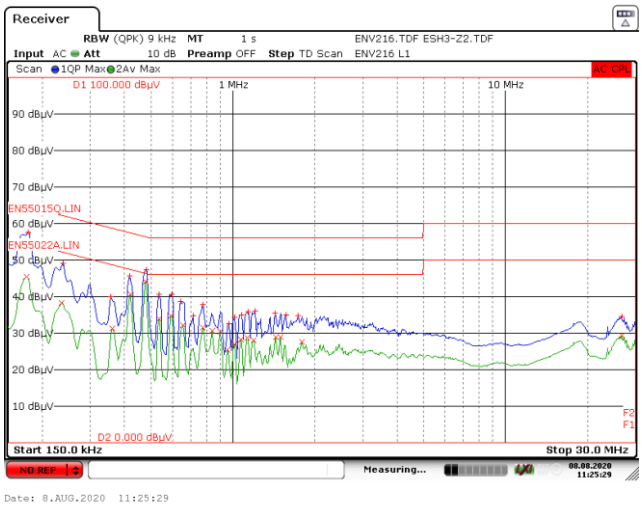
17.1.3 Output: 15 V / 3 A

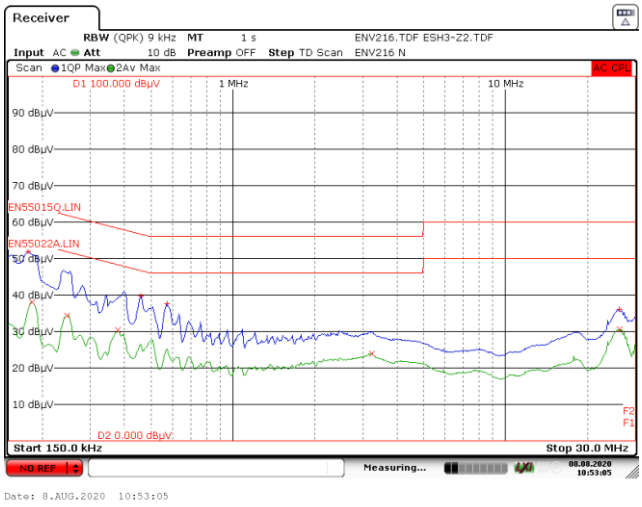


115 VAC.

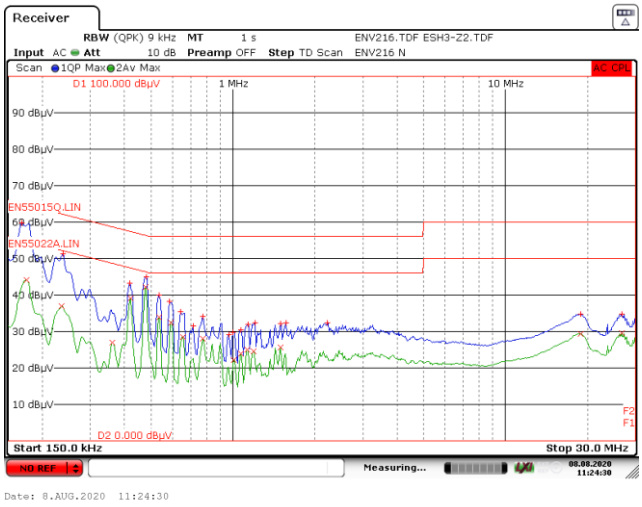


230 VAC.

Figure 145 – Floating Ground EMI, 15 V / 3 A Load [Line Scan].



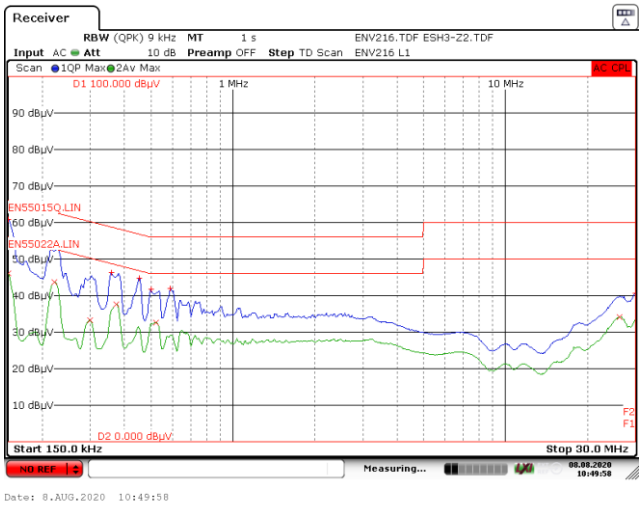
115 VAC.



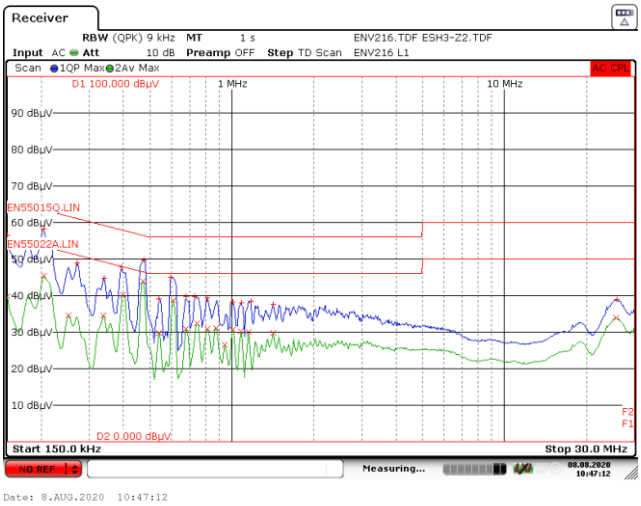
230 VAC.

Figure 146 – Floating Ground EMI, 15 V / 3 A Load [Neutral Scan].

17.1.4 Output: 20 V / 3 A

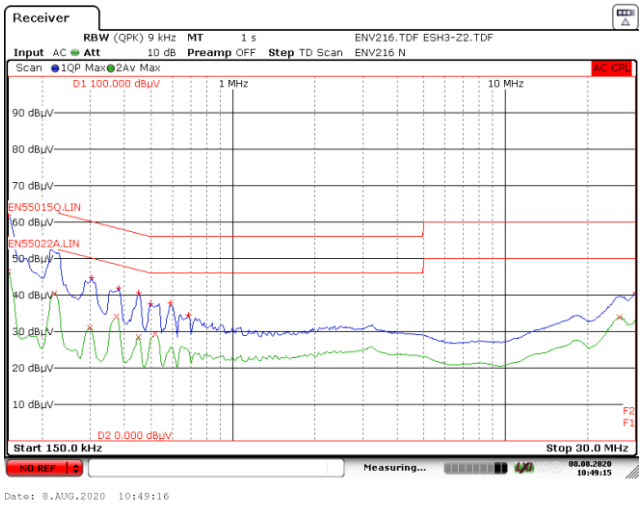


115 VAC.

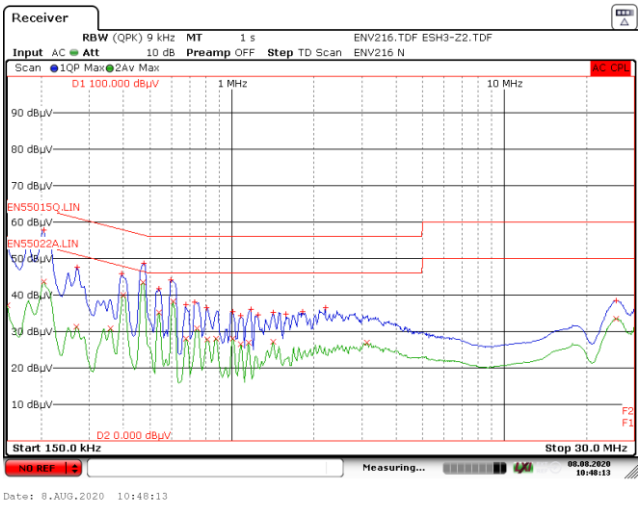


230 VAC.

Figure 147 – Floating Ground EMI, 20 V / 3 A Load [Line Scan].



115 VAC.



230 VAC.

Figure 148 – Floating Ground EMI, 20 V / 3 A Load [Neutral Scan].

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18 Combination Wave Surge

The unit was subjected to ±1000 V differential-mode and ±2000 V common-mode combination wave surge at several line phase angles with 10 strikes for each condition.

A test failure is defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

18.1 *Differential Mode Surge (L1 to L2), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A	Test Result 20 V / 3 A
+1000	L1 to L2	0	Pass	Pass
-1000	L1 to L2	0	Pass	Pass
+1000	L1 to L2	90	Pass[1]	Pass[1]
-1000	L1 to L2	90	Pass[1]	Pass[1]
+1000	L1 to L2	270	Pass[1]	Pass[1]
-1000	L1 to L2	270	Pass[1]	Pass[1]

[1]Power supply might initiate Auto-Restart protection due to Line OV condition

18.2 *Common Mode Surge (L1, L2 to PE), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A	Test Result 20 V / 3 A
+2000	L1, L2 to PE	0	Pass	Pass
-2000	L1, L2 to PE	0	Pass	Pass
+2000	L1, L2 to PE	90	Pass	Pass
-2000	L1, L2 to PE	90	Pass	Pass
+2000	L1, L2 to PE	270	Pass	Pass
-2000	L1, L2 to PE	270	Pass	Pass

18.3 *Common Mode Surge (L1 to PE), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A	Test Result 20 V / 3 A
+2000	L1 to PE	0	Pass	Pass
-2000	L1 to PE	0	Pass	Pass
+2000	L1 to PE	90	Pass[1]	Pass[1]
-2000	L1 to PE	90	Pass	Pass
+2000	L1 to PE	270	Pass	Pass
-2000	L1 to PE	270	Pass[1]	Pass[1]

[1]Power supply might initiate Auto-Restart protection due to Line OV condition.

18.4 *Common Mode Surge (L2 to PE), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A	Test Result 20 V / 3 A
+2000	L2 to PE	0	Pass	Pass
-2000	L2 to PE	0	Pass	Pass
+2000	L2 to PE	90	Pass	Pass
-2000	L2 to PE	90	Pass[1]	Pass[1]
+2000	L2 to PE	270	Pass[1]	Pass[1]
-2000	L2 to PE	270	Pass	Pass

[1]Power supply might initiate Auto-Restart protection due to Line OV condition

Note: Surge events might trigger input line OV Protection and initiate an auto-restart. Auto-restart (AR) is one of the safety features of InnoSwitch3-Pro to protect the converter from fault conditions. For applications that require completely no output interruption, the design can be modified to have a higher input line OVP voltage threshold or with the input line OVP completely disabled.

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19 Electrostatic Discharge

The unit was tested with ±8 kV to ±16.5 kV air discharge and ±8.8 kV contact discharge with 10 strikes for each condition at the following locations:

- End of cable +VOUT
- End of cable GND
- On-board +VOUT
- On-board GND
- End of cable CC1
- End of cable CC2
- On-board CC1
- On-board CC2

A test failure is defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

Note: 1. End of cable discharge points (VOUT, GND, CC1, CC2) located on the USB-C power adapter tester Tiny-PAT
2. Type-C cable for all test conditions: Passive 3 A cable, 1 meter (Google)

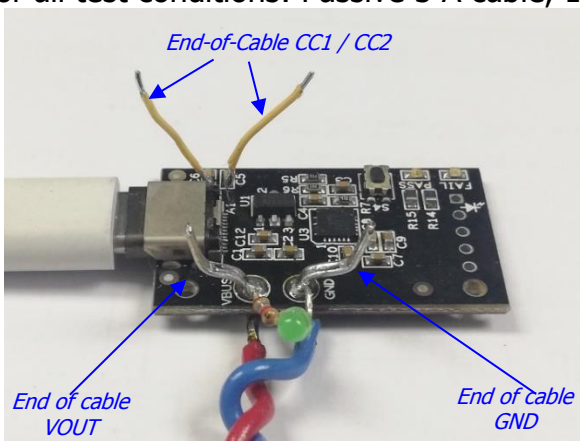

Figure 149 – End-of-Cable ESD Discharge Points.

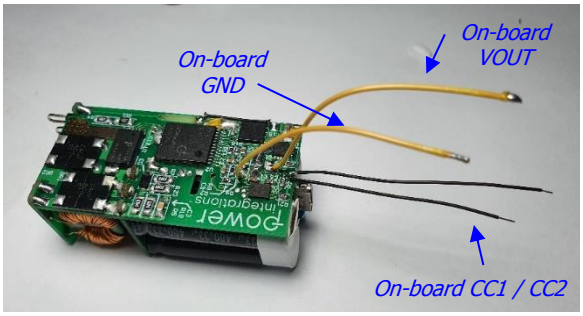

Figure 150 - On-board ESD Discharge Points.

19.1 *Air Discharge, +VOUT and GND, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location		Test Result 5 V / 0 A	Test Result 20 V / 3 A
+8	End of Cable	+VOUT	Pass	Pass
		GND	Pass	Pass
-8		+VOUT	Pass	Pass
		GND	Pass	Pass
+10		+VOUT	Pass	Pass
		GND	Pass	Pass
-10		+VOUT	Pass	Pass
		GND	Pass	Pass
+12		+VOUT	Pass	Pass
		GND	Pass	Pass
-12		+VOUT	Pass	Pass
		GND	Pass	Pass
+14		+VOUT	Pass	Pass
		GND	Pass	Pass
-14		+VOUT	Pass	Pass
		GND	Pass	Pass
+16.5		+VOUT	Pass	Pass
		GND	Pass	Pass
-16.5		+VOUT	Pass	Pass
		GND	Pass	Pass
+8	On the Board	+VOUT	Pass	Pass
		GND	Pass	Pass
-8		+VOUT	Pass	Pass
		GND	Pass	Pass
+10		+VOUT	Pass	Pass
		GND	Pass	Pass
-10		+VOUT	Pass	Pass
		GND	Pass	Pass
+12		+VOUT	Pass	Pass
		GND	Pass	Pass
-12		+VOUT	Pass	Pass
		GND	Pass	Pass
+14		+VOUT	Pass	Pass
		GND	Pass	Pass
-14		+VOUT	Pass	Pass
		GND	Pass	Pass
+16.5		+VOUT	Pass	Pass
		GND	Pass	Pass
-16.5		+VOUT	Pass	Pass
		GND	Pass	Pass

19.2 *Air Discharge, CC1 and CC2, 230 VAC Input*

Discharge	ESD Strike Location	Test Result

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Voltage (kV)			20 V / 3 A
+8	End of Cable	CC1	Pass
		CC2	Pass
-8		CC1	Pass
		CC2	Pass
+10		CC1	Pass
		CC2	Pass
-10		CC1	Pass
		CC2	Pass
+12		CC1	Pass
		CC2	Pass
-12		CC1	Pass
		CC2	Pass
+14		CC1	Pass
		CC2	Pass
-14		CC1	Pass
		CC2	Pass
+16.5		CC1	Pass
		CC2	Pass
-16.5		CC1	Pass
		CC2	Pass
+8	On the Board	CC1	Pass
		CC2	Pass
-8		CC1	Pass
		CC2	Pass
+10		CC1	Pass
		CC2	Pass
-10		CC1	Pass
		CC2	Pass
+12		CC1	Pass
		CC2	Pass
-12		CC1	Pass
		CC2	Pass
+14		CC1	Pass
		CC2	Pass
-14		CC1	Pass
		CC2	Pass
+16.5		CC1	Pass
		CC2	Pass
-16.5		CC1	Pass
		CC2	Pass

19.3 *Contact Discharge, +VOUT and GND, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location	Test Result 5 V / 0 A	Test Result 20 V / 3 A

+8.0	End of Cable	+VOUT	Pass	Pass
		GND	Pass	Pass
-8.0		+VOUT	Pass	Pass
		GND	Pass	Pass
+8.8		+VOUT	Pass	Pass
		GND	Pass	Pass
-8.8		+VOUT	Pass	Pass
		GND	Pass	Pass
+8.0	On the Board	+VOUT	Pass	Pass
		GND	Pass	Pass
-8.0		+VOUT	Pass	Pass
		GND	Pass	Pass
+8.8		+VOUT	Pass	Pass
		GND	Pass	Pass
-8.8		+VOUT	Pass	Pass
		GND	Pass	Pass

19.4 *Contact Discharge, CC1 and CC2, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location		Test Result 20 V / 3 A
+8.0	End of Cable	CC1	Pass[1]
		CC2	Pass[1]
-8.0		CC1	Pass[1]
		CC2	Pass[1]
+8.8		CC1	Pass[1]
		CC2	Pass[1]
-8.8		CC1	Pass[1]
		CC2	Pass[1]

[1]Power supply initiates Auto-Restart due to

- USB-C power adapter tester Tiny-PAT protection at the load

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20 Revision History

Date	Author	Revision	Description & Changes	Reviewed
07-Oct-20	GC	1.0	Initial Release.	Apps & Mktg

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