# Design Example Report

| Title | ***2.7 W StackFET Buck Power Supply Using LinkSwitch<sup>TM</sup>-TN2 LNK3206GQ*** |
|---|---|
| **Specification** | 60 VDC – 950 VDC Input (Withstand 1100 VDC); 18.0 V / 150 mA Output |
| **Application** | Automotive Application |
| **Author** | Applications Engineering Department |
| **Document Number** | DER-719Q |
| **Date** | July 23, 2021 |
| **Revision** | 1.1 |

## Summary and Features

- Automotive graded BOM
- 750 V power MOSFET rating
- Highly integrated solution
- Lowest possible component count
- No optocoupler required for regulation
- 950 VDC input. Can withstand 1100 VDC input
- <±5% load regulation
- 105 ºC ambient temperature operation

## Table of Contents

**Important Note:** Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved.

# 1    Introduction

This engineering report describes a StackFET buck converter designed to provide a non-isolated nominal output voltage of 18 V at 150 mA load from a wide input voltage range of 60 VDC to 950 VDC and can withstand 1100 VDC for automotive application. This power supply utilizes the LNK3206GQ from the LinkSwitch-TN2 family for Automotive of ICs.

This document contains the complete power supply specifications, bill of materials, transformer construction, circuit schematic and printed circuit board layout, along with performance data and electrical waveforms.
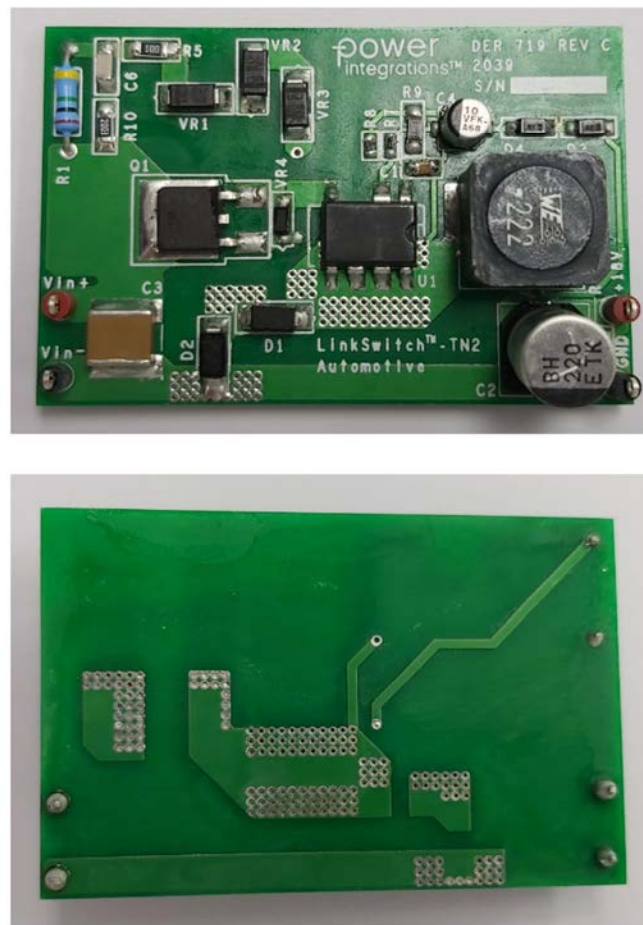




**Figure 1 –** Populated Circuit Board.

## 2    **Power Supply Specification**

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

| Description | Symbol | Min | Typ | Max | Units | Comment |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| Voltage | $V_{IN}$ | 60 | | 950 | VDC | Withstand 1100 VDC Input. |
| **Output1** | | | | | | |
| Output Voltage | $V_{OUT}$ | 17.1 | 18 | 18.9 | V | ± 5% |
| No-Load Output Voltage | $V_{OUT}$ | | | 19.08 | V | Regulation at No-Load. |
| Output Ripple Voltage | $V_{RIPPLE}$ | | | 180 | mV | 20 MHz Bandwidth. |
| Output Current | $I_{OUT}$ | | | 150 | mA | |
| **Total Output Power** | | | | | | |
| Continuous Output Power | $P_{OUT}$ | | | 2.7 | W | |
| **Efficiency** | | | | | | |
| Full Load Efficiency @ 60 $V_{IN}$ | $\eta$ | 73 | | | % | Measured at $P_{OUT}$ 25 $^o$C. |
| Full Load Efficiency @ 360 $V_{IN}$ | $\eta$ | 74 | | | % | Measured at $P_{OUT}$ 25 $^o$C. |
| Full Load Efficiency @ 950 $V_{IN}$ | $\eta$ | 64 | | | % | Measured at $P_{OUT}$ 25 $^o$C. |
| **Environmental** | | | | | | |
| Ambient Temperature | $T_{AMB}$ | 0 | | 105 | $^o$C | Free Convection, Sea Level. |

## 3   Schematic



**Figure 2 –** Schematic.



**Figure 3 –** Test Set-up.

# 4    Circuit Description

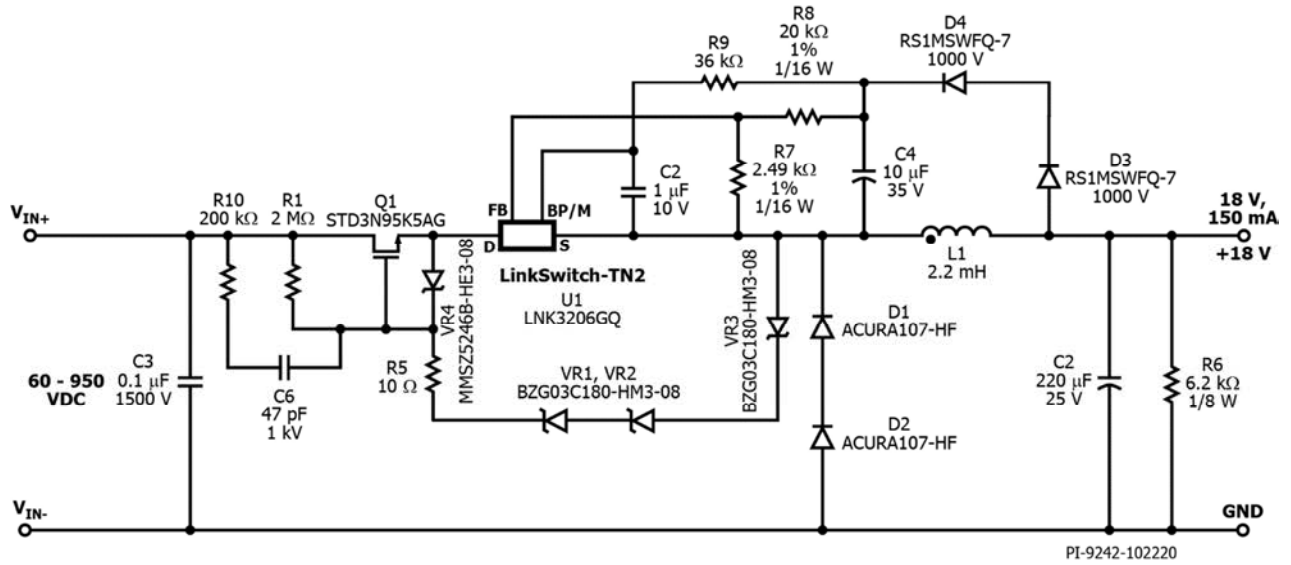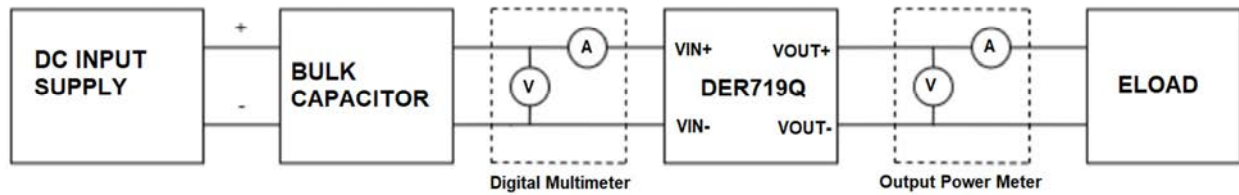The schematic in Figure 2 shows a StackFET buck converter using LNK3206GQ. The circuit provides a non-isolated 18 V, 150 mA continuous output. This configuration enhances its withstanding voltage so that the circuit can be applied with higher input voltage.

In this design, automotive battery will be the intended input source of the buck circuit. To simulate battery stiff voltage source, bulk capacitors were added in the test set-up during the test as shown in Figure 3.

All components selected in this report are automotive compliant.

## 4.1    *Input Filter*

A bypass capacitor C1 is added to provide a local instantaneous charge and a stable DC bus to the buck converter.

## 4.2    *Power Stage*

MOSFET Q1 and LNK3206GQ are arranged in the StackFET configuration. The resistor R1 performs the function of initially turning on the MOSFET, so that the BYPASS pin capacitor can be charged from the input voltage. Resistor R10 and C6 are used to balance the voltage sharing between MOSFET and LNK3206GQ during start-up.

The Zener diodes (VR1, VR2, and VR3) performs dual function in the circuit. It limits the voltage across LNK3206GQ to less than 600 V. It also provides gate current to Q1 (from the charge stored across its junction capacitance) while turning it on and off. Series resistor R5 limits gate charging current so that any tendency of high frequency oscillation can be damped out. Zener VR4 limits the gate to source voltage of Q1.

During normal operation the device is powered from output via a current limiting resistor R9.

The operation of U1 is unaffected by the StackFET configuration. When LNK3206GQ turns on Q1 also turn on, applying the input voltage across the output inductor L1. Once the primary current reaches the internal current limit of LNK3206GQ IC, the MOSFET turns-off. The on-time for each switching cycle is set by the inductance value of L1, LinkSwitch-TN2 auto current limit and the high-voltage DC input bus across C3. Output regulation is accomplished by skipping switching cycles in response to an ON/OFF feedback signal applied to the FEEDBACK (FB) pin. This differs significantly from traditional PWM schemes that control the duty factor (duty cycle) of each switching cycle. Unlike TinySwitch, the logic of the FB pin has been inverted in LinkSwitch-TN. This allows a very simple feedback scheme to be used when the device is used in the buck converter configuration. Current into the FB pin greater than 49 µA will inhibit the switching of the internal MOSFET, while current below this allows switching cycles to occur.

## 4.3   *Output Rectification*

During the ON time of U1, current ramps in L1 and is simultaneously delivered to the load. During the OFF time, the inductor current ramps down via free-wheeling diode D1 and D2 into C2 and is delivered to the load. Diode D1 and D2 should be selected as an ultrafast diode (low $T_{RR}$) due to high ambient temperature operation. To meet 80% diode voltage derating requirement, two freewheeling diode in series was implemented.

Capacitor C2 should be selected to have an adequate ripple current rating (very low ESR type). Please see the spreadsheet output capacitor section.

## 4.4   *Output Feedback*

The voltage across L1 is rectified and smoothed by D3, D4, and C4 during the off-time of U1. To provide a feedback signal, the voltage developed across C4 is divided by R7 and R8 and connected to U1's FB pin. The values of R7 and R8 are selected such that at the nominal output voltage, the voltage on the FB pin is 2 V. Resistor R7 and R8 can be optimized for better output voltage regulation and efficiency. This voltage is specified for U1 at an FB pin current of 49 $\mu$A. This allows simple feedback to meet the required overall output tolerance of ±5% at rated output current.

## 4.5   *PCB*

Printed Circuit Board (PCB) should be rigid enough to survive the harsh environment of automotive application. FR-4 High Tg PCB material was used in the design.

## 5   **PCB Layout**

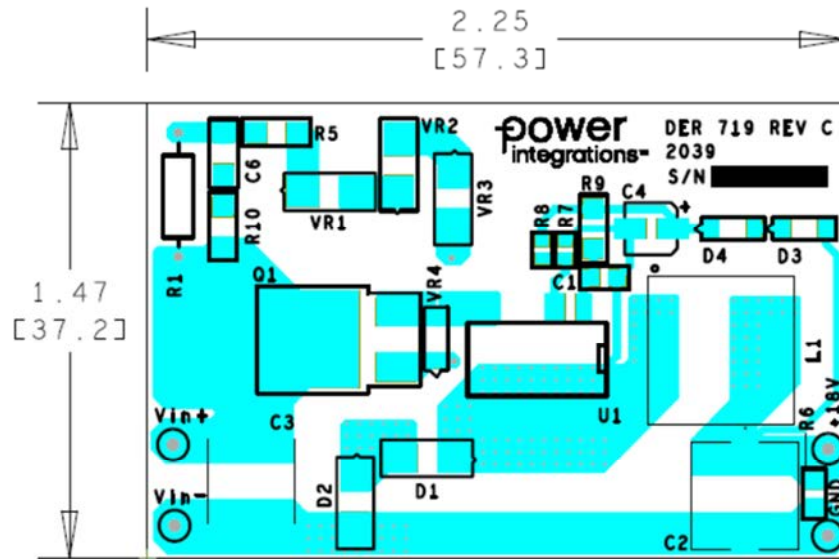PCB copper thickness is 2oz. PCB thickness is 1 mm. PCB Material FR4 High Tg 170.
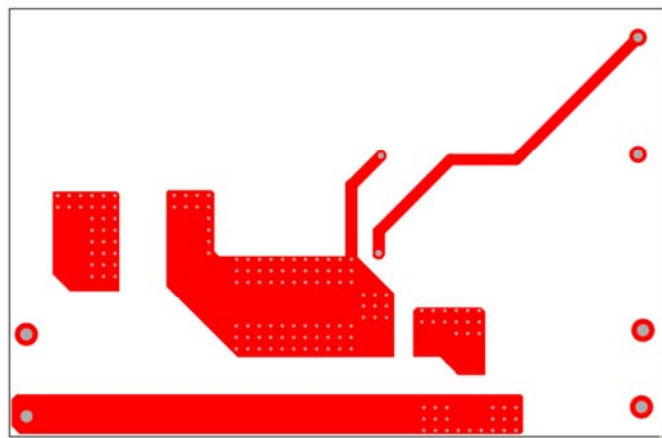


**Figure 4 –** Printed Circuit Board, Top View.



**Figure 5 –** Printed Circuit Board, Bottom View.

## 6    **Bill of Materials**

| Item | Qty | Ref Des | Description | Mfg Part Number | Mfg |
|---|---|---|---|---|---|
| 1 | 1 | C1 | 1 µF ±10% 10 V Ceramic X7R 0805 | C0805C105K8RACAUTO | Kemet |
| 2 | 1 | C2 | 220 µF, 20%, 25 V, Electrolytic, (8.30 mm x 8.30 mm), SMD | 25TKV220M8X10.5 | Rubycon |
| 3 | 1 | C3 | 0.1 µF ±10% 1500 V (1.5kV) Ceramic X7R 2225 | C2225C104KFRACAUTO | Kemet |
| 4 | 1 | C4 | 10 µF, 20%, 35V, Electrolytic, (4.30 mm x 4.30 mm), SMD | EEE-FK1V100UR | Panasonic |
| 5 | 1 | C6 | 47 pF,10000 pF, ±5%, 1000 V, Ceramic,C0G_NP0, 1206 | C1206C470JDGACAUTO | KEMET |
| 6 | 1 | D1 | Diode, Ultrafast Recovery, 1000 V, 1 A, Surface Mount, DO-214AC (SMA) | ACURA107-HF | Comchip |
| 7 | 1 | D2 | Diode, Ultrafast Recovery, 1000 V, 1 A, Surface Mount, DO-214AC (SMA) | ACURA107-HF | Comchip |
| 8 | 1 | D3 | Diode Standard, Fast Recovery, 1000 V 1 A SMT SOD-123F | RS1MSWFQ-7 | Diodes, Inc. |
| 9 | 1 | D4 | Diode Standard, Fast Recovery, 1000 V 1 A SMT SOD-123F | RS1MSWFQ-7 | Diodes, Inc. |
| 10 | 1 | L1 | 2.2 mH Shielded Wirewound Inductor 530 mA 3.75Ω Max Nonstandard (12 x 12 mm) | 7447709222 | Wurth |
| 11 | 1 | Q1 | N-Channel C 2A (Tc) 45 W (Tc) SMT, DPAK, TO-252-3, DPak (2 Leads + Tab), SC-63 | STD3N95K5AG | ST Micro |
| 12 | 1 | R1 | RES, 2 MΩ, ±5%, ¼ W Through Hole, Axial, High-Voltage, Pulse Withstanding Metal Film | VR25000002004JR500 | Vishay |
| 13 | 1 | R5 | RES, 10 Ω, 5%, 1/4 W, Thick Film, 1206 | ERJ-8GEYJ100V | Panasonic |
| 14 | 1 | R6 | RES, 6.2 kΩ, 5%, 1/8 W, Thick Film, 0805 | ERJ-6GEYJ622V | Panasonic |
| 15 | 1 | R7 | RES, 2.49 kΩ, 1%, 1/16 W, Thick Film, 0603 | ERJ-3EKF2491V | Panasonic |
| 16 | 1 | R8 | RES, 20 kΩ, 1%, 1/16 W, Thick Film, 0603 | ERJ-3EKF2002V | Panasonic |
| 17 | 1 | R9 | RES, 36 kΩ, 5%, 1/4 W, Thick Film, 1206 | ERJ-8GEYJ363V | Panasonic |
| 18 | 1 | R10 | RES, 200 kΩ, 5%, 1/4 W, Thick Film, 1206 | ERJ-8GEYJ204V | Panasonic |
| 19 | 1 | U1 | LinkSwitch-TN2, SMD-8C | LNK3206GQ | Power Integrations |
| 20 | 1 | VR1 | Zener Diode 180 V 1.25 W ±6.39% SMT DO-214AC (SMA) | BZG03C180-HM3-08 | Vishay |
| 21 | 1 | VR2 | Zener Diode 180 V 1.25 W ±6.39% SMT DO-214AC (SMA) | BZG03C180-HM3-08 | Vishay |
| 22 | 1 | VR3 | Zener Diode 180 V 1.25 W ±6.39% SMT DO-214AC (SMA) | BZG03C180-HM3-08 | Vishay |
| 23 | 1 | VR4 | Zener Diode 16 V 500 mW ±5% SMT SOD-123 | MMSZ5246B-HE3-08 | Vishay |

### **Miscellaneous**

| Item | Qty | Ref Des | Description | Mfg Part Number | Mfg |
|---|---|---|---|---|---|
| 1 | 1 | +18V | Test Point, RED, Miniature THRU-HOLE MOUNT | 5000 | Keystone |
| 2 | 1 | GND | Test Point, BLK, Miniature THRU-HOLE MOUNT | 5001 | Keystone |
| 3 | 1 | VIN+ | Test Point, RED, Miniature THRU-HOLE MOUNT | 5000 | Keystone |
| 4 | 1 | VIN- | Test Point, BLK, Miniature THRU-HOLE MOUNT | 5001 | Keystone |

## 7    Design Spreadsheet

| DCDC_LinkSwitchTN2-Automotive-Buck_080320; Rev.1.1; Copyright Power Integrations 2020 | INPUT | INFO | OUTPUT | UNIT | DCDC LinkSwitchTN2-Automotive Buck |
|---|---|---|---|---|---|
| **ENTER APPLICATION VARIABLES** | | | | | |
| VDCMIN | 60.00 | | 60.00 | V | Minimum DC voltage |
| VDCMAX | 950.00 | Info | 950.00 | V | Entered maximum DC voltage exceeds device datasheet recommendation. Decrease the value to less than or equal to 550V |
| VOUT | 18.00 | | 18.00 | V | Output voltage |
| IOUT | 0.150 | | 0.150 | A | Average output current |
| EFFICIENCY_ESTIMATED | | | 0.80 | | Efficiency estimate at output terminals |
| EFFICIENCY_CALCULATED | | | 0.78 | | Calculated efficiency based on real components and operating point |
| POUT | | | 2.70 | W | Continuous output power |
| INPUT STAGE RESISTANCE | | | 10 | Ohms | Input stage resistance in ohms (includes thermistor, filtering components, etc) |
| PLOSS_INPUTSTAGE | | | 0.032 | W | Maximum input stage loss |
| **ENTER LINKSWITCH-TN2-AUTOMOTIVE VARIABLES** | | | | | |
| OPERATION MODE | | | MDCM | | Mostly discontinuous mode of operation |
| CURRENT LIMIT MODE | RED | | RED | | Choose 'RED' for reduced current limit or 'STD' for standard current limit |
| PACKAGE | | | SMD-8C | | Select the device package |
| DEVICE SERIES | | | LNK3206 | | Generic LinkSwitch-TN2 device |
| DEVICE CODE | | | LNK3206GQ | | Required LinkSwitch-TN2 device |
| ILIMITMIN | | | 0.325 | A | Minimum current limit of the device |
| ILIMITTYP | | | 0.370 | A | Typical current limit of the device |
| ILIMITMAX | | | 0.415 | A | Maximum current limit of the device |
| RDSON | | | 15.50 | ohms | Primary switch on-time drain to source resistance at 125degC |
| FSMIN | | | 62000 | Hz | Minimum switching frequency |
| FSTYP | | | 66000 | Hz | Typical switching frequency |
| FSMAX | | | 70000 | Hz | Maximum switching frequency |
| BVDSS | | | 750 | V | Device breakdown voltage |
| **PRIMARY SWITCH PARAMETERS** | | | | | |
| VDSON | | | 2.00 | V | Primary switch on-time drain to source voltage estimate |
| VDSOFF | | Warning | 998 | V | Drain voltage stress exceeds breakdown voltage of device. Decrease maximum DC input voltage |
| DUTY | | | 0.325 | | Maximum duty cycle |
| TIME_ON_MIN | | | 0.821 | us | Primary switch minimum on-time |
| IPED_PRIMARYSWITCH | | | 0.000 | A | Maximum primary switch pedestal current |
| IRMS_PRIMARYSWITCH | | | 0.116 | A | Maximum primary switch RMS current |
| PLOSS_PRIMARYSWITCH | | | 0.273 | W | Maximum primary switch loss |
| **BUCK INDUCTOR PARAMETERS** | | | | | |
| INDUCTANCE_MIN | | | 1980 | uH | Minimum design inductance required for current delivery. Note that the chosen inductor must be AEC-Q200 compliant |
| INDUCTANCE_TYP | 2200 | | 2200 | uH | Typical design inductance required for current delivery. Note that the chosen inductor must be AEC-Q200 compliant |
| INDUCTANCE_MAX | | | 2420 | uH | Maximum design inductance required for current delivery. Note that the chosen inductor must be AEC-Q200 compliant |
| TOLERANCE_INDUCTANCE | 10 | | 10 | % | Tolerance of the design inductance |
| DC RESISTANCE OF INDUCTOR | | | 2.0 | ohms | DC resistance of the buck inductor |
| FACTOR_KLOSS | | | 0.50 | | Factor that accounts for "off-state" power loss to be supplied by inductor (usually between 50% to 66%) |

| | | | | | |
|---|---|---|---|---|---|
| IRMS_INDUCTOR | | | 0.222 | A | Maximum inductor RMS current |
| PLOSS_INDUCTOR | | | 0.098 | W | Maximum inductor losses |
| **FREEWHEELING DIODE PARAMETERS** | | | | | |
| VF_FREEWHEELING | | | 2.50 | V | Forward voltage drop across the two freewheeling diodes in series |
| PIV_RATING | | | 600.00 | V | Peak inverse voltage rating of each freewheeling diode |
| TRR | | | 25 | ns | Reverse recovery time of each freewheeling diode |
| PIV_CALCULATED | | Info | 998 | V | Combined PIV ratings of two diodes should meet 80% voltage derating requirement |
| IRMS_DIODE | | | 0.219 | A | Maximum diode RMS current |
| PLOSS_DIODE | | | 0.390 | W | Maximum loss across both freewheeling diodes |
| RECOMMENDED DIODE | UF1JLW | | UF1JLW | | Recommended freewheeling diode. Two of this diode in series must be implemented to pass 80% voltage derating and thermal requirements |
| **BIAS/FEEDBACK PARAMETERS** | | | | | |
| VF_BIAS | | | 0.70 | V | Forward voltage drop of the bias diode |
| RBIAS | | | 2490 | Ohms | Bias resistor |
| CBP | | | 1.0 | uF | BP pin capacitor |
| RFB | | | 21000 | Ohms | Feedback resistor |
| CFB | | | 10 | uF | Feedback capacitor |
| C_SOFTSTART | | | 1-10 | uF | If the output voltage is greater than 12 V or total output and system capacitance is greater than 100 uF, a soft start capacitor between 1uF and 10 uF is recommended |
| PLOSS_FEEDBACK | | | 0.014 | W | Maximum feedback component losses |
| **OUTPUT CAPACITOR** | | | | | |
| OUTPUT VOLTAGE RIPPLE | | | 360 | mV | Desired output voltage ripple |
| IRMS_COUT | | | 0.163 | A | Maximum output capacitor RMS current |
| PLOSS_COUT | | | 0.031 | W | Maximum output capacitor power loss |
| ESR_COUT | | | 1153 | mOhms | ESR of the output capacitor |
| | | | | | |
| | | | | | |

**Notes:**

1) VDSOFF warning was address by using a Stack Fet Buck topology. Stack Fet Buck topology will limit the Vds of the LNK3206GQ to a safe level.

2) Freewheeling diode PIV info was addressed by using two 1000V rated diodes in series.

# 8    Performance Data

## 8.1    *Efficiency*

### 8.1.1    Line Efficiency

Test Condition: Soak for 10 minutes for each line.
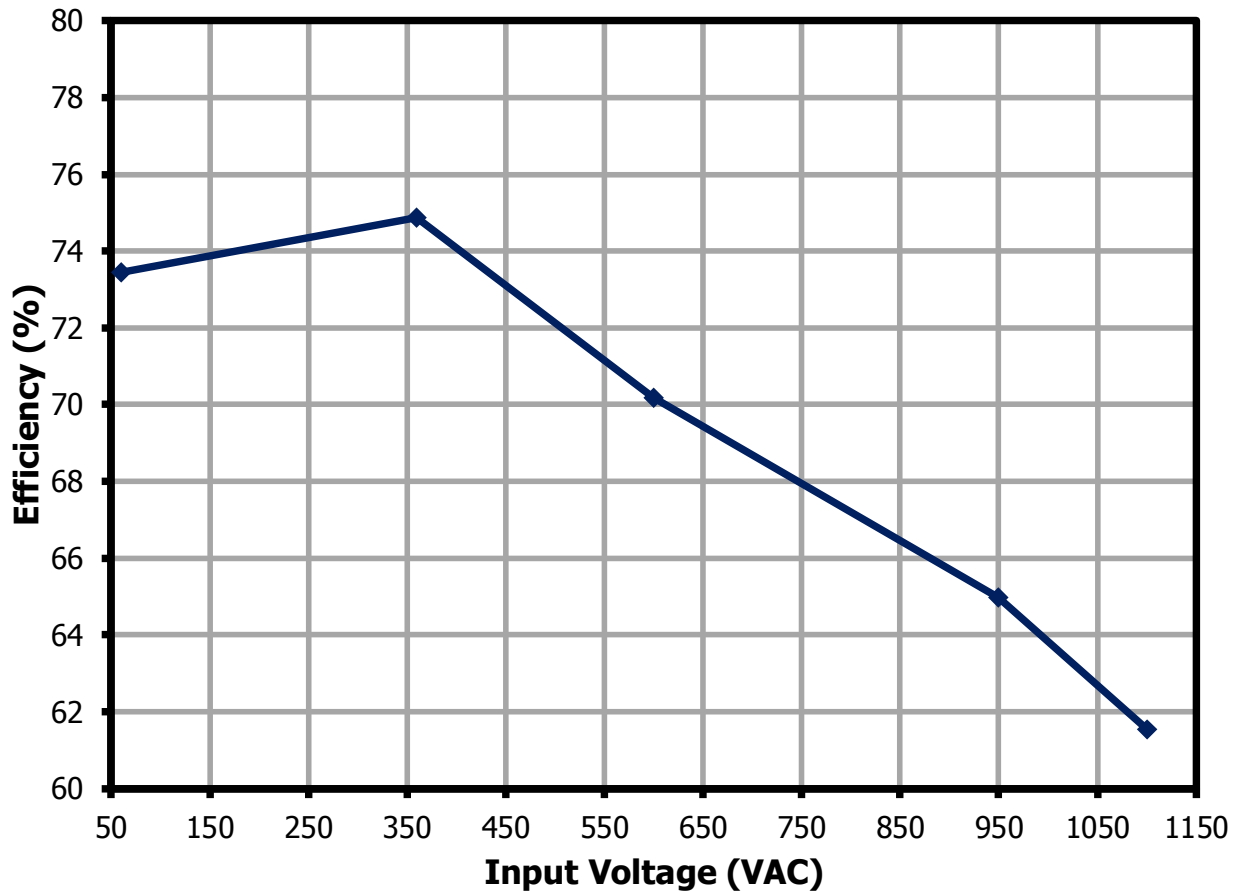


**Figure 6 –** Efficiency vs. Input Voltage.

### 8.1.2    Load Efficiency

Test Condition: Soak for 10 minutes, 5 minutes delay per each line, and 10 sec. delay for each load
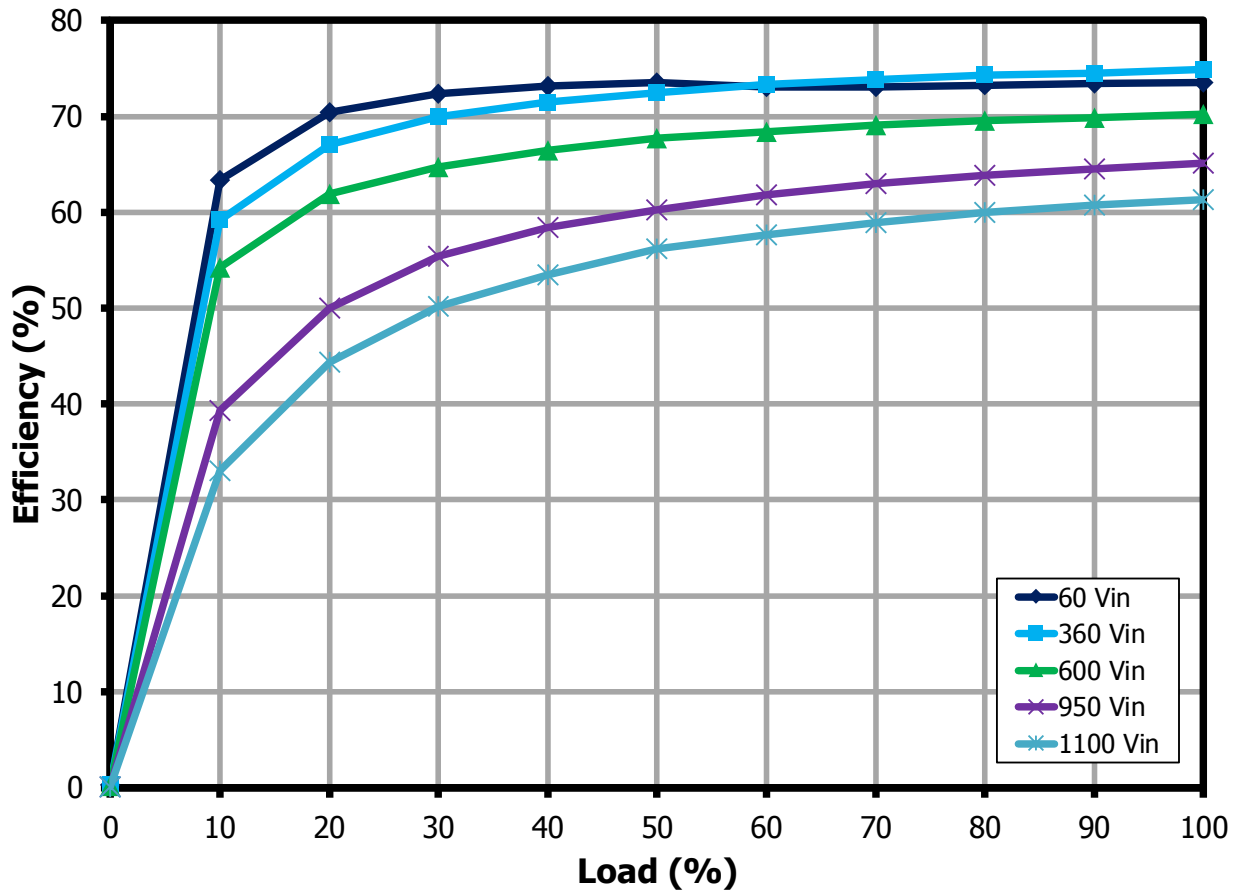


**Figure 7 –** Efficiency vs. Percentage Load.

## 8.2 *Line Regulation*

Test Condition: Soak for 10 minutes for each line.
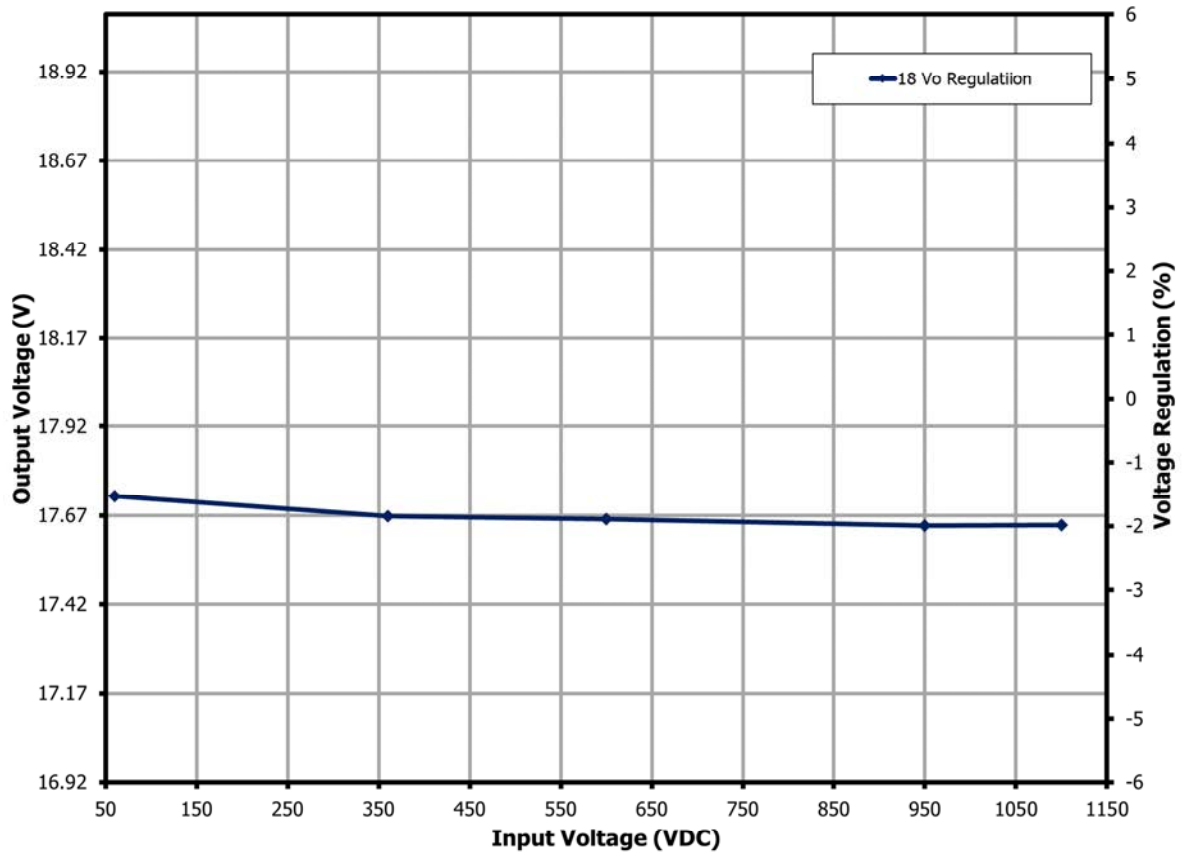


**Figure 8 –** Output Voltage vs. Input Voltage.

## 8.3  *Load Regulation*

Test Condition: Soak for 10 minutes, 5 minutes delay per each line, and 10 sec. delay for each load
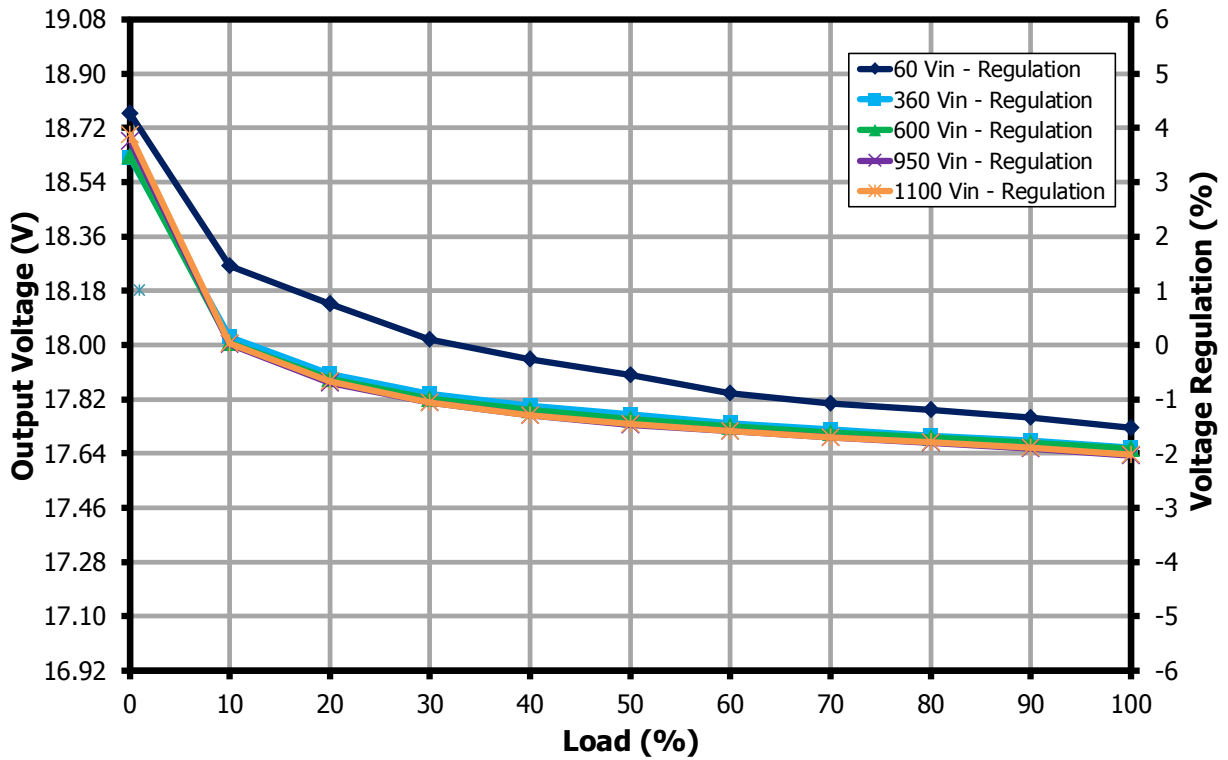


**Figure 9 –** Output Voltage vs. Percent Load.

## 9    Waveforms

### 9.1    *Load Transient Response*

Test Condition: Dynamic load frequency = 1 kHz, Duty cycle = 50 %
Slew Rate = 0.8 A / µs

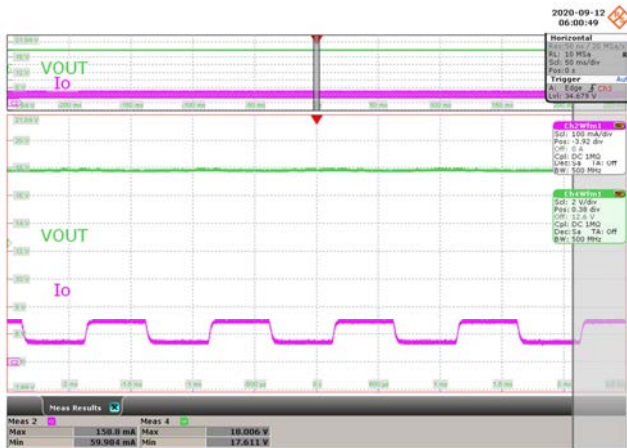#### 9.1.1    18 V Transient 0% - 100% Load Change
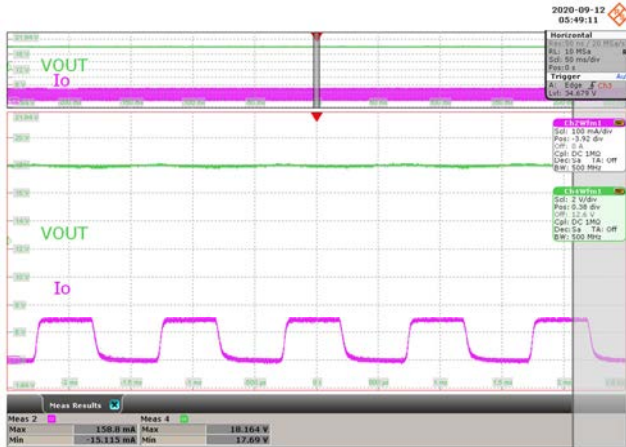
**Figure 10 –** 60 VDC Input.
CH2: $I_{OUT}$, 100 mA / div., 50 ms / div.
CH4: $V_{OUT}$, 2 V / div., 50 ms / div.
Zoom: 500 µs / div.
$V_{OUT(MAX)}$ = 18.164 V, $V_{OUT(MIN)}$ = 17.69 V.
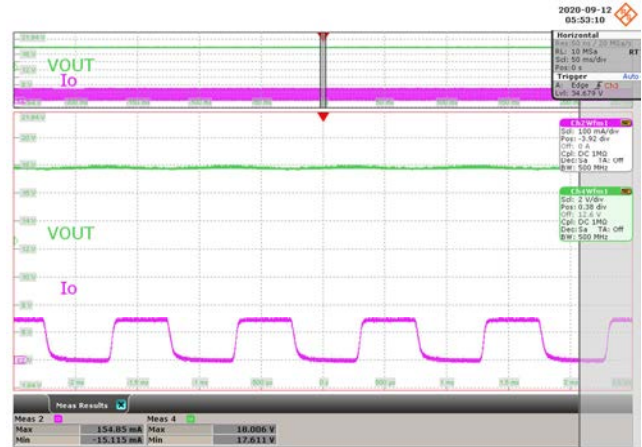
**Figure 11 –** 360 VDC Input.
CH2: $I_{OUT}$, 100 mA / div., 50 ms / div.
CH4: $V_{OUT}$, 2 V / div., 50 ms / div.
Zoom: 500 µs / div.
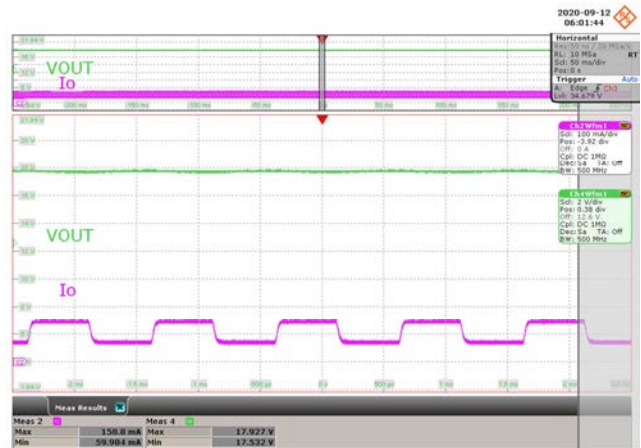$V_{OUT(MAX)}$ = 18.006 V, $V_{OUT(MIN)}$ = 17.611 V.

**Figure 12 –** 600 VDC Input.
CH2: $I_{OUT}$, 100 mA / div., 50 ms / div.
CH4: $V_{OUT}$, 2 V / div., 50 ms / div.
Zoom: 500 µs / div.
$V_{OUT(MAX)}$ = 18.006 V, $V_{OUT(MIN)}$ = 17.532 V.

**Figure 13 –** 950 VDC Input.
CH2: $I_{OUT}$, 100 mA / div., 50 ms / div.
CH4: $V_{OUT}$, 2 V / div., 50 ms / div.
Zoom: 500 µs / div.
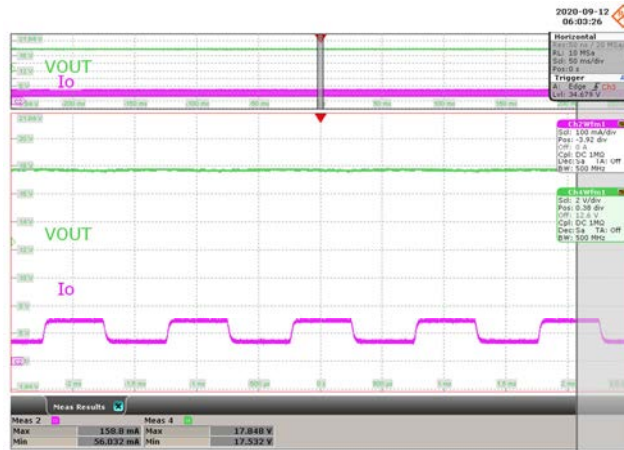$V_{OUT(MAX)}$ = 17.927 V, $V_{OUT(MIN)}$ = 17.532 V.

**Figure 14 –** 1100 VDC Input.
CH2: I$_{OUT,}$ 100 mA / div., 50 ms / div.
CH4: V$_{OUT,}$ 2 V / div., 50 ms / div.
Zoom: 500 µs / div.
V$_{OUT(MAX)}$ = 17.927 V, V$_{OUT(MIN)}$ = 17.532 V.

### 9.1.2    18 V Transient 10% - 100% Load Change
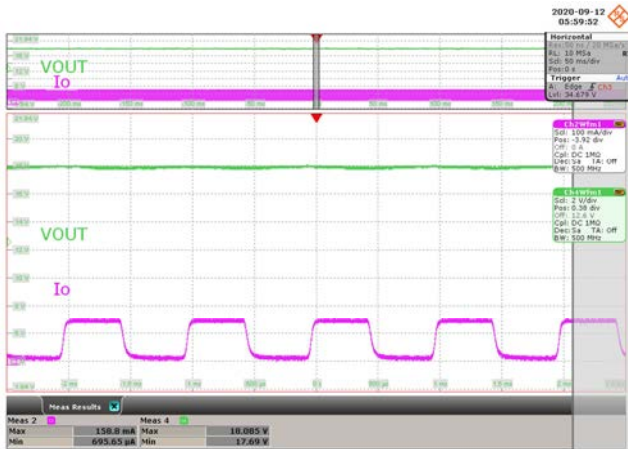




**Figure 15 –** 60 VDC Input.
CH2: I$_{OUT,}$ 100 mA / div., 50 ms / div.
CH4: V$_{OUT,}$ 2 V / div., 50 ms / div.
Zoom: 500 µs / div.
V$_{OUT(MAX)}$ = 18.085 V, V$_{OUT(MIN)}$ = 17.69 V.
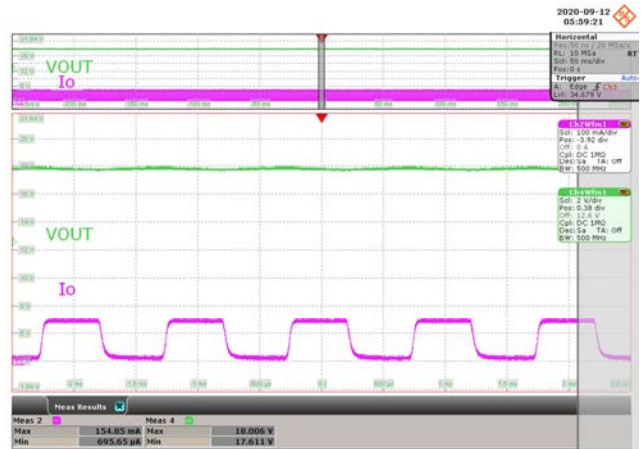
**Figure 16 –** 360 VDC Input.
CH2: I$_{OUT,}$ 100 mA / div., 50 ms / div.
CH4: V$_{OUT,}$ 2 V / div., 50 ms / div.
Zoom: 500 µs / div.
V$_{OUT(MAX)}$ = 18.006 V, V$_{OUT(MIN)}$ = 17.611 V.

**Figure 17 –** 600 VDC Input.
CH2: I_OUT, 100 mA / div., 50 ms / div.
CH4: V_OUT, 2 V / div., 50 ms / div.
Zoom: 500 µs / div.
$V_{OUT(MAX)}$ = 18.006 V, $V_{OUT(MIN)}$ = 17.532 V.



**Figure 18 –** 950 VDC Input.
CH2: I_OUT, 100 mA / div., 50 ms / div.
CH4: V_OUT, 2 V / div., 50 ms / div.
Zoom: 500 µs / div.
$V_{OUT(MAX)}$ = 17.927 V, $V_{OUT(MIN)}$ = 17.532 V.



**Figure 19 –** 1100 VDC Input.
CH2: I_OUT, 100 mA / div., 50 ms / div.
CH4: V_OUT, 2 V / div., 50 ms / div.
Zoom: 500 µs / div.
$V_{OUT(MAX)}$ = 17.927 V, $V_{OUT(MIN)}$ = 17.532 V.

### 9.1.3    18 V Transient 50% - 100% Load Change



**Figure 20 –** 60 VDC Input.
CH2: I$_{OUT,}$ 100 mA / div., 50 ms / div.
CH4: V$_{OUT,}$ 2 V / div., 50 ms / div.
Zoom: 500 µs / div.
V$_{OUT(MAX)}$ = 18.006 V, V$_{OUT(MIN)}$ = 17.611 V.



**Figure 21 –** 360 VDC Input.
CH2: I$_{OUT,}$ 100 mA / div., 50 ms / div.
CH4: V$_{OUT,}$ 2 V / div., 50 ms / div.
Zoom: 500 µs / div.
V$_{OUT(MAX)}$ = 17.927 V, V$_{OUT(MIN)}$ = 17.532 V.



**Figure 22 –** 600 VDC Input.
CH2: I$_{OUT,}$ 100 mA / div., 50 ms / div.
CH4: V$_{OUT,}$ 2 V / div., 50 ms / div.
Zoom: 500 µs / div.
V$_{OUT(MAX)}$ = 17.927 V, V$_{OUT(MIN)}$ = 17.532 V.



**Figure 23 –** 950 VDC Input.
CH2: I$_{OUT,}$ 100 mA / div., 50 ms / div.
CH4: V$_{OUT,}$ 2 V / div., 50 ms / div.
Zoom: 500 µs / div.
V$_{OUT(MAX)}$ = 17.848 V, V$_{OUT(MIN)}$ = 17.532 V.

**Figure 24 –** 1100 VDC Input.
CH2: $I_{OUT}$, 100 mA / div., 50 ms / div.
CH4: $V_{OUT}$, 2 V / div., 50 ms / div.
Zoom: 500 $\mu$s / div.
$V_{OUT(MAX)}$ = 17.848 V, $V_{OUT(MIN)}$ = 17.532 V.

## 9.2    *Switching Waveforms*

### 9.2.1        Primary MOSFET $V_{DS}$ and $I_{DS}$ at Normal Operation
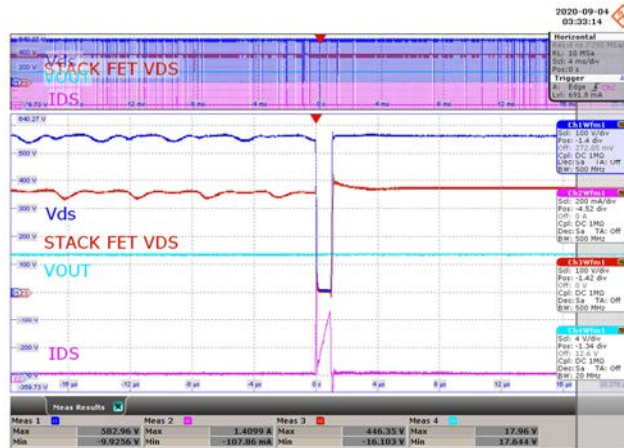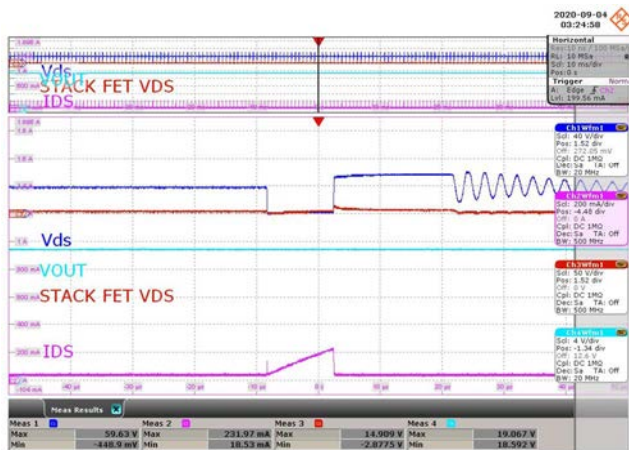
#### 9.2.1.1    Full Load
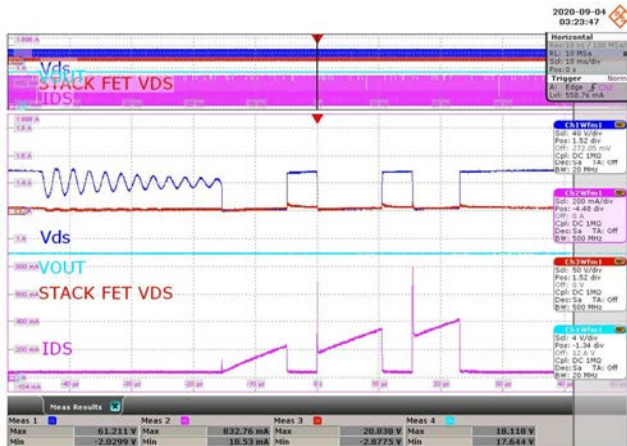


**Figure 25 –** 60 VDC Input.
CH1: IC $V_{DS,}$ 40 V / div., 10 ms / div.
Ch2: $I_{DS}$, 200 mA / div.,10 ms / div.
CH3: FET $V_{DS}$, 50 V / div., 10 ms / div.
Ch4: $V_{OUT}$, 4 V / div., 10 ms / div.
IC $V_{DS(MAX)}$ = 61.21 V, $I_{DS(MAX)}$ = 832.76 mA.
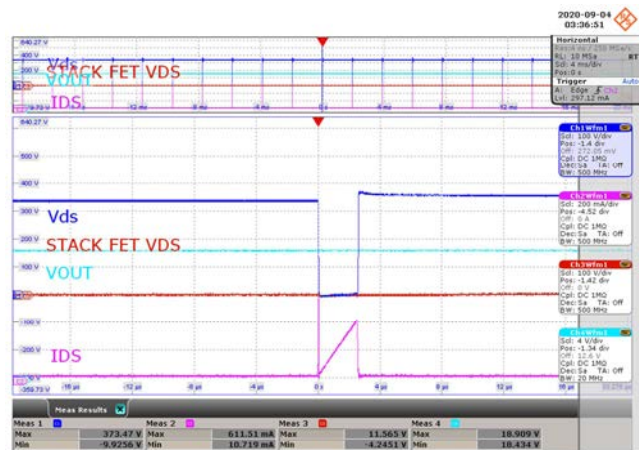Stack FET $V_{DS(MAX)}$ = 20.83 V.
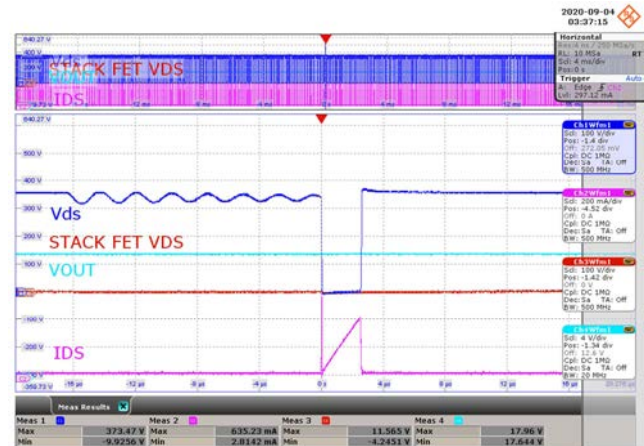


**Figure 26 –** 360 VDC Input.
CH1: IC $V_{DS,}$ 100 V / div., 4 ms / div.
Ch2: $I_{DS}$, 200 mA / div., 4 ms / div.
CH3: FET $V_{DS}$, 100 V / div., 4 ms / div.
Ch4: $V_{OUT}$, 4 V / div., 4 ms / div.
IC $V_{DS(MAX)}$ = 373.47 V, $I_{DS(MAX)}$ = 635.23 mA.
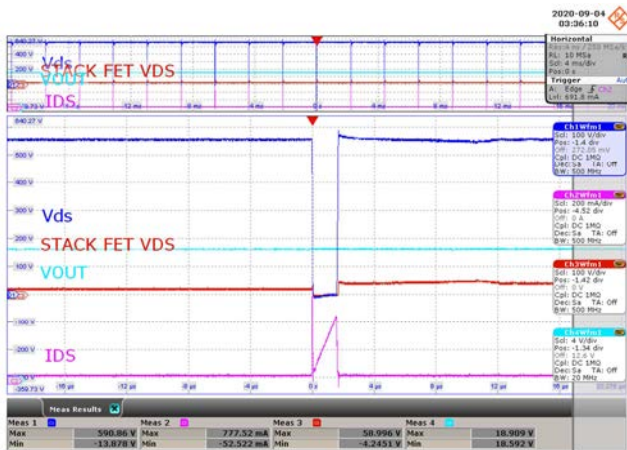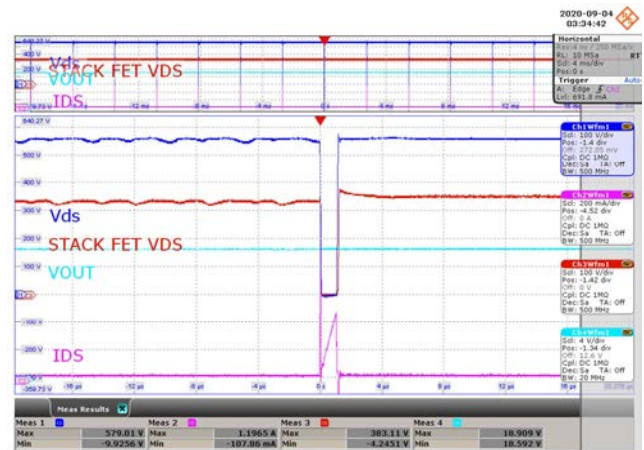Stack FET $V_{DS(MAX)}$ = 11.56 V.
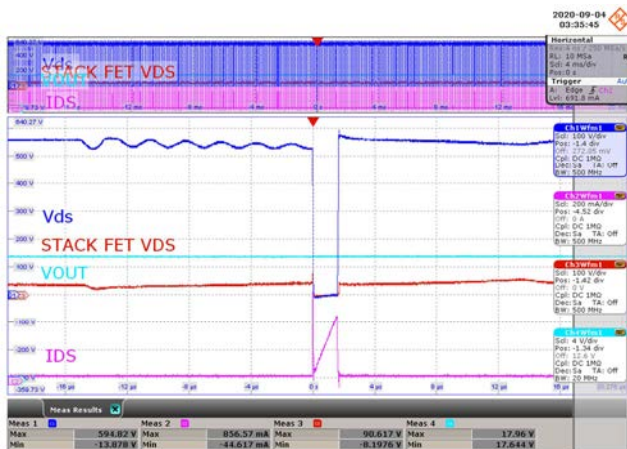


**Figure 27 –** 600 VDC Input.
CH1: IC $V_{DS,}$ 100 V / div., 4 ms / div.
Ch2: $I_{DS}$, 200 mA / div., 4 ms / div.
CH3: FET $V_{DS}$, 100 V / div., 4 ms / div.
Ch4: $V_{OUT}$, 4 V / div., 4 ms / div.
IC $V_{DS(MAX)}$ = 594.82 V, $I_{DS(MAX)}$ = 856.57 mA.
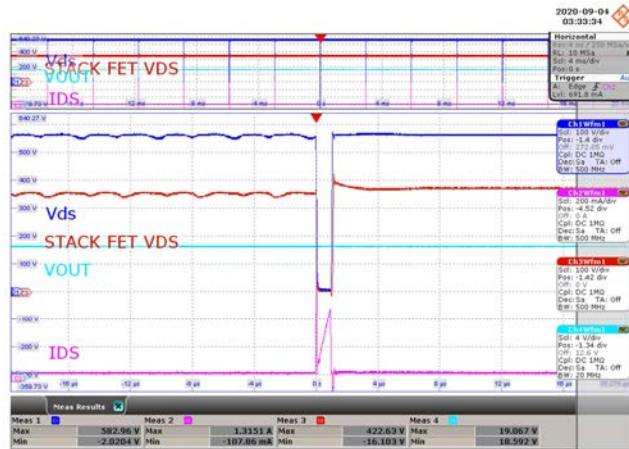Stack FET $V_{DS(MAX)}$ = 90.617 V.
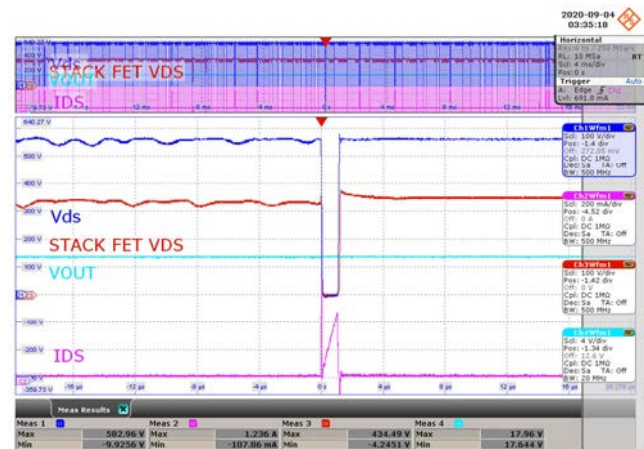


**Figure 28 –** 950 VDC Input.
CH1: IC $V_{DS,}$ 100 V / div., 4 ms / div.
Ch2: $I_{DS}$, 200 mA / div., 4 ms / div.
CH3: FET $V_{DS}$, 100 V / div., 4 ms / div.
Ch4: $V_{OUT}$, 4 V / div., 4 ms / div.
IC $V_{DS(MAX)}$ = 582.96 V, $I_{DS(MAX)}$ = 1.23 A.
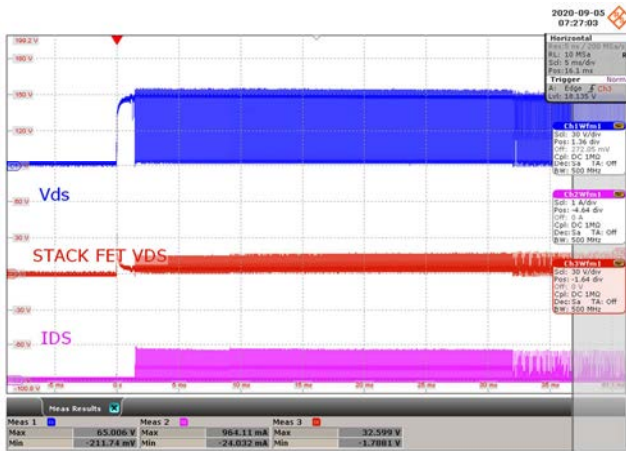Stack FET $V_{DS(MAX)}$ = 434.49 V.

**Figure 29 –** 1100 VDC Input.
CH1: IC $V_{DS}$, 100 V / div., 4 ms / div.
Ch2: $I_{DS}$, 200 mA / div., 4 ms / div.
CH3: FET $V_{DS}$, 100 V / div., 4 ms / div.
Ch4: $V_{OUT}$, 4 V / div., 4 ms / div.
IC $V_{DS(MAX)}$ = 582.96 V, $I_{DS(MAX)}$ = 1.40 A.
Stack FET $V_{DS(MAX)}$ = 446.35 V.

## 9.2.1.2   No-Load





**Figure 30 –** 60 VDC Input.
CH1: IC $V_{DS}$, 40 V / div., 10 ms / div.
Ch2: $I_{DS}$, 200 mA / div.,10 ms / div.
CH3: FET $V_{DS}$, 50 V / div., 10 ms / div.
Ch4: $V_{OUT}$, 4 V / div., 10 ms / div.
IC $V_{DS(MAX)}$ = 59.63 V, $I_{DS(MAX)}$ = 231.97 mA.
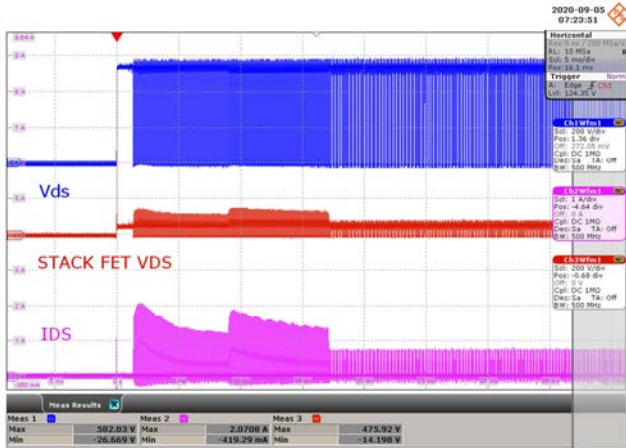Stack FET $V_{DS(MAX)}$ = 14.909 V.

**Figure 31 –** 360 VDC Input.
CH1: IC $V_{DS}$, 100 V / div., 4 ms / div.
Ch2: $I_{DS}$, 200 mA / div., 4 ms / div.
CH3: FET $V_{DS}$, 100 V / div., 4 ms / div.
Ch4: $V_{OUT}$, 4 V / div., 4 ms / div.
IC $V_{DS(MAX)}$ = 373.47 V, $I_{DS(MAX)}$ = 611.51 mA.
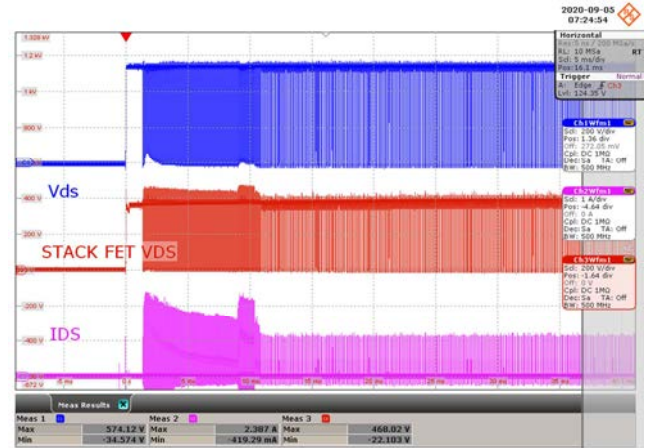Stack FET $V_{DS(MAX)}$ = 11.565 V.

**Figure 32 –** 600 VDC Input.
CH1: IC $V_{DS,}$ 100 V / div., 4 ms / div.
Ch2: $I_{DS}$, 200 mA / div., 4 ms / div.
CH3: FET $V_{DS}$, 100 V / div., 4 ms / div.
Ch4: $V_{OUT}$, 4 V / div., 4 ms / div.
IC $V_{DS(MAX)}$ = 590.86 V, $I_{DS(MAX)}$ = 777.52 mA.
Stack FET $V_{DS(MAX)}$ = 58.996 V.



**Figure 33 –** 950 VDC Input.
CH1: IC $V_{DS,}$ 100 V / div., 4 ms / div.
Ch2: $I_{DS}$, 200 mA / div., 4 ms / div.
CH3: FET $V_{DS}$, 100 V / div., 4 ms / div.
Ch4: $V_{OUT}$, 4 V / div., 4 ms / div.
IC $V_{DS(MAX)}$ = 579.01 V, $I_{DS(MAX)}$ = 1.1965 A.
Stack FET $V_{DS(MAX)}$ = 383.11 V.



**Figure 34 –** 1100 VDC Input.
CH1: IC $V_{DS,}$ 100 V / div., 4 ms / div.
Ch2: $I_{DS}$, 200 mA / div., 4 ms / div.
CH3: FET $V_{DS}$, 100 V / div., 4 ms / div.
Ch4: $V_{OUT}$, 4 V / div., 4 ms / div.
IC $V_{DS(MAX)}$ = 582.96 V, $I_{DS(MAX)}$ = 1.3151 A.
Stack FET $V_{DS(MAX)}$ = 422.63 V.

### 9.2.2    Primary MOSFET $V_{DS}$ and $I_{DS}$ at Start-up Operation
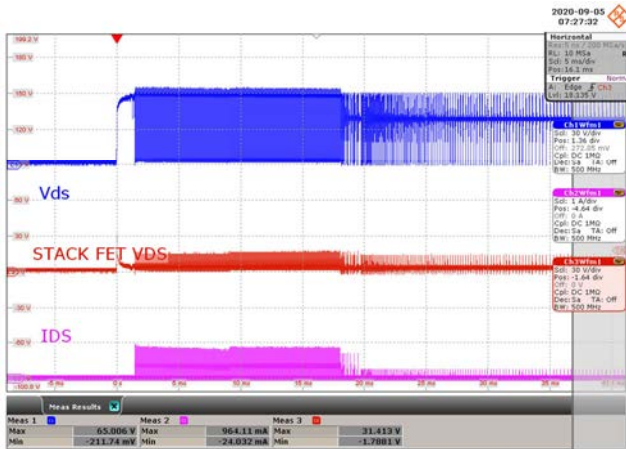
### 9.2.2.1    Full Load



**Figure 35 –** 60 VDC Input.
CH1: IC $V_{DS}$, 30 V / div., 5 ms / div.
Ch2: $I_{DS}$, 1 A / div., 5 ms / div.
CH3: FET $V_{DS}$, 30 V / div., 5 ms / div.
IC $V_{DS(MAX)}$ = 65.00 V, $I_{DS(MAX)}$ = 964.11 mA.
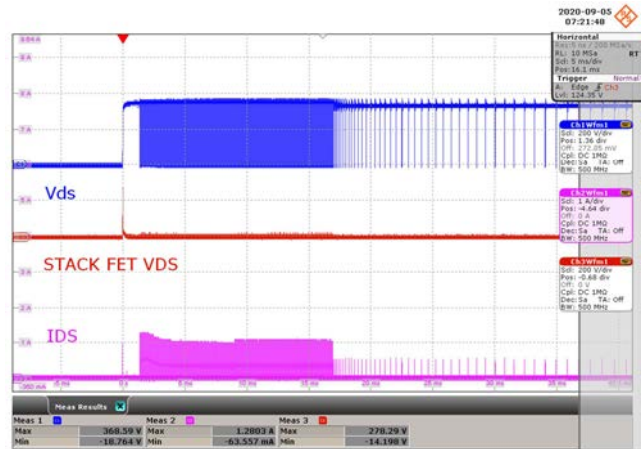Stack FET $V_{DS(MAX)}$ = 32.59 V.
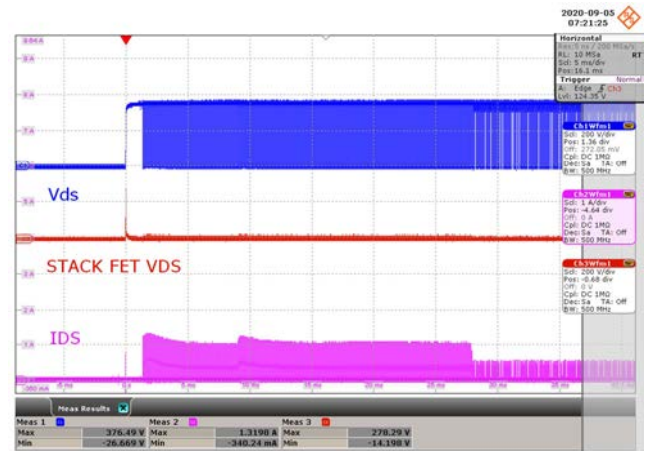


**Figure 36 –** 360 VDC Input.
CH1: IC $V_{DS}$, 200 V / div., 5 ms / div.
Ch2: $I_{DS}$, 1 A / div., 5 ms / div.
CH3: FET $V_{DS}$, 200 V / div., 5 ms / div.
IC $V_{DS(MAX)}$ = 376.49 V, $I_{DS(MAX)}$ = 1.3198 A.
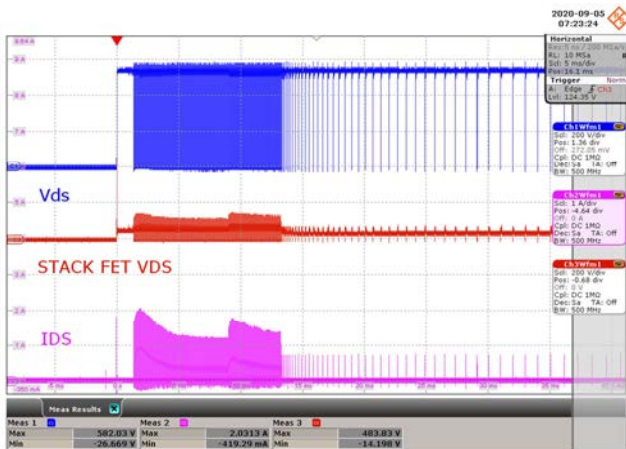Stack FET $V_{DS(MAX)}$ = 278.29 V.



**Figure 37 –** 600 VDC Input.
CH1: IC $V_{DS}$, 200 V / div., 5 ms / div.
Ch2: $I_{DS}$, 1 A /div., 5 ms / div.
CH3: FET $V_{DS}$, 200 V / div., 5 ms / div.
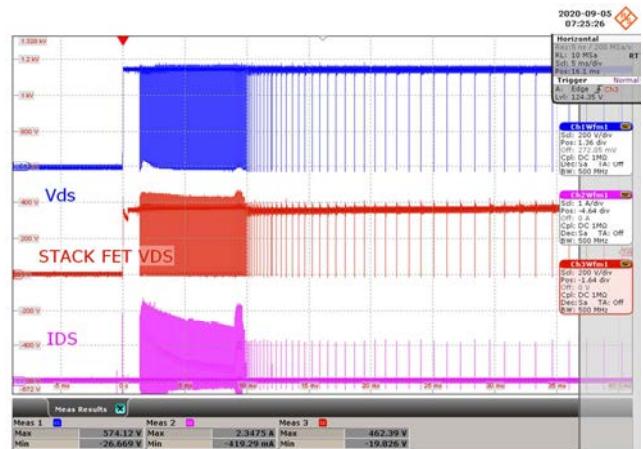IC $V_{DS(MAX)}$ = 582.03 V, $I_{DS(MAX)}$ = 2.07 A.
Stack FET $V_{DS(MAX)}$ = 475.92 V.



**Figure 38 –** 950 VDC Input.
CH1: IC $V_{DS}$, 200 V / div., 5 ms / div.
Ch2: $I_{DS}$, 1 A /div., 5 ms / div.
CH3: FET $V_{DS}$, 200 V / div., 5 ms / div.
IC $V_{DS(MAX)}$ = 574.12 V, $I_{DS(MAX)}$ = 2.38 A.
Stack FET $V_{DS(MAX)}$ = 468.02 V.

### 9.2.2.2   No-Load



**Figure 39 –** 60 VDC Input.
    CH1: IC V$_{DS}$, 30 V / div., 5 ms / div.
    Ch2: I$_{DS}$, 1 A /div., 5 ms / div.
    CH3: FET V$_{DS}$, 30 V / div., 5 ms / div.
    IC V$_{DS(MAX)}$ = 65.00 V, I$_{DS(MAX)}$ = 964.11 mA.
    Stack FET V$_{DS(MAX)}$ = 31.41 V.



**Figure 40 –** 360 VDC Input.
    CH1: IC V$_{DS}$, 200 V / div., 5 ms / div.
    Ch2: I$_{DS}$, 1 A /div., 5 ms / div.
    CH3: FET V$_{DS}$, 200 V / div., 5 ms / div.
    IC V$_{DS(MAX)}$ = 368.59 V, I$_{DS(MAX)}$ = 1.28 A.
    Stack FET V$_{DS(MAX)}$ = 278.29 V



**Figure 41 –** 600 VDC Input.
    CH1: IC V$_{DS}$, 200 V / div., 5 ms / div.
    Ch2: I$_{DS}$, 1 A /div., 5 ms / div.
    CH3: FET V$_{DS}$, 200 V / div., 5 ms / div.
    IC V$_{DS(MAX)}$ = 582.03 V, I$_{DS(MAX)}$ = 2.03 A.
    Stack FET V$_{DS(MAX)}$ = 483.83 V.



**Figure 42 –** 950 VDC Input.
    CH1: IC V$_{DS}$, 200 V / div., 5 ms / div.
    Ch2: I$_{DS}$, 1 A /div., 5 ms / div.
    CH3: FET V$_{DS}$, 200 V / div., 5 ms / div.
    IC V$_{DS(MAX)}$ = 574.12 V, I$_{DS(MAX)}$ = 2.34 A.
    Stack FET V$_{DS(MAX)}$ = 462.39 V.

### 9.2.3    Free Wheeling Diode Voltage at Normal Operation

### 9.2.3.1    Full Load
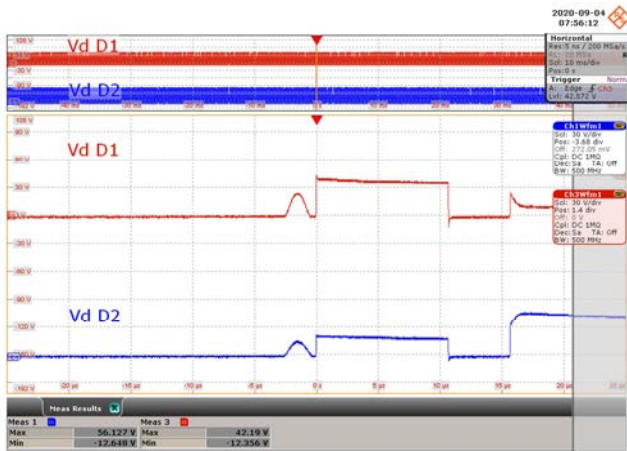


**Figure 43 –** 60 VDC Input.
  CH1: $V_{R,DIODE2}$, 30 V / div., 10 ms / div.
  CH3: $V_{R,DIODE1}$, 30 V / div., 10 ms / div.
  Zoom: 5 µs / div.
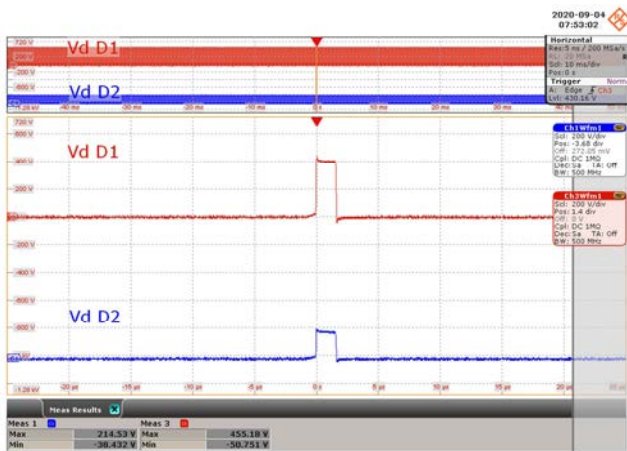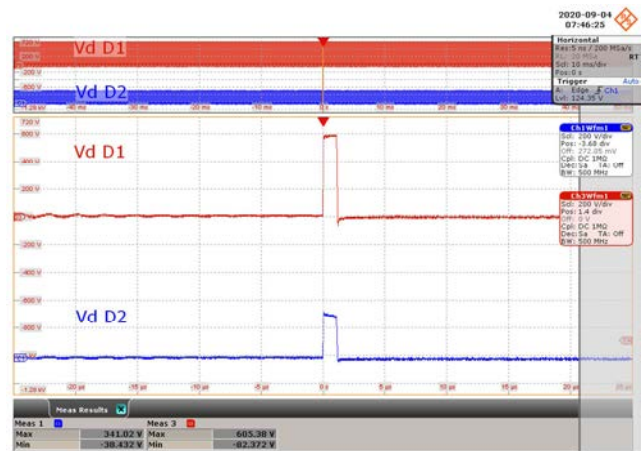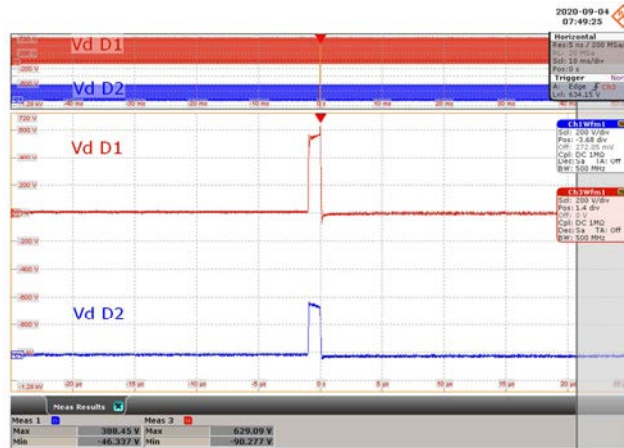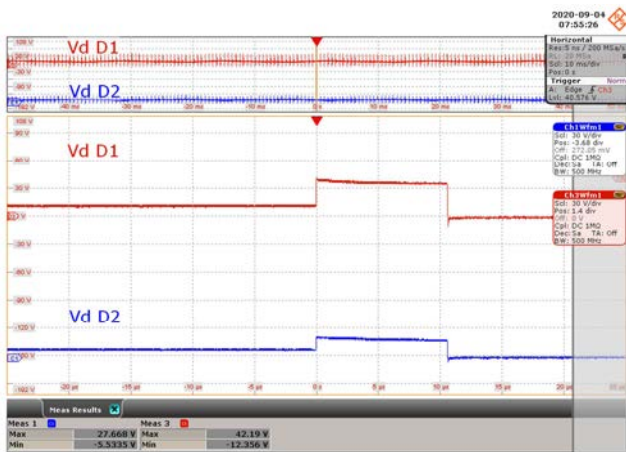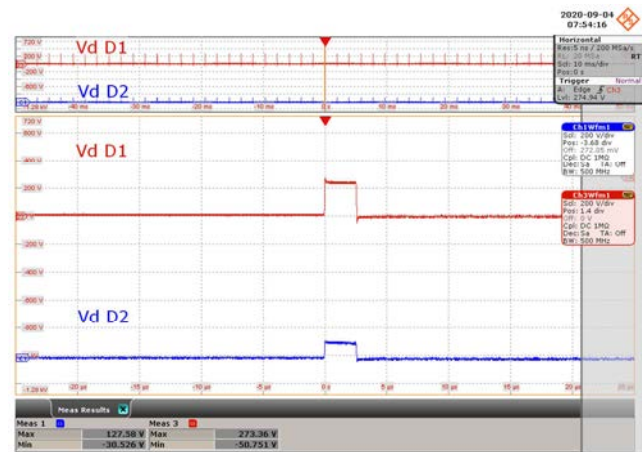  $PIV_{D1}$ = 42.19 V, $PIV_{D2}$ = 56.12 V.
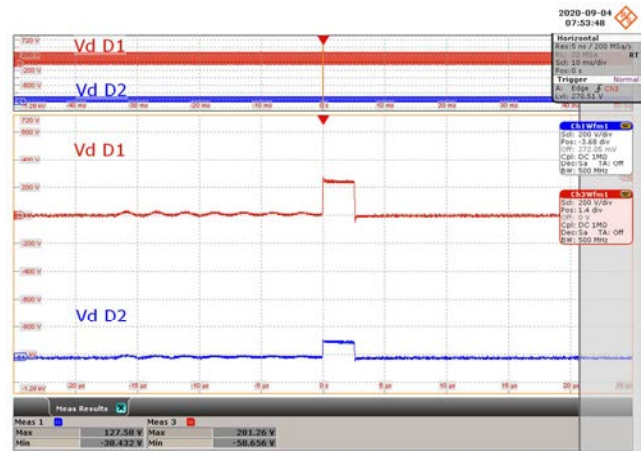


**Figure 44 –** 360 VDC Input.
  CH1: $V_{R,DIODE2}$, 200 V / div., 10 ms / div.
  CH3: $V_{R,DIODE1}$, 200 V / div., 10 ms / div.
  Zoom: 5 µs / div.
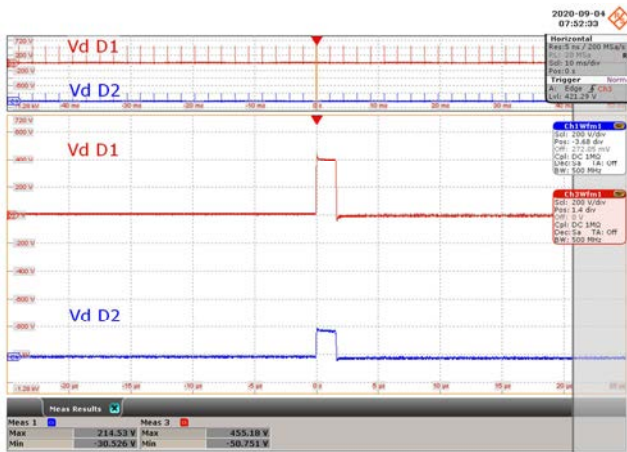  $PIV_{D1}$ = 281.26 V, $PIV_{D2}$ = 127.58 V.



**Figure 45 –** 600 VDC Input.
  CH1: $V_{R,DIODE2}$, 200 V / div., 10 ms / div.
  CH3: $V_{R,DIODE1}$, 200 V / div., 10 ms / div.
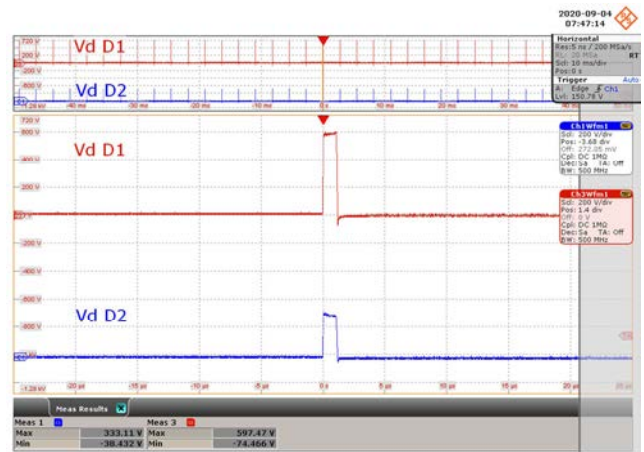  Zoom: 5 µs / div.
  $PIV_{D1}$ = 455.18 V, $PIV_{D2}$ = 214.53 V.



**Figure 46 –** 950 VDC Input.
  CH1: $V_{R,DIODE2}$, 200 V / div., 10 ms / div.
  CH3: $V_{R,DIODE1}$, 200 V / div., 10 ms / div.
  Zoom: 5 µs / div.
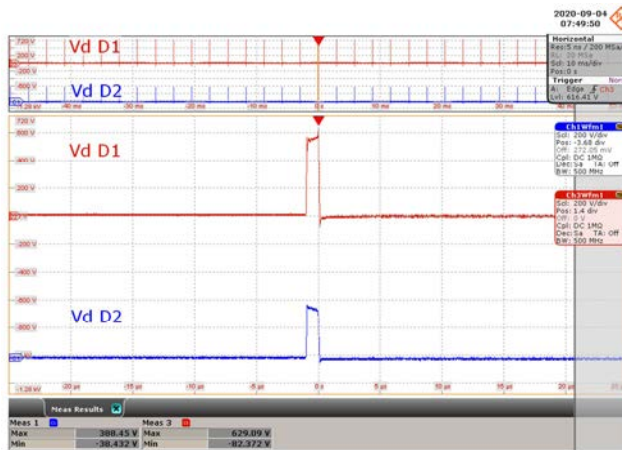  $PIV_{D1}$ = 605.38 V, $PIV_{D2}$ = 341.02 V.

**Figure 47 –** 1100 VDC Input.
CH1: $V_{R,DIODE2}$, 200 V / div., 10 ms / div.
CH3: $V_{R,DIODE1}$, 200 V / div., 10 ms / div.
Zoom: 5 µs / div.
$PIV_{D1}$ = 629.09 V, $PIV_{D2}$ = 388.45 V.

### 9.2.3.2   No-Load



**Figure 48 –** 60 VDC Input.
CH1: $V_{R,DIODE2}$, 30 V / div., 10 ms / div.
CH3: $V_{R,DIODE1}$, 30 V / div., 10 ms / div.
Zoom: 5 µs / div.
$PIV_{D1}$ = 42.19 V, $PIV_{D2}$ = 27.66 V.



**Figure 49 –** 360 VDC Input.
CH1: $V_{R,DIODE2}$, 200 V / div., 10 ms / div.
CH3: $V_{R,DIODE1}$, 200 V / div., 10 ms / div.
Zoom: 5 µs / div.
$PIV_{D1}$ = 273.36 V, $PIV_{D2}$ = 127.58 V.

**Figure 50 –** 600 VDC Input.
CH1: $V_{R,DIODE2}$, 200 V / div., 10 ms / div.
CH3: $V_{R,DIODE1}$, 200 V / div., 10 ms / div.
Zoom: 5 µs / div.
$PIV_{D1}$ = 455.18 V, $PIV_{D2}$ = 214.53 V.

**Figure 51 –** 950 VDC Input.
CH1: $V_{R,DIODE2}$, 200 V / div., 10 ms / div.
CH3: $V_{R,DIODE1}$, 200 V / div., 10 ms / div.
Zoom: 5 µs / div.
$PIV_{D1}$ = 597.47 V, $PIV_{D2}$ = 333.11 V.

**Figure 52 –** 1100 VDC Input.
CH1: $V_{R,DIODE2}$, 200 V / div., 10 ms / div.
CH3: $V_{R,DIODE1}$, 200 V / div., 10 ms / div.
Zoom: 5 µs / div.
$PIV_{D1}$ = 629.09 V, $PIV_{D2}$ = 388.45 V.

## 9.3    *Output Start-Up*

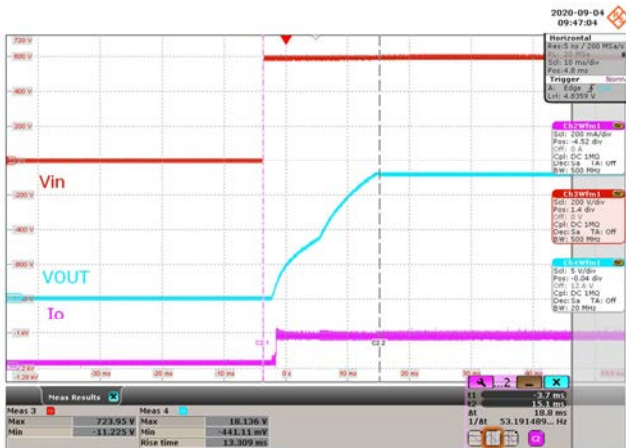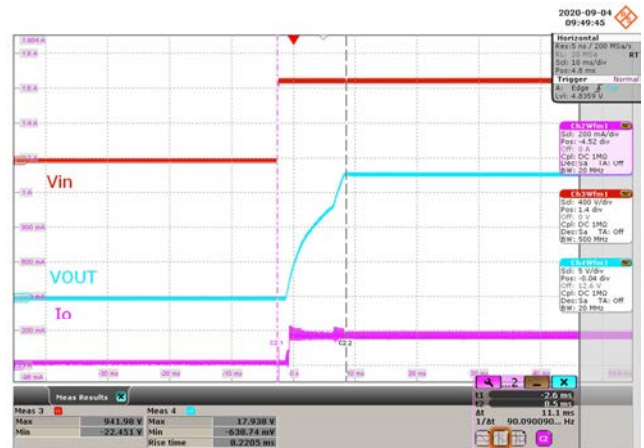### 9.3.1      Output Start-Up Full Load CC
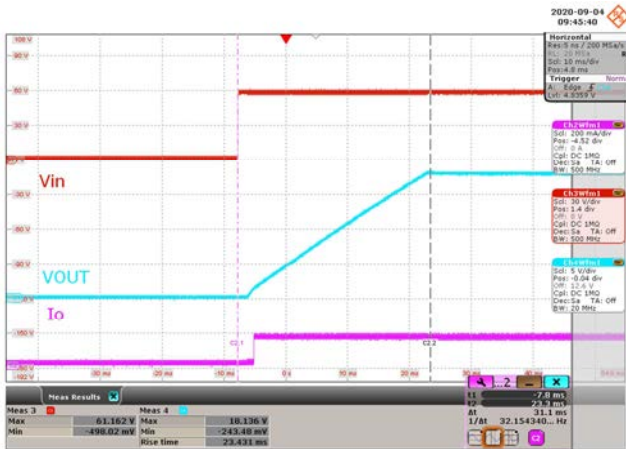


**Figure 53 –** 60 VDC Input.
Ch2: $I_{OUT}$, 200 mA / div., 10 ms / div.
CH3: $V_{IN}$, 30 V / div., 10 ms / div.
Ch4: $V_{OUT}$, 5 V / div., 10 ms / div.
$V_{OUT(MAX)}$ = 18.13 V, $V_{OUT(RISE)}$ = 23.43 ms.
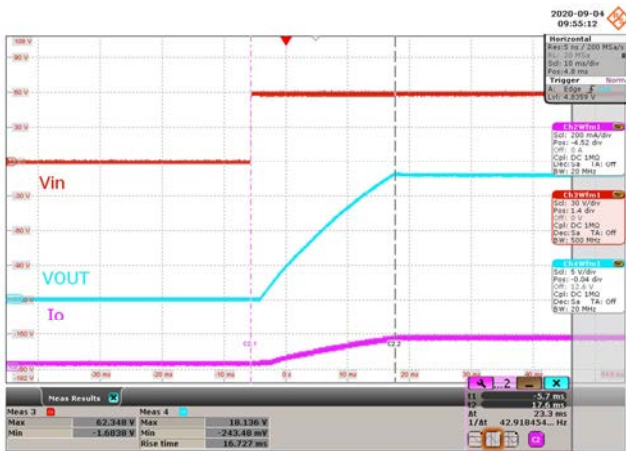$T_{\_Vo\_to\_Vin}$ = 31.1 ms.
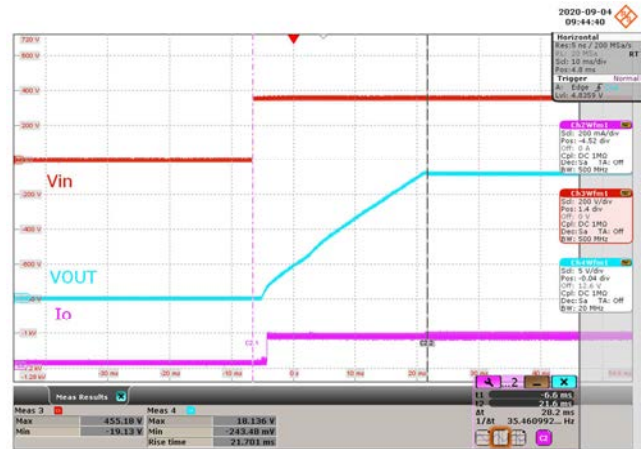


**Figure 54 –** 360 VDC Input.
Ch2: $I_{OUT}$, 200 mA / div., 10 ms / div.
CH3: $V_{IN}$, 200 V / div., 10 ms / div.
Ch4: $V_{OUT}$, 5 V / div., 10 ms / div.
$V_{OUT(MAX)}$ = 18.13, $V_{OUT(RISE)}$ = 21.70 ms.
$T_{\_Vo\_to\_Vin}$ = 28.2 ms.



**Figure 55 –** 600 VDC Input.
Ch2: $I_{OUT}$, 200 mA / div., 10 ms / div.
CH3: $V_{IN}$, 200 V / div., 10 ms / div.
Ch4: $V_{OUT}$, 5 V / div., 10 ms / div.
$V_{OUT(MAX)}$ = 18.13 V, $V_{OUT(RISE)}$ = 13.30 ms.
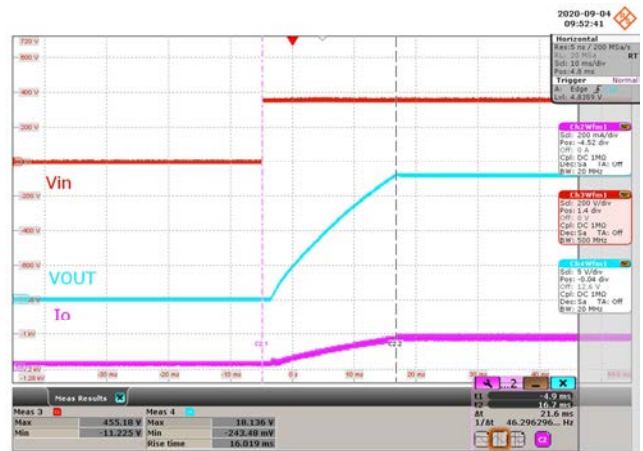$T_{\_Vo\_to\_Vin}$ = 18.8 ms.



**Figure 56 –** 950 VDC Input.
Ch2: $I_{OUT}$, 200 mA / div., 10 ms / div.
CH3: $V_{IN}$, 400 V / div., 10 ms / div.
Ch4: $V_{OUT}$, 5 V / div., 10 ms / div.
$V_{OUT(MAX)}$ = 17.93 V, $V_{OUT(RISE)}$ = 8.22 ms.
$T_{\_Vo\_to\_Vin}$ = 11.1 ms.

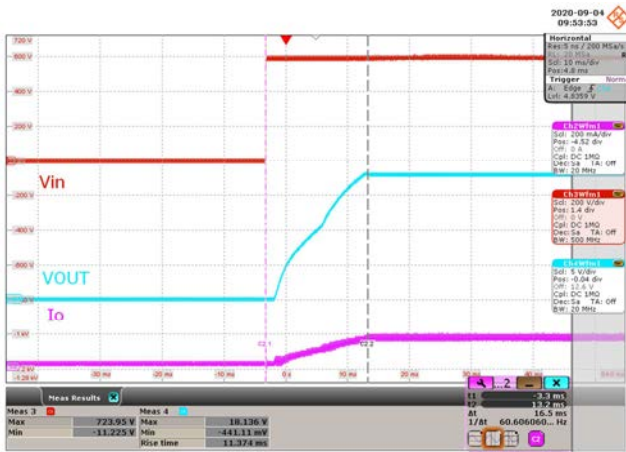## 9.3.2       Output Start-Up Full Load CR



**Figure 57 –** 60 VDC Input.
   Ch2: $I_{OUT}$, 200 mA / div., 10 ms / div.
   CH3: $V_{IN}$, 30 V / div., 10 ms / div.
   Ch4: $V_{OUT}$, 5 V / div., 10 ms / div.
   $V_{OUT(MAX)}$ = 18.13 V, $V_{OUT(RISE)}$ = 16.72 ms.
   $T_{\_Vo\_to\_Vin}$ = 23.3 ms.



**Figure 58 –** 360 VDC Input.
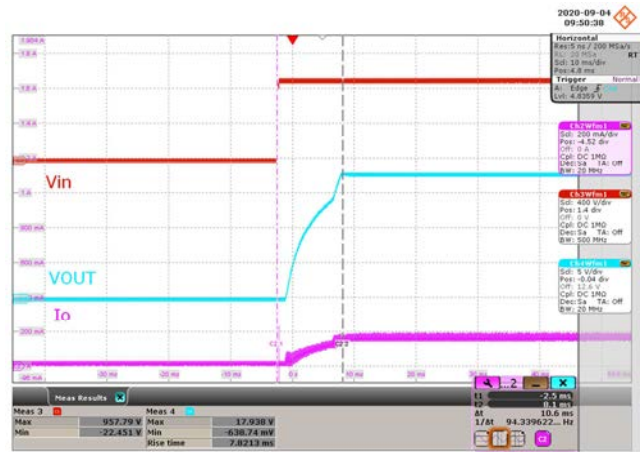   Ch2: $I_{OUT}$, 200 mA / div., 10 ms / div.
   CH3: $V_{IN}$, 200 V / div., 10 ms / div.
   Ch4: $V_{OUT}$, 5 V / div., 10 ms / div.
   $V_{OUT(MAX)}$ = 18.13 V, $V_{OUT(RISE)}$ = 16.01 ms.
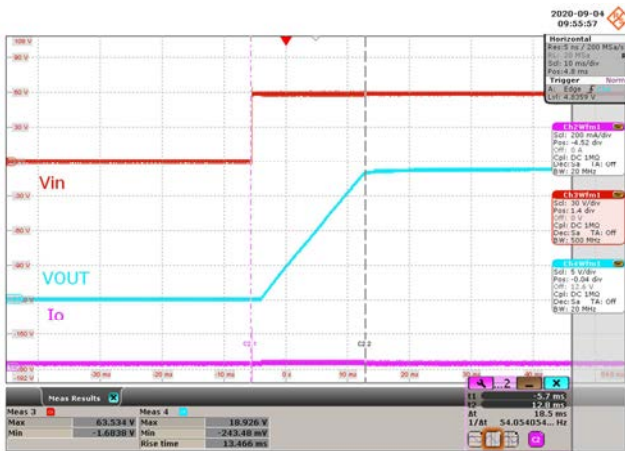   $T_{\_Vo\_to\_Vin}$ = 21.6 ms.



**Figure 59 –** 600 VDC Input.
   Ch2: $I_{OUT}$, 200 mA / div., 10 ms / div.
   CH3: $V_{IN}$, 200 V / div., 10 ms / div.
   Ch4: $V_{OUT}$, 5 V / div., 10 ms / div.
   $V_{OUT(MAX)}$ = 18.13 V, $V_{OUT(RISE)}$ = 11.37 ms.
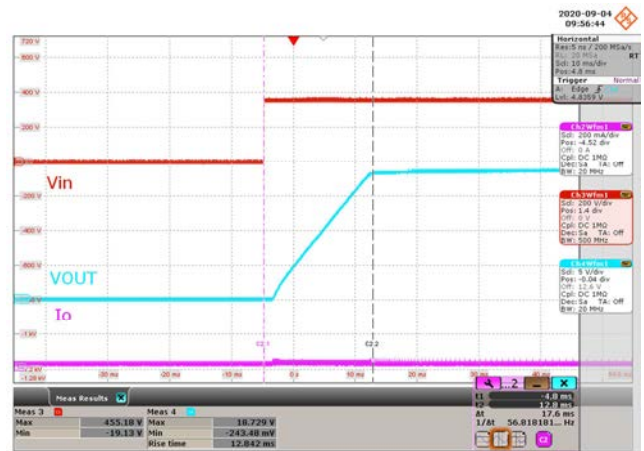   $T_{\_Vo\_to\_Vin}$ = 16.5 ms.



**Figure 60 –** 950 VDC Input.
   Ch2: $I_{OUT}$, 200 mA / div., 10 ms / div.
   CH3: $V_{IN}$, 400 V / div., 10 ms / div.
   Ch4: $V_{OUT}$, 5 V / div., 10 ms / div.
   $V_{OUT(MAX)}$ = 17.93 V, $V_{OUT(RISE)}$ = 7.82 ms.
   $T_{\_Vo\_to\_Vin}$ = 10.6 ms.

### 9.3.3    Output Start-Up No-Load



**Figure 61 –** 60 VDC Input.
Ch2: $I_{OUT}$, 200 mA / div., 10 ms / div.
CH3: $V_{IN}$, 30 V / div., 10 ms / div.
Ch4: $V_{OUT}$, 5 V / div., 10 ms / div.
$V_{OUT(MAX)}$ = 18.92 V, $V_{OUT(RISE)}$ = 13.46 ms.
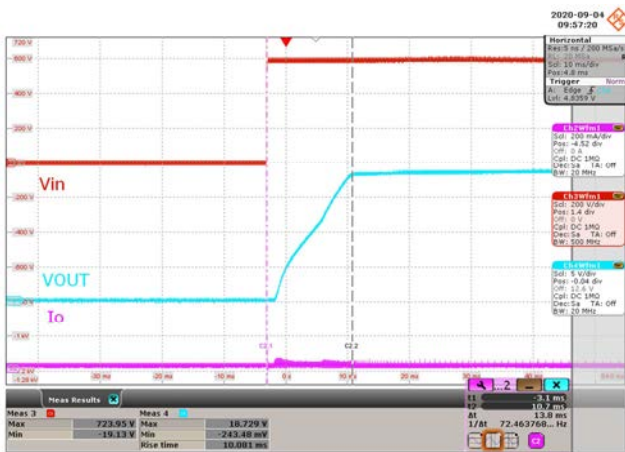$T_{\_Vo\_to\_Vin}$ = 18.5 ms.



**Figure 62 –** 360 VDC Input.
Ch2: $I_{OUT}$, 200 mA / div., 10 ms / div.
CH3: $V_{IN}$, 200 V / div., 10 ms / div.
Ch4: $V_{OUT}$, 5 V / div., 10 ms / div.
$V_{OUT(MAX)}$ = 18.72 V, $V_{OUT(RISE)}$ = 12.842 ms.
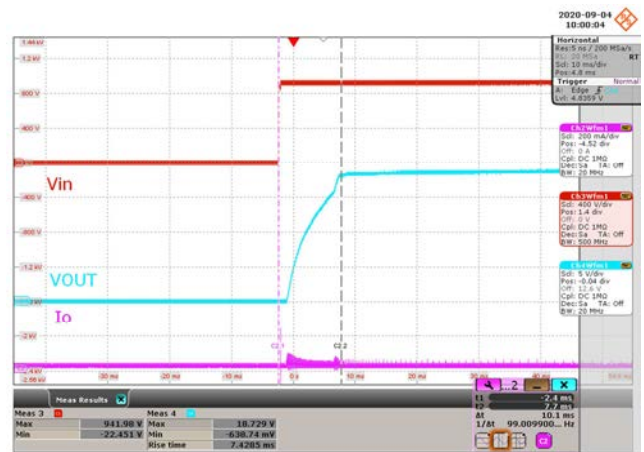$T_{\_Vo\_to\_Vin}$ = 17.6 ms.



**Figure 63 –** 600 VDC Input.
Ch2: $I_{OUT}$, 200 mA / div., 10 ms / div.
CH3: $V_{IN}$ , 200 V / div., 10 ms / div.
Ch4: $V_{OUT}$, 5 V / div., 10 ms / div.
$V_{OUT(MAX)}$ = 18.72 V, $V_{OUT(RISE)}$ = 10.08 ms.
$T_{\_Vo\_to\_Vin}$ = 13.8 ms.



**Figure 64 –** 950 VDC Input.
Ch2: $I_{OUT}$, 200 mA / div., 10 ms / div.
CH3: $V_{IN}$ , 400 V / div., 10 ms / div.
Ch4: $V_{OUT}$, 5 V / div., 10 ms / div.
$V_{OUT(MAX)}$ = 18.72 V, $V_{OUT(RISE)}$ = 7.42 ms.
$T_{\_Vo\_to\_Vin}$ = 10.1 ms.

## 9.4    *Fault Conditions*

### 9.4.1    18 V Output Short-Circuit



**Figure 65 –** 60 VDC Input. Output Short.
CH1: IC $V_{DS}$, 30 V / div., 1 s / div.
Ch2: $I_{DS}$, 1 A / div., 1 s / div.
CH3: FET $V_{DS}$, 30 V / div., 1 s / div.
IC $V_{DS(MAX)}$ = 66.19 V., $I_{DS(MAX)}$ = 924.58 mA.
Stack FET $V_{DS(MAX)}$ = 30.22 V.



**Figure 66 –** 360 VDC Input. Output Short.
CH1: IC $V_{DS}$, 200 V / div., 1 s / div.
Ch2: $I_{DS}$, 1 A / div., 1 s / div.
CH3: FET $V_{DS}$, 200 V / div., 1 s / div.
IC $V_{DS(MAX)}$ = 376.49 V., $I_{DS(MAX)}$ = 1.63 A.
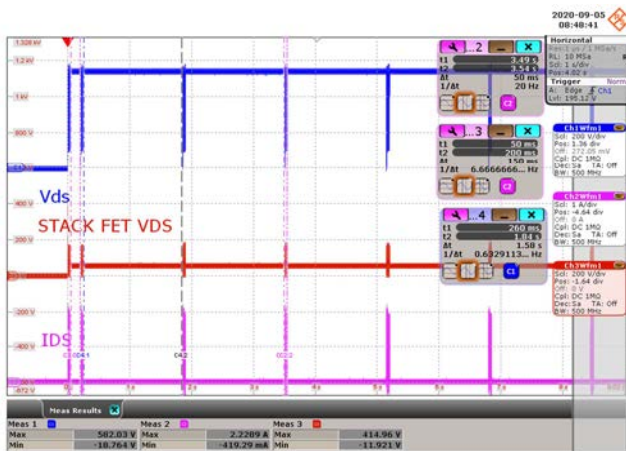Stack FET $V_{DS(MAX)}$ = 225.53 V.



**Figure 67 –** 600 VDC Input. Output Short.
CH1: IC $V_{DS}$, 200 V / div., 1 s / div.
Ch2: $I_{DS}$, 1 A / div., 1 s / div.
CH3: FET $V_{DS}$, 200 V / div., 1 s / div.
IC $V_{DS(MAX)}$ = 582.03 V., $I_{DS(MAX)}$ = 2.22 A.
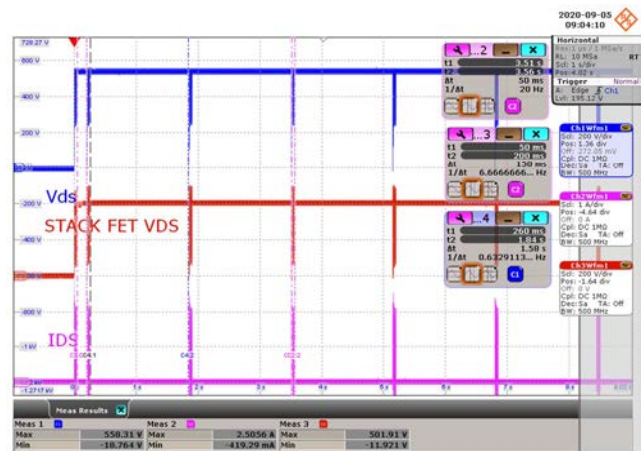Stack FET $V_{DS(MAX)}$ = 414.96 V.



**Figure 68 –** 950 VDC Input. Output Short.
CH1: IC $V_{DS}$, 200 V / div., 1 s / div.
Ch2: $I_{DS}$, 1 A / div., 1 s / div.
CH3: FET $V_{DS}$, 200 V / div., 1 s / div.
IC $V_{DS(MAX)}$ = 558.31 V., $I_{DS(MAX)}$ = 2.50A.
Stack FET $V_{DS(MAX)}$ = 501.91 V.

**Figure 69 –** 1100 VDC Input. Output Short.
CH1: IC $V_{DS}$, 200 V / div., 1 s / div.
Ch2: $I_{DS}$, 1 A / div., 1 s / div.
CH3: FET $V_{DS}$, 200 V / div., 1 s / div.
IC $V_{DS(MAX)}$ = 574.12 V., $I_{DS(MAX)}$ = 2.14 A.
Stack FET $V_{DS(MAX)}$ = 628.4 V.

## 9.5    *Output Voltage Ripple*

### 9.5.1    Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 $\mu$F / 50 V ceramic type and one (1) 47 $\mu$F / 50 V aluminum electrolytic.  The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).
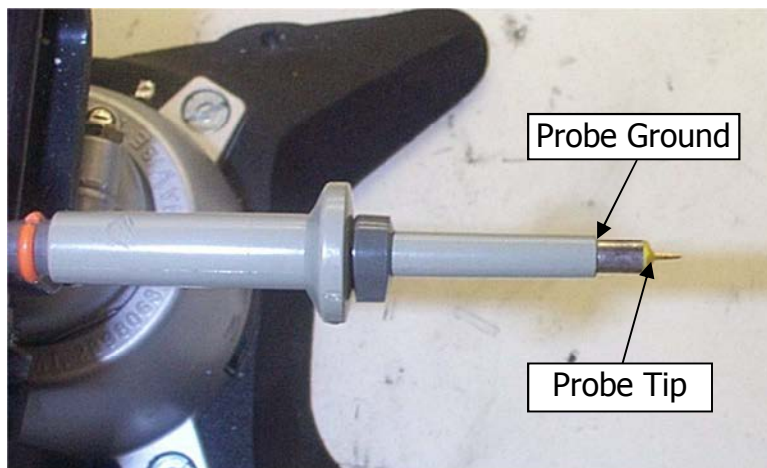


Probe Ground

Probe Tip

**Figure 70 –** Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)
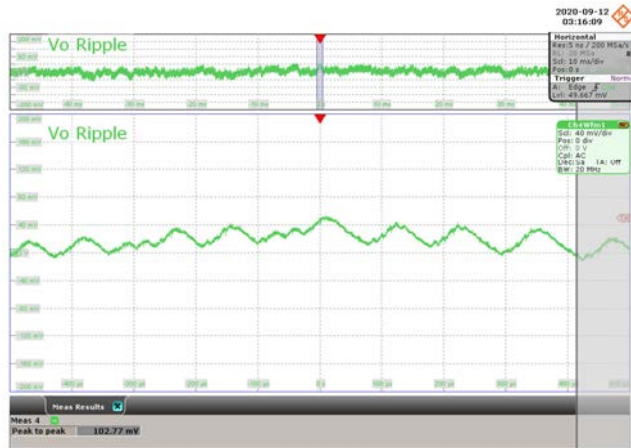


**Figure 71 –** Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter.
(Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

### 9.5.2      Measurement Results

Note: All ripple measurements were taken at PCB end.

### 9.5.2.1      100% Load Condition



20

**Figure 72 –** 60 VDC Input.
        CH4: V$_{OUT,}$ 40 mV / div., 10 ms / div.
        Zoom: 100 µs / div.
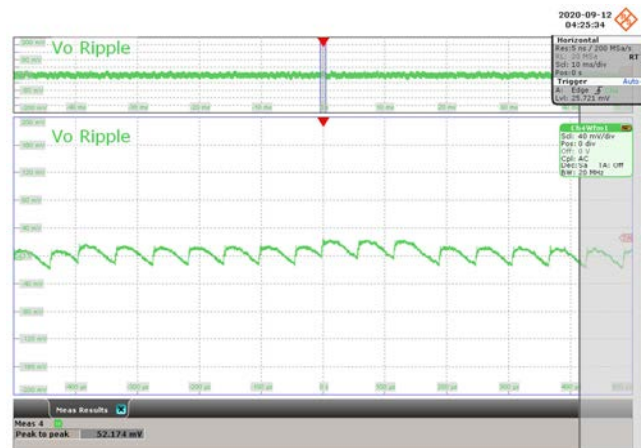        18 V Output Ripple = 102.77 mV.



**Figure 73 –** 360VDC Input.
        CH4: V$_{OUT,}$ 40 mV / div., 10 ms / div.
        Zoom: 100 µs / div.
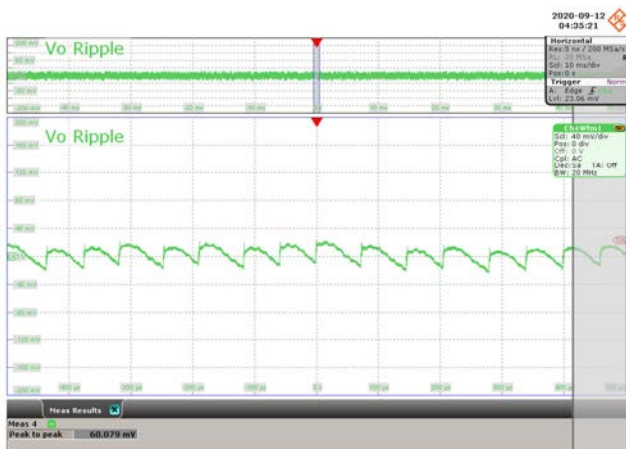        18 V Output Ripple = 52.17 mV.



**Figure 74 –** 600 VDC Input.
        CH4: V$_{OUT,}$ 40 mV / div., 10 ms / div.
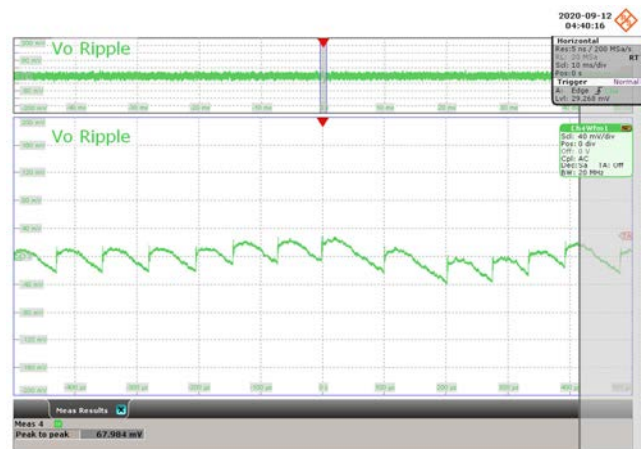        Zoom: 100 µs / div.
        18 V Output Ripple = 60.07 mV.



**Figure 75 –** 950 VDC Input.
        CH4: V$_{OUT,}$ 40 mV / div., 10 ms / div.
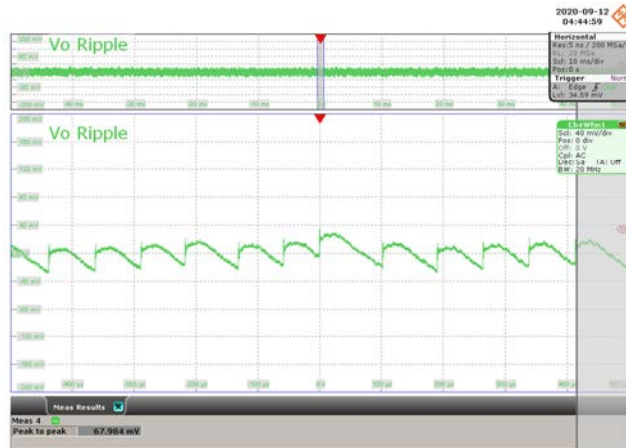        Zoom: 100 µs / div.
        18 V Output Ripple = 67.98 mV.

**Figure 76 –** 1100 VDC Input.
CH4: V$_{OUT,}$ 40 mV / div., 10 ms / div.
Zoom: 100 µs / div.
18 V Output Ripple = 67.98 mV.
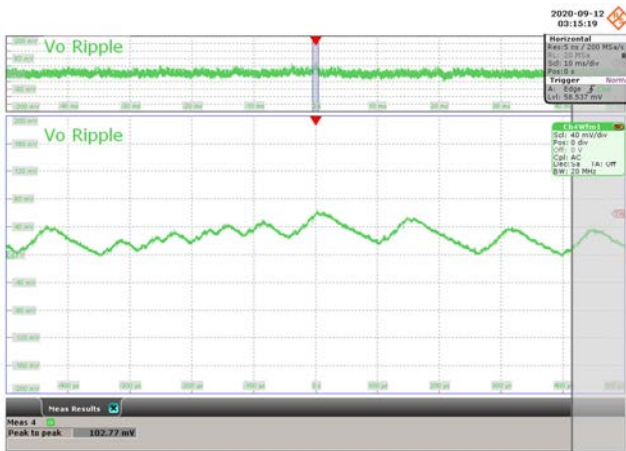
## 9.5.2.2    75% Load Condition





2.

**Figure 77 –** 60 VDC Input.
CH4: V$_{OUT,}$ 40 mV / div., 10 ms / div.
Zoom: 100 µs / div.
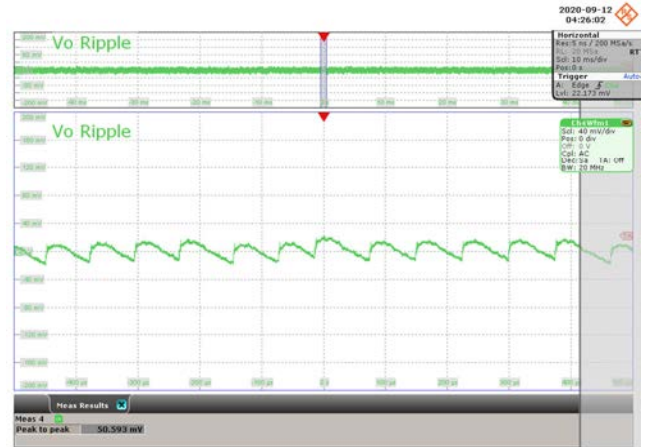18 V Output Ripple = 102.77 mV.

**Figure 78 –** 360 VDC Input.
CH4: V$_{OUT,}$ 40 mV / div., 10 ms / div.
Zoom: 100 µs / div.
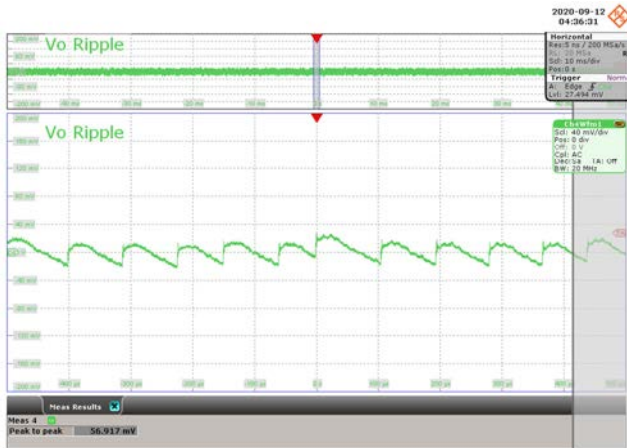18 V Output Ripple = 50.59 mV.

**Figure 79 –** 600 VDC Input.
CH4: $V_{OUT}$, 40 mV / div., 10 ms / div.
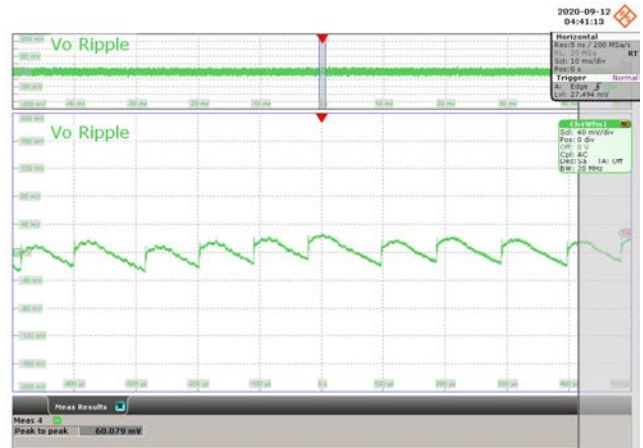Zoom: 100 µs / div.
18 V Output Ripple = 56.91 mV.



**Figure 80 –** 950 VDC Input.
CH4: $V_{OUT}$, 40 mV / div., 10 ms / div.
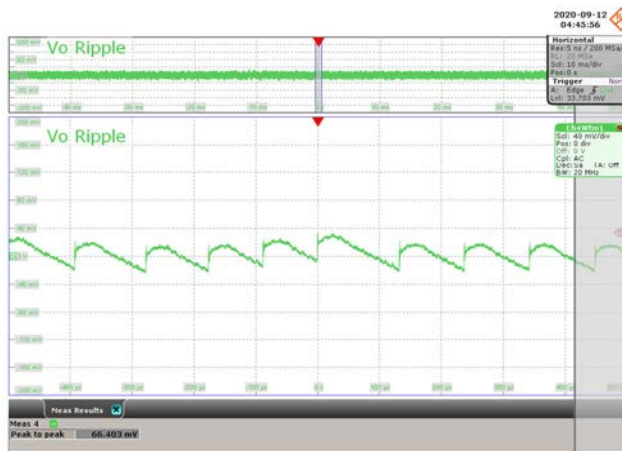Zoom: 100 µs / div.
18 V Output Ripple = 60.07 mV.



**Figure 81 –** 1100 VDC Input.
CH4: $V_{OUT}$, 40 mV / div., 10 ms / div.
Zoom: 100 µs / div.
18 V Output Ripple = 66.40 mV.
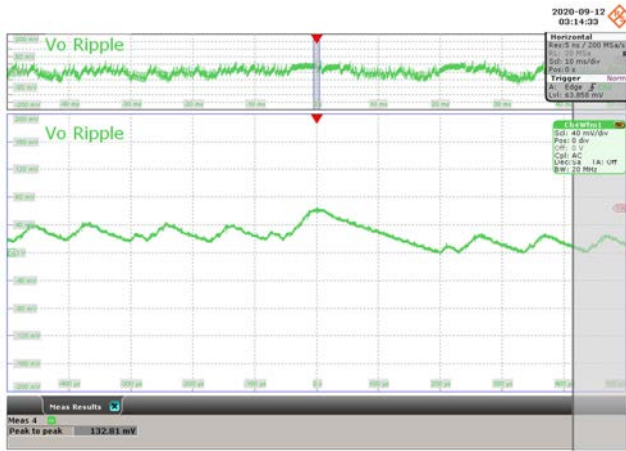
### 9.5.2.3    50% Load Condition



**Figure 82 –** 60 VDC Input.
CH4: V$_{OUT}$, 40 mV / div., 10 ms / div.
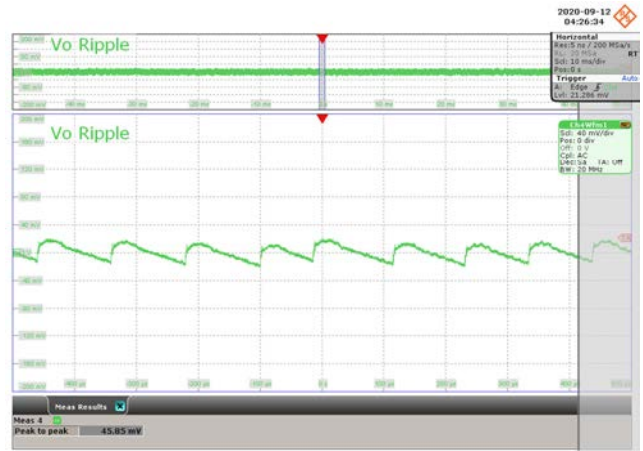Zoom: 100 µs / div.
18 V Output Ripple = 132.81 mV.



**Figure 83 –** 360 VDC Input.
CH4: V$_{OUT}$, 40 mV / div., 10 ms / div.
Zoom: 100 µs / div.
18 V Output Ripple = 45.85 mV.



**Figure 84 –** 600 VDC Input.
CH4: V$_{OUT}$, 40 mV / div., 10 ms / div.
Zoom: 100 µs / div.
18 V Output Ripple = 50.59 mV**.**



**Figure 85 –** 950 VDC Input.
CH4: V$_{OUT}$, 40 mV / div., 10 ms / div.
Zoom: 100 µs / div.
18 V Output Ripple = 55.33 mV**.**

**Figure 86 –** 1100 VDC Input.
CH4: V$_{OUT,}$ 40 mV / div., 10 ms / div.
Zoom: 100 μs / div.
18 V Output Ripple = 60.07 mV**.**

### 9.5.2.4    25% Load Condition





**Figure 87 –** 60 VDC Input.
CH4: V$_{OUT,}$ 40 mV / div., 10 ms / div.
Zoom: 100 μs / div.
18 V Output Ripple = 104.35 mV.

**Figure 88 –** 360 VDC Input.
CH4: V$_{OUT,}$ 40 mV / div., 10 ms / div.
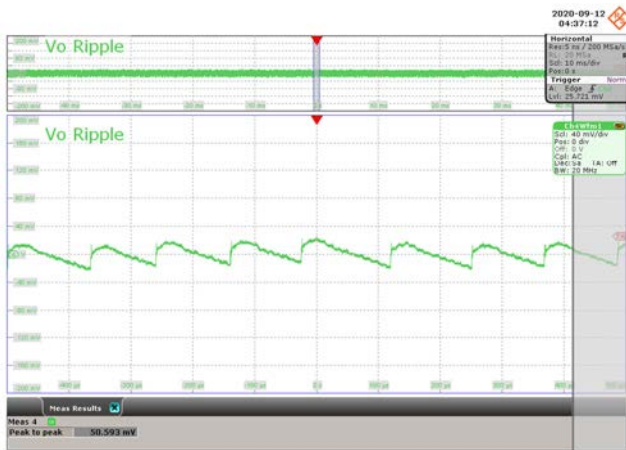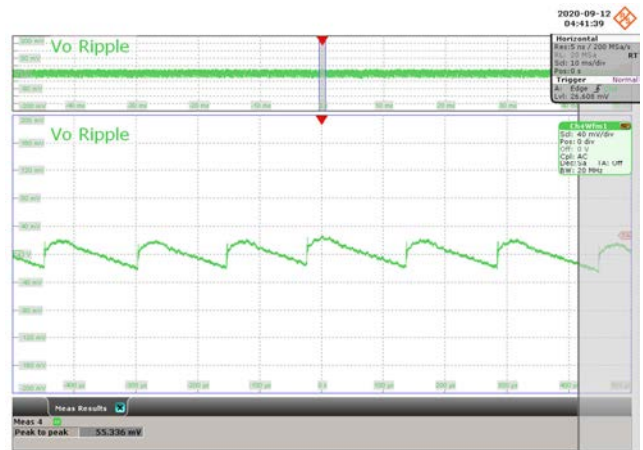Zoom: 100 μs / div.
18 V Output Ripple =44.26 mV**.**

**Figure 89 –** 600 VDC Input.
CH4: $V_{OUT,}$ 40 mV / div., 10 ms / div.
Zoom: 100 µs / div.
18 V Output Ripple = 47.43 mV.



**Figure 90 –** 950 VDC Input.
CH4: $V_{OUT,}$ 40 mV / div., 10 ms / div.
Zoom: 100 µs / div.
18 V Output Ripple = 52.17 mV.



**Figure 91 –** 1100 VDC Input.
CH4: $V_{OUT,}$ 40 mV / div., 10 ms / div.
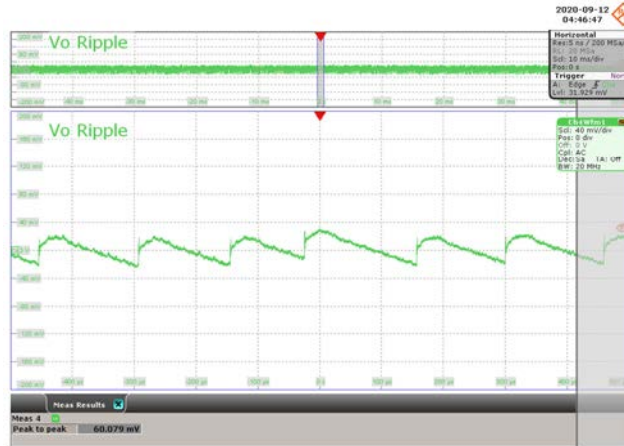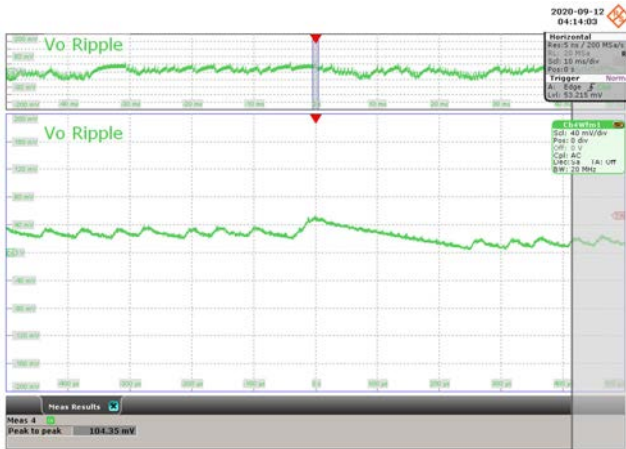Zoom: 100 µs / div.
18 V Output Ripple = 55.33 mV.

## 9.5.2.5    10% Load Condition



**Figure 92 –** 60 VDC Input.
CH4: V~OUT,~ 40 mV / div., 10 ms / div.
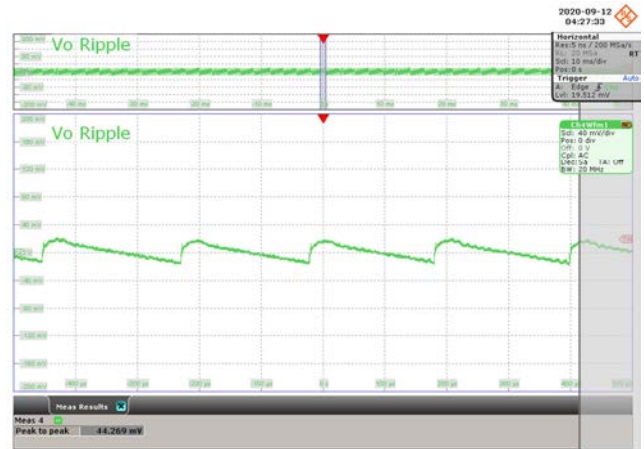Zoom: 100 μs / div.
18 V Output Ripple = 23.71 mV.



**Figure 93 –** 360 VDC Input.
CH4: V~OUT,~ 40 mV / div., 10 ms / div.
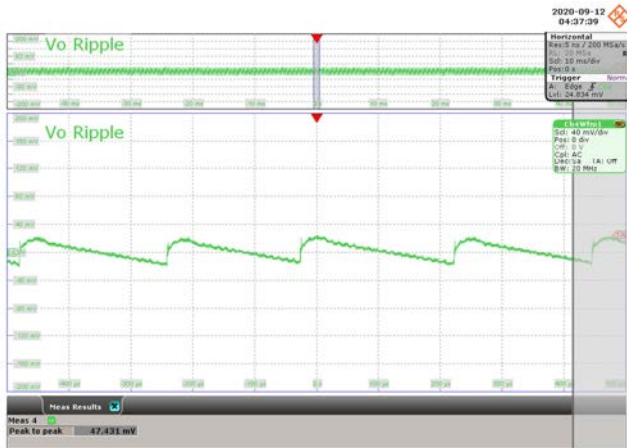Zoom: 100 μs / div.
18 V Output Ripple = 41.10 mV.



**Figure 94 –** 600 VDC Input.
CH4: V~OUT,~ 40 mV / div., 10 ms / div.
Zoom: 100 μs / div.
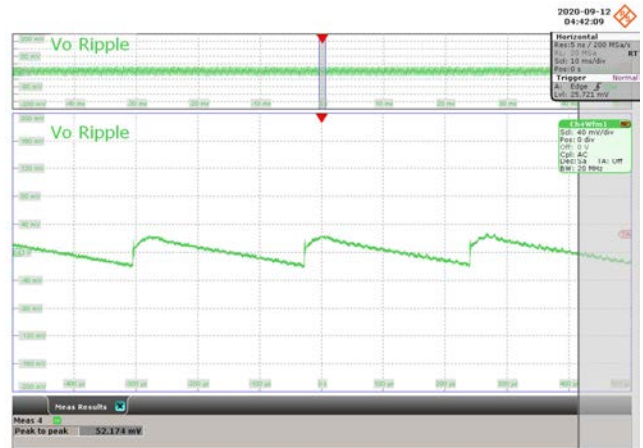18 V Output Ripple = 45.85 mV.
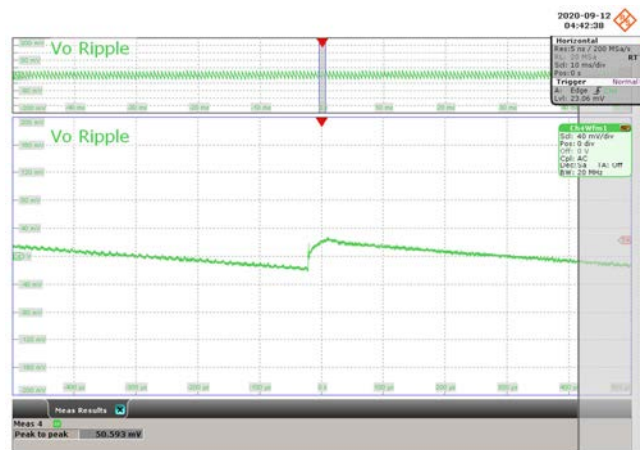


**Figure 95 –** 950 VDC Input.
CH4: V~OUT,~ 40 mV / div., 10 ms / div.
Zoom: 100 μs / div.
18 V Output Ripple = 50.59 mV.
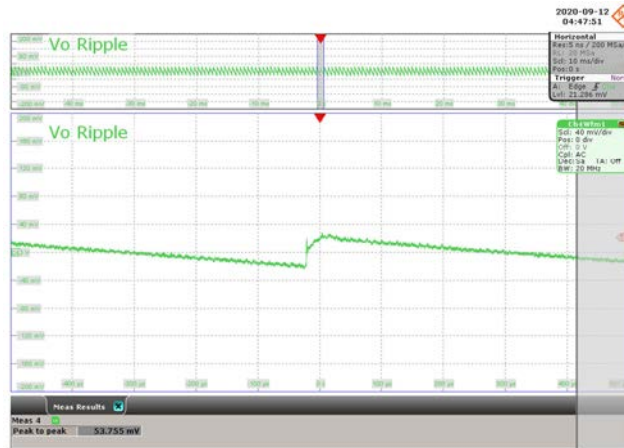
**Figure 96 –** 1100 VDC Input.
CH4: V<sub>OUT,</sub> 40 mV / div., 10 ms / div.
Zoom: 100 µs / div.
18 V Output Ripple = 53.75 mV.

## 9.5.2.6    No-Load Condition
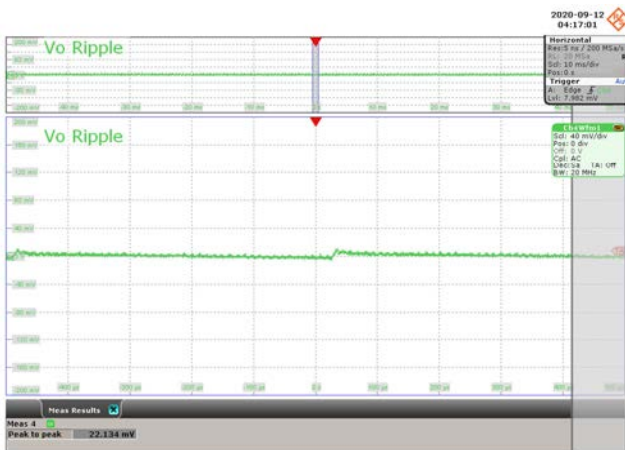


**Figure 97 –** 60 VDC Input.
CH4: V<sub>OUT,</sub> 40 mV / div., 10 ms / div.
Zoom: 100 µs / div.
18 V Output Ripple = 22.13 mV.
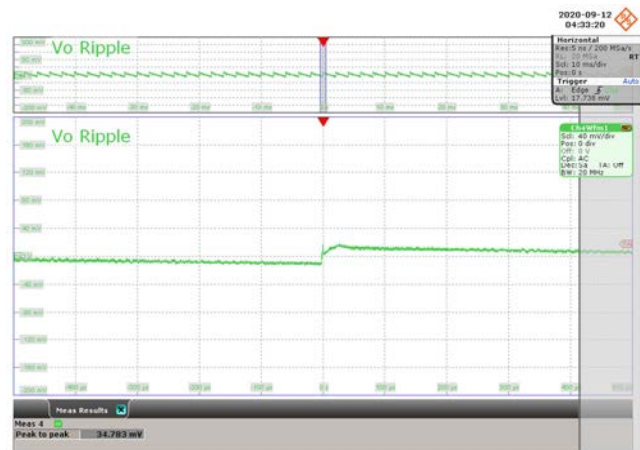


**Figure 98 –** 360 VDC Input.
CH4: V<sub>OUT,</sub> 40 mV / div., 10 ms / div.
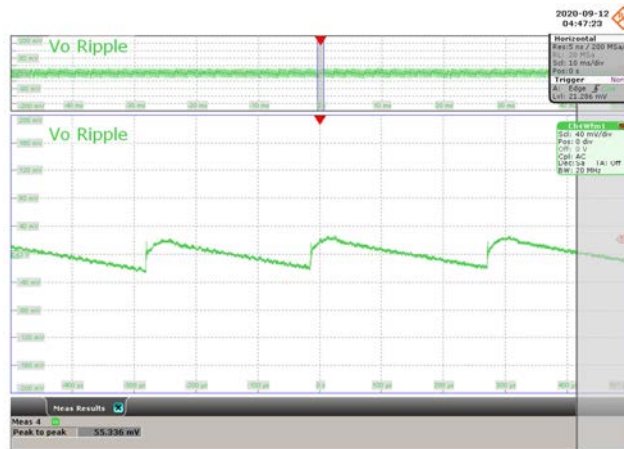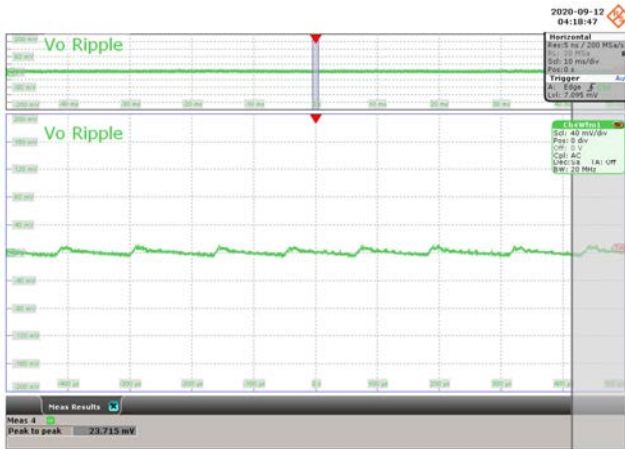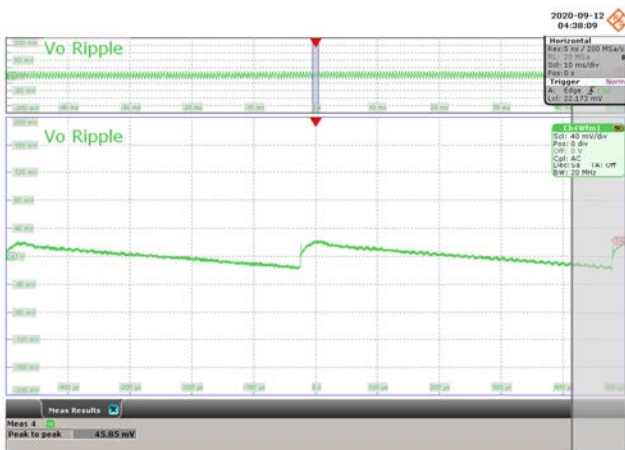Zoom: 100 µs / div.
18 V Output Ripple = 34.78 mV.
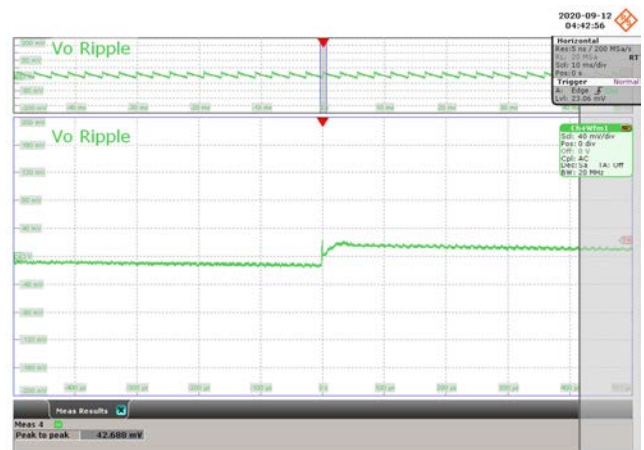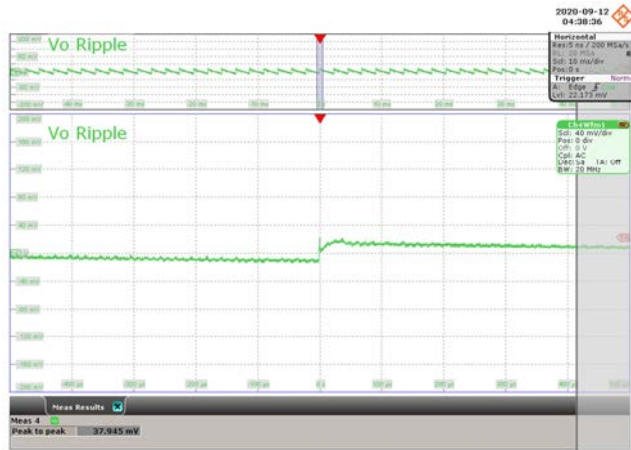
10

**Figure 99 –** 600 VDC Input.
CH4: V$_{OUT,}$ 40 mV / div., 10 ms / div.
Zoom: 100 µs / div.
18 V Output Ripple = 37.94 mV.

**Figure 100 –** 950 VDC Input.
CH4: V$_{OUT,}$ 40 mV / div., 10 ms / div.
Zoom: 100 µs / div.
18 V Output Ripple = 42.68 mV.
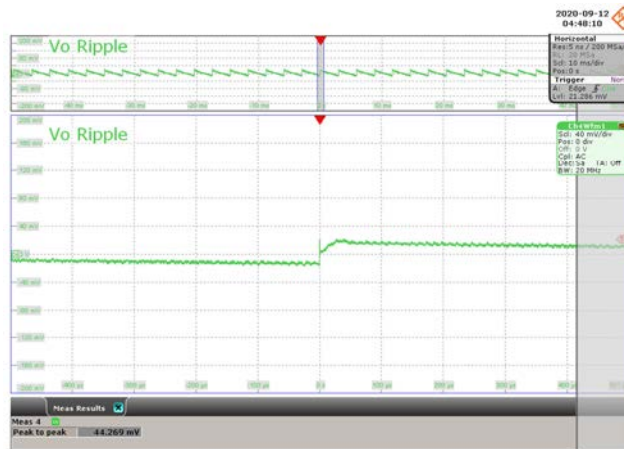


**Figure 101 –** 1100 VDC Input.
CH4: V$_{OUT,}$ 40 mV / div., 10 ms / div.
Zoom: 100 µs / div.
18 V Output Ripple = 44.269 mV.

### 9.5.3      18 V Output Ripple Voltage Graph
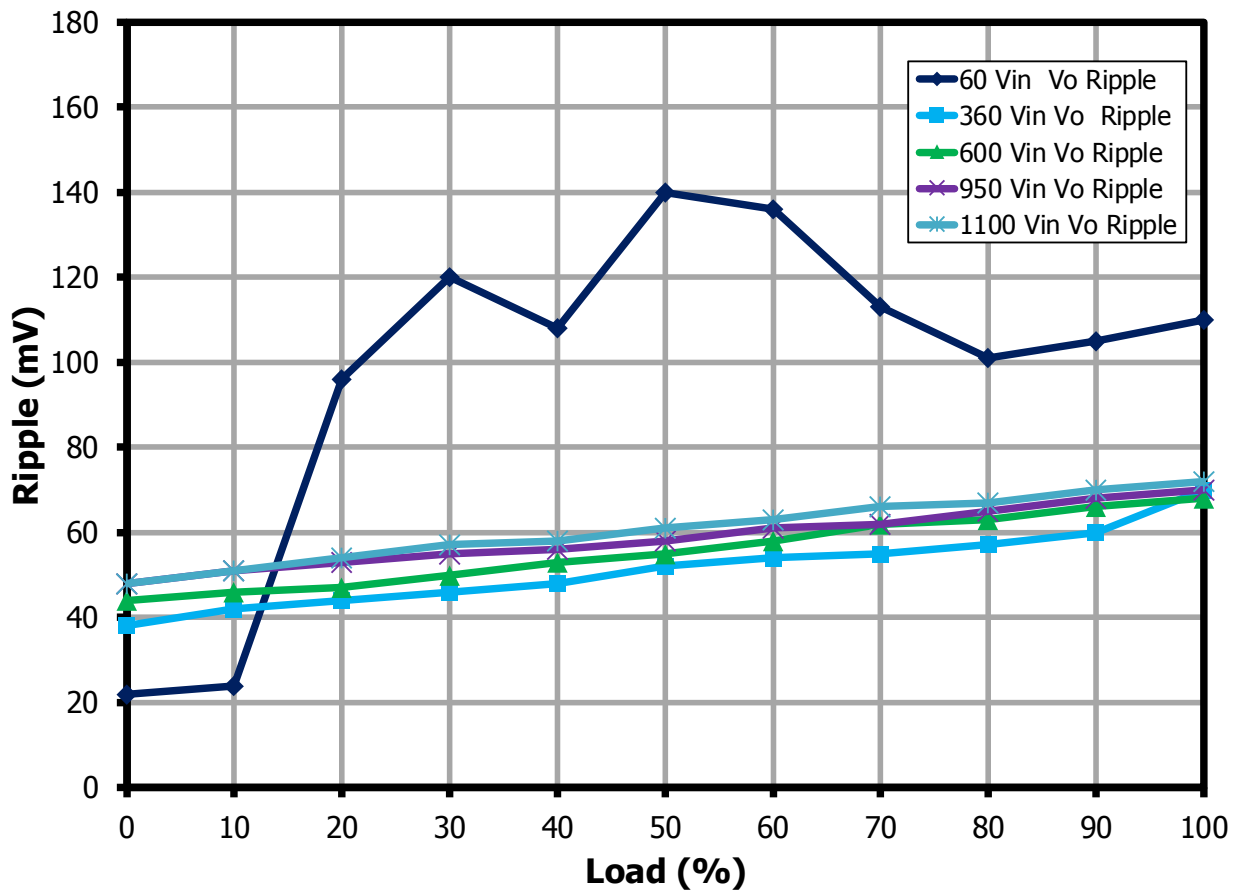


**Figure 102 –** 18 V Voltage Ripple (Measured at PCB End at Room Temperature).

## 10   Thermal Performance

### 10.1   *Test Set-up*

Thermal evaluation was performed under two conditions: (1) room temperature with the circuit board enclosed inside an acrylic box and (2), 105 ºC ambient inside a thermal chamber. In both conditions, the circuit is soaked for one hour under full load conditions.
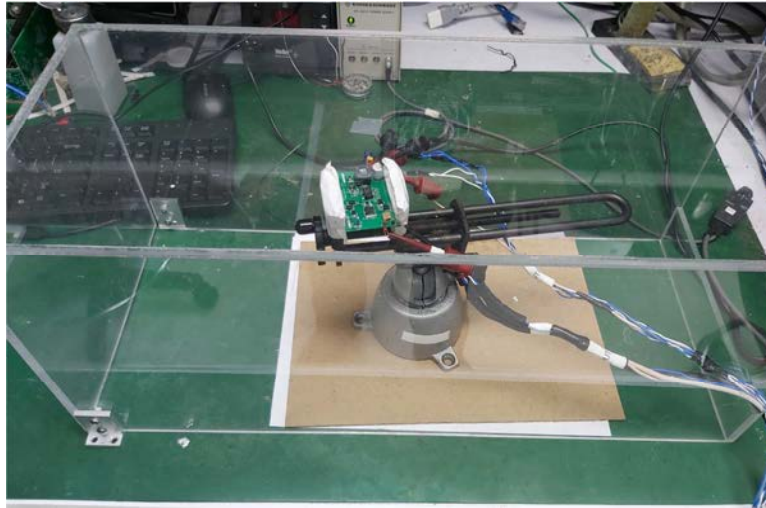


**Figure 103 –** Thermal Performance Set-up Using an Acrylic Box.



**Figure 104 –** Thermal Performance Set-up Using Thermal Chamber.

## 10.2 *Thermal Performance at Room Temperature*

### 10.2.1    60 VDC at Room Temperature

Test Condition: 29.7 °C ambient, soak time = 1 hour, full load
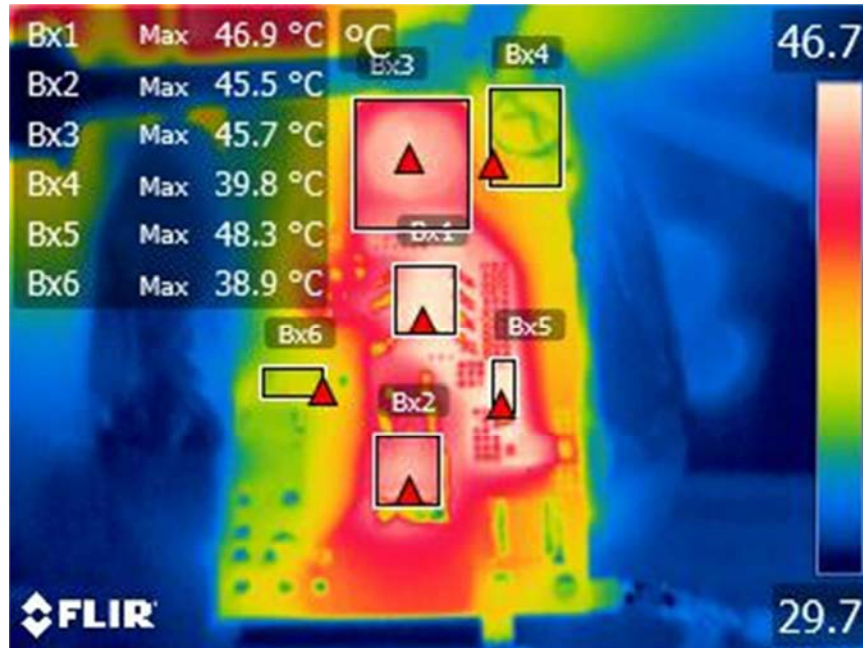


**Figure 105 –** Thermal Performance at 60 VDC Input.

| Component | Temperature (°C) |
|---|---|
| Ambient | 29.7 |
| LNK3206GQ (U1) | 46.9 |
| StackFET (Q1) | 45.5 |
| Output Inductor (L1) | 45.7 |
| Output Capacitor (C2) | 39.8 |
| Freewheeling Diode (D1) | 48.3 |
| Clamp Zener (VR3) | 38.9 |

## 10.2.2    950 VDC at Room Temperature

Test Condition: 29.3 °C ambient, soak time = 1 hour, full load
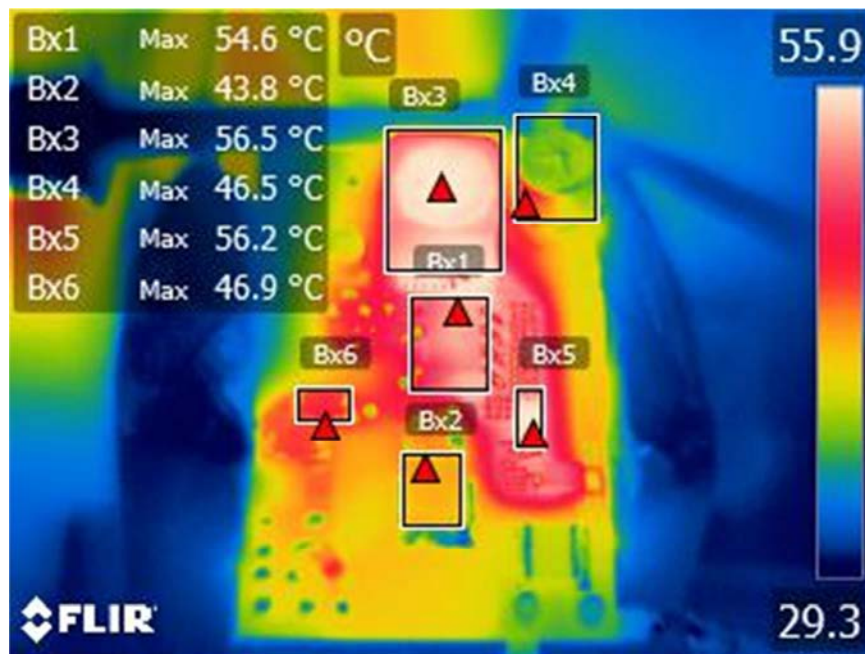


**Figure 106 –** Thermal Performance at 950 VDC Input.

| Component | Temperature (°C) |
|---|---|
| Ambient | 29.3 |
| LNK3206GQ (U1) | 54.6 |
| StackFET (Q1) | 43.8 |
| Output Inductor (L1) | 56.5 |
| Output Capacitor (C2) | 46.5 |
| Freewheeling Diode (D1) | 56.2 |
| Clamp Zener (VR3) | 46.9 |

### 10.2.3    1100 VDC at Room Temperature

Test Condition: 29.3 °C ambient, soak time = 1 hour, full load
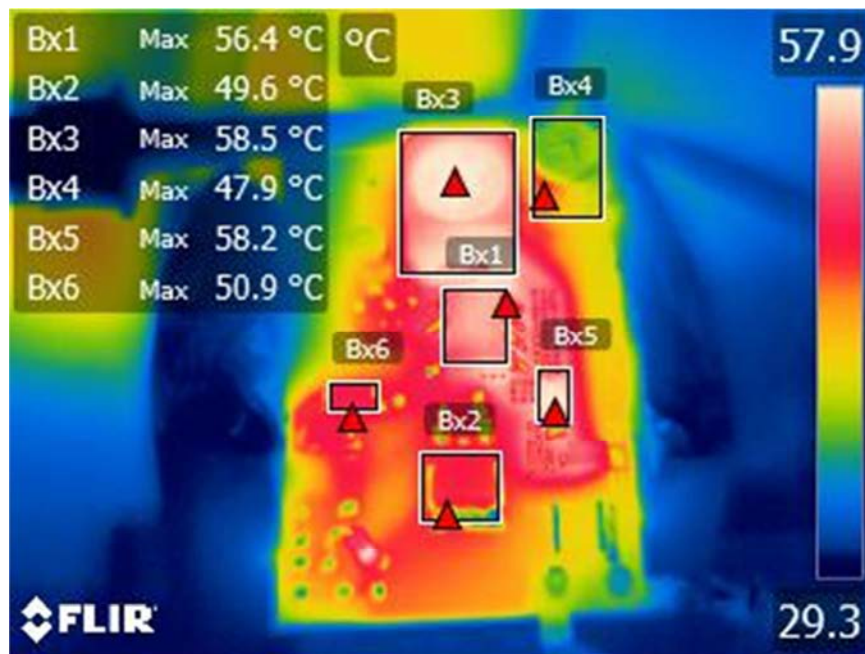


**Figure 107 –** Thermal Performance at 1100 VDC Input.

| Component | Temperature (°C) |
|---|---|
| Ambient | 29.3 |
| LNK3206GQ (U1) | 56.4 |
| StackFET (Q1) | 49.6 |
| Output Inductor (L1) | 58.5 |
| Output Capacitor (C2) | 47.9 |
| Freewheeling Diode (D1) | 58.2 |
| Clamp Zener (VR3) | 50.9 |

## 10.3    *Thermal Performance at 105 ºC*

### 10.3.1    60 VDC at 105 ºC Ambient
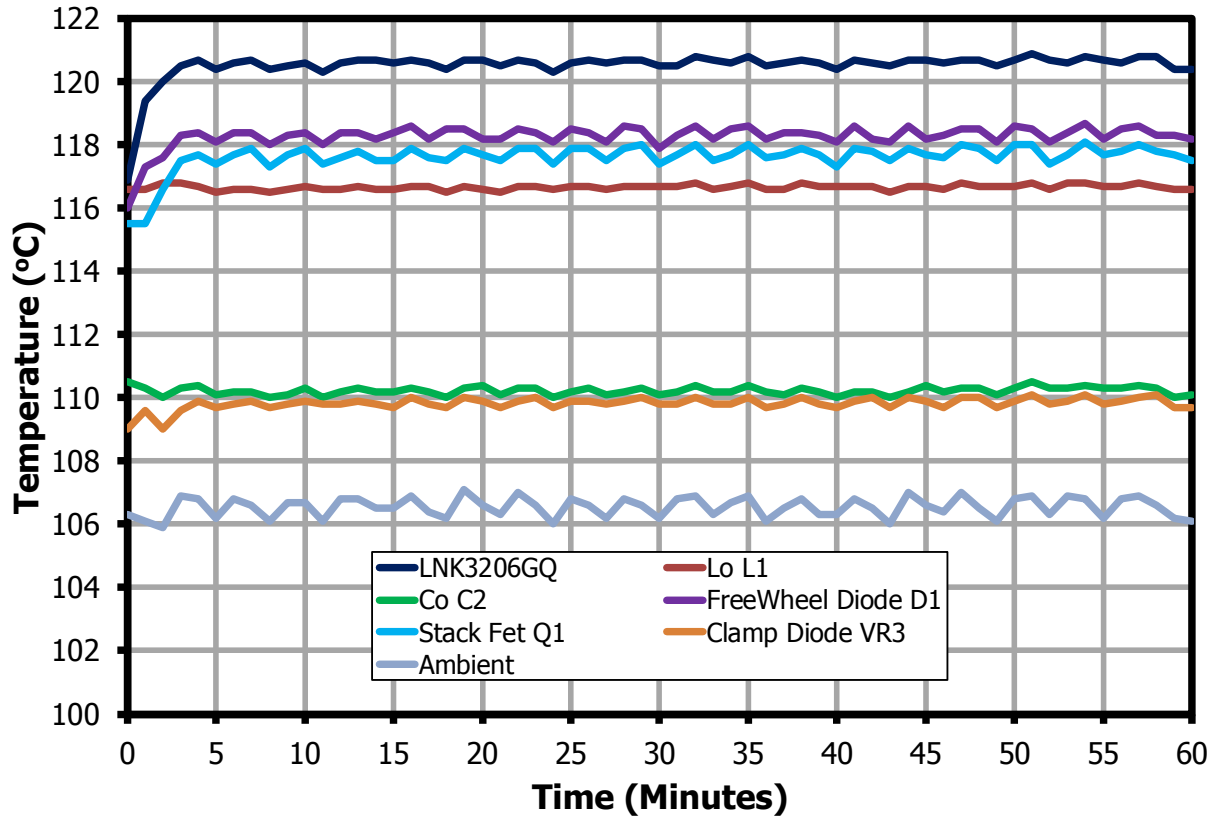


**Figure 108 –** Thermal Performance 60 VDC input at 105 ºC.

| Component | Temperature (°C) |
|---|---|
| Ambient | 106.1 |
| LNK3206GQ (U1) | 120.4 |
| StackFET (Q1) | 117.5 |
| Output Inductor (L1) | 116.6 |
| Output Capacitor (C2) | 110.1 |
| Freewheeling Diode (D1) | 118.2 |
| Clamp Zener (VR3) | 109.7 |

## 10.3.2    950 VDC at 105 ºC Ambient
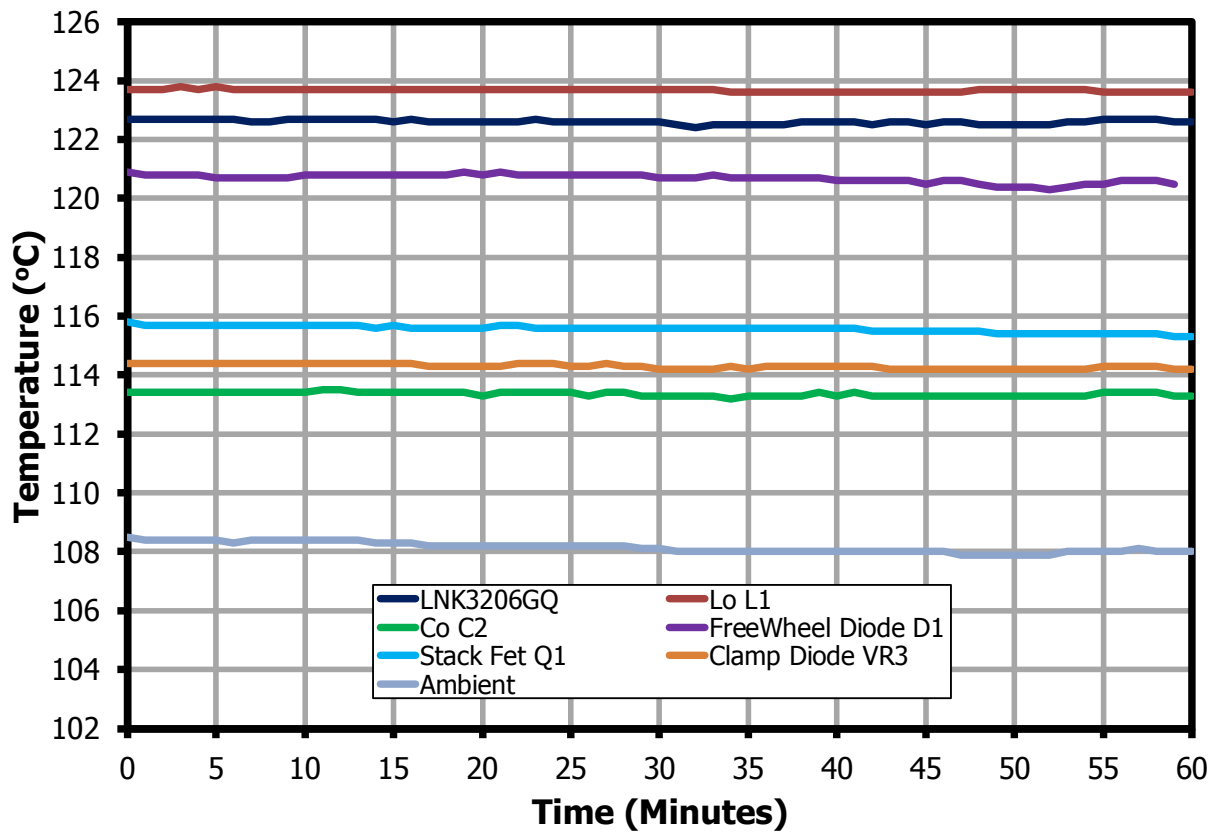


**Figure 109 –** Thermal Performance 950 VDC input at 105 ºC.

| Component | Temperature (°C) |
|---|---|
| Ambient | 108 |
| LNK3206GQ (U1) | 122.6 |
| StackFET (Q1) | 115.3 |
| Output Inductor (L1) | 123.6 |
| Output Capacitor (C2) | 113.3 |
| Freewheeling Diode (D1) | 120.5 |
| Clamp Zener (VR3) | 114.2 |

### 10.3.3    1100 VDC at 105 ºC Ambient
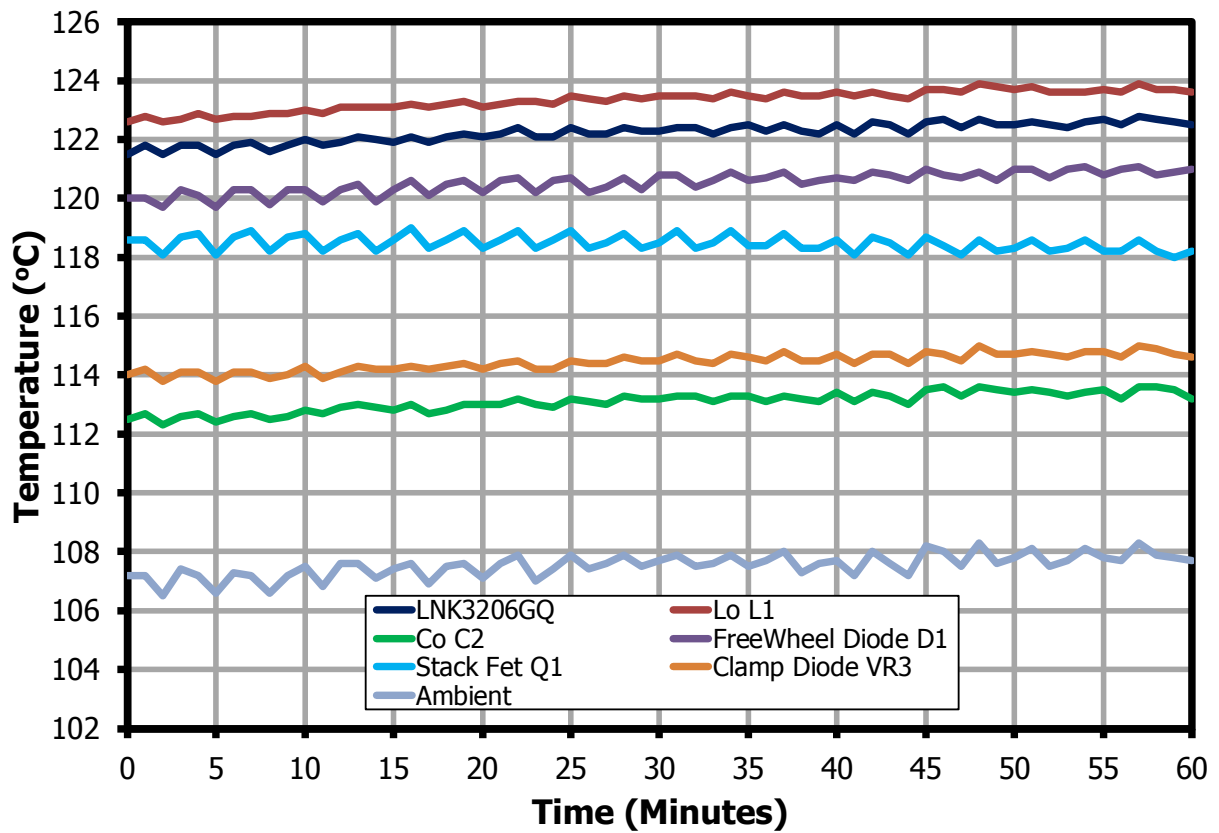


**Figure 110 –** Thermal Performance 1100 VDC input at 105 ºC.

| Component | Temperature (°C) |
|---|---|
| Ambient | 107.7 |
| LNK3206GQ (U1) | 122.5 |
| StackFET (Q1) | 118.2 |
| Output Inductor (L1) | 123.6 |
| Output Capacitor (C2) | 113.2 |
| Freewheeling Diode (D1) | 121 |
| Clamp Zener (VR3) | 114.6 |

## 11  **Revision History**

| Date | Author | Revision | Description and Changes | Reviewed |
|------|--------|----------|-------------------------|----------|
| 07-Jan-21 | RPA | 1.0 | Initial Release. | Apps & Mktg |
| 23-Jul-21 | KM | 1.1 | Minor Formatting Change. | Mktg |
| | | | | |
| | | | | |

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