Application Note AN-55
HiperLCS Family

Design Guide

Introduction

The HiperLCS™ is a family of integrated circuits which combines an LLC controller, a low and a high-side driver, and two half-bridge MOSFETs in a single package.

This Application Note provides information for designing an LLC converter using the HiperLCS device.

Scope

This document is intended for designers who have some familiarity with LLC converters. It covers details of HiperLCS operation, provides design guidelines for high frequency integrated transformers, and an instructional guide for the use of the HiperLCS PIXls Spreadsheet which is part of the PI Expert™ suite. Please download the latest version from www.power.com or if already installed, update via the "Check Latest Updates" feature found under the Help menu

Application information is also shown in the HiperLCS data sheet, including a basic explanation of resonant tank value selection and circuit board layout guidelines. As that information is not repeated in this document, the data sheet should also be used for guidance.

Step-by-Step Design Procedure Using PIXls Spreadsheet

Overview of Spreadsheet

The HiperLCS Spreadsheet is a design tool to assist in creating a first-pass LLC design, and to subsequently iterate parameters to meet the design goals. The spreadsheet uses a steady-state LLC switching model for improved accuracy, instead of the more common, simplistic "First Harmonic Analysis" LLC model which is based on pure sinusoidal waveforms and phasor analysis.

The spreadsheet provides:

- Starting values for L_{PRI}, L_{RES}, C_{RES} and turns ratio
- Starting values for transformer turns and wire size
- Calculations for transformer current and flux density
- Calculations for losses
- Calculations for operating frequency at nominal and minimum input voltage, and other operating parameters
- A graph for comparing two designs
- Passive component values for HiperLCS

See Figure 1 for an example of a design derived using this spreadsheet.

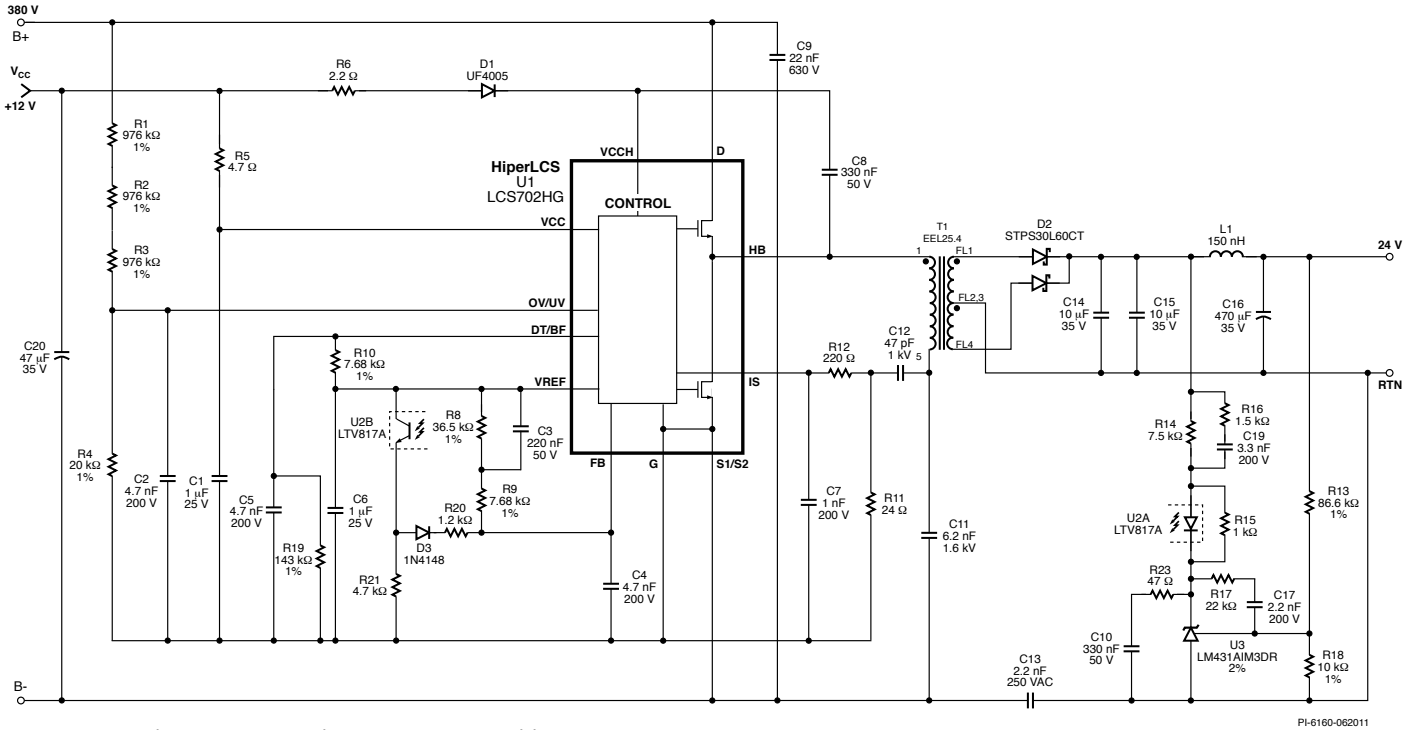

Figure 1. Example Design Generated using HiperLCS Spreadsheet.

Note that for a 2 output design, this spreadsheet assumes an "AC stacked" secondary. (See Figures 4 and 5 for examples. Figures 61, 62 and 63 in Appendix B show non-preferred alternatives to AC Stacking.)

The spreadsheet is organized into sections and columns. The section titles are in bold capitalized text. The columns are "Parameter Names", "INPUTS", "INFO", "OUTPUTS", "UNITS", and "Comments".

In the "INPUTS" column, those cells which have a gray back-ground are user-changeable inputs. The "OUTPUTS" cells will reflect what the user has entered. Some input cells, if left blank, will result in an auto-calculation of suggested values. These will be shown in the corresponding output cell. For example, L_{PRI} is an input. If it is left blank, a recommended value will be calculated. It will appear in the output column. These auto-calculated values are recommended for use in an initial design. The designer can then iterate the values in order to achieve design goals.

Those cells which have no corresponding gray cell in the input column are outputs only. These are calculated and are not directly user-changeable. They may be changed indirectly by changing an input variable. For example, $V_{BROWNIN}$ is calculated from a user input, $V_{BROWNOUT}$. To change $V_{BROWNIN}$, $V_{BROWNOUT}$ needs to be changed.

The "INFO" column will show warnings and errors. The "Comments" column usually contains a short description of the parameter. If there is a warning or error, the comments column will instead display an explanation of the warning/error.

Step 1: Enter Input Parameters

Enter Input Parameters				
VBULK_NOM		380	V	Nominal LLC input voltage
Vbrownout		280	V	Brownout threshold voltage. HiperLCS will shut down if voltage drops below this value. Allowable value is between 65% and 76% of VBULK_NOM. Set to 65% for max holdup time
Vbrownin		353	V	Startup threshold on bulk capacitor
VOV_shut		465	V	OV protection on bulk voltage
VOV_restart		448	V	Restart voltage after OV protection.
CBULK		100	uF	Minimum value of bulk cap to meet holdup time requirement; Adjust holdup time and Vbulkmin to change bulk cap value
tHOLDUP		21.8	ms	Bulk capacitor hold up time

Figure 2. Enter Input Parameter Section from HiperLCS Spreadsheet.

V_{BULK_NOM} is the nominal input (bulk capacitor) voltage. The majority of LLC applications will have a PFC pre-regulator front end with a fixed output voltage. For a 265 VAC max input application, the typical PFC output voltage set-point is 380 VDC. For a low-range input design (132 VAC max), the recommended set-point is 190 VDC. However for a 190 VDC design, the primary current is twice as large as at 380 V for the same output power. Thus for the same HiperLCS losses, a much larger device, with 1/4 the R_{DS-ON}, is required. A higher input voltage set-point will tend to yield higher LLC efficiency, but will tend to reduce PFC efficiency.

The recommended V_{BULK_NOM} range for HiperLCS is 180 V to 450 V. Lower input voltages will tend to produce sub-optimal efficiency. Spreadsheet calculations for nominal conditions assume an input voltage equal to V_{BULK_NOM}.

The HiperLCS senses input voltage on its OV/UV pin via a resistor divider. At power-up, as V_{BULK} rises, HiperLCS will turn on at $V_{BROWNIN}$. If HiperLCS is already running and the input voltage drops, it will turn off at $V_{BROWNOUT}$, the minimum input voltage for the design.

V_{OV_SHUT} is the input overvoltage protection set-point. This feature is used to protect against line voltage swells. The HiperLCS will turn off if V_{OV_SHUT} is exceeded. It will perform a soft-start when V_{BULK} comes back down to $V_{OV\_RESTART}$. The following ratios are fixed:

- V_{OV_SHUT} to $V_{OV\_RESTART}$
- $V_{OV\_RESTART}$ to $V_{BROWNIN}$
- $V_{BROWNIN}$ to $V_{BROWNOUT}$

If different ratios are necessary, additional components can be added to the OV/UV divider.

$V_{BROWNOUT}$ must be between 65% and 76% of V_{BULK_NOM}. If $V_{BROWNOUT}$ is set above this range, $V_{BROWNIN}$ will be greater than V_{BULK_NOM}, and the HiperLCS will not start-up at nominal input voltage. If $V_{BROWNOUT}$ is below this range, the $V_{OV\_RESTART}$ point will be below V_{BULK_NOM}, and the HiperLCS will not restart after a voltage swell event that triggers V_{OV_SHUT}.

For maximum hold-up time, set $V_{BROWNOUT}$ to 65% of V_{BULK_NOM}. The designer may choose to use a higher $V_{BROWNOUT}$ voltage than this. In some cases, this will allow a transformer with a high leakage inductance to be used. It also decreases the peak current during brown-out.

The spreadsheet will default to a C_{BULK} value calculated at 66% of the output power (for V_{BULK_NOM} = 380 V). The hold-up time, t_{HOLDUP}, is the hold-up time calculated from C_{BULK}, input power, V_{BULK_NOM}, and $V_{BROWNOUT}$. When the PFC turns off or the AC supply is removed, t_{HOLDUP} is the time for the bulk capacitor to discharge from V_{BULK_NOM} to $V_{BROWNOUT}$ at full load. If a different hold-up time is desired, enter a new value for C_{BULK}.

Step 2: Enter LLC (Secondary) Outputs

Enter LLC (secondary) outputs				The spreadsheet assumes AC stacking of the secondaries
VO1	24.00	24.0	V	Main Output Voltage. Spreadsheet assumes that this is the regulated output
IO1	6.00	6.0	A	Main output maximum current
VD1		0.70	V	Forward voltage of diode in Main output
PO1		144	W	Output Power from first LLC output
VO2		0.0	V	Second Output Voltage
IO2		0.0	A	Second output current
VD2		0.70	V	Forward voltage of diode used in second output
PO2		0.00	W	Output Power from second LLC output
P_LLC		144	W	Specified LLC output power

Figure 3. Enter LLC (Secondary) Outputs Section from HiperLCS Spreadsheet.

This spreadsheet is designed for a maximum of two output voltages. VO_1 and VO_2 refer to the two output voltages. If there is only one output, leave VO_2 and IO_2 blank. For a two output design, VO_1 is used to calculate the "Secondary Turns" in the main Resonant Parameter section. Either VO_1 or VO_2 can be the higher output voltage, and either one can have the higher output current or higher power. See Figure 4 and Figure 5.

IO_1 and IO_2 are the rated output currents. V_{D1} and V_{D2} refer to the diode voltage drops. A 30 V rated Schottky diode may have a drop as low as 0.3 V. A 200 V PN diode may be > 0.8 V. Synchronous rectifiers may be as low as 0.05 ~ 0.2 V.

PO_1 and PO_2 are the calculated rated output power of the two outputs. P_{LLC} is the calculated total output power.

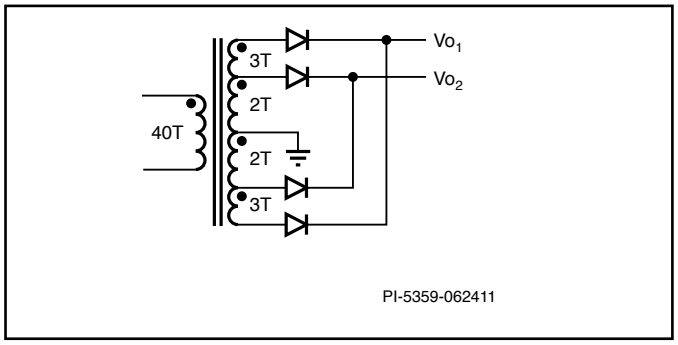

Figure 4. Schematic Showing VO_1 Voltage Greater Than VO_2. "Secondary Turns", Which Always Refer to VO_1, in This Case is 5. "Sec 1 Turns" is 2, and "Sec 2 Turns" is 3.

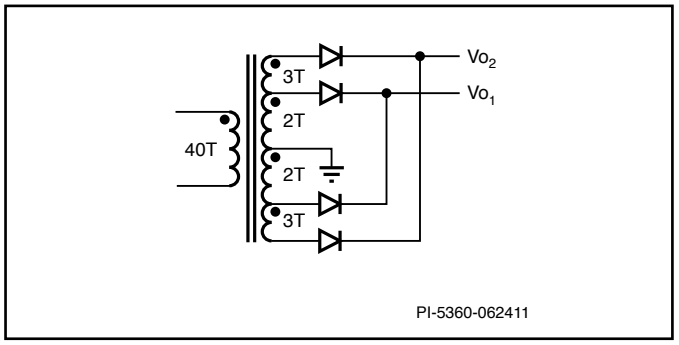

Figure 5. Schematic Showing VO_2 Voltage Greater Than VO_1. "Secondary Turns", Which Always Refer to VO_1, in This Case is 2. "Sec 1 Turns" is 2, and "Sec 2 Turns" is 3.

Step 3: LCS Device Selection

LCS Device selection				
Device	Auto	LCS701		LCS Device
RDSON (MAX)		1.86	ohms	RDSON (max) of selected device
Coss		187	pF	Equivalent Coss of selected device
Cpri		40	pF	Stray Capacitance at transformer primary
PCOND_LOSS		1.8	W	Conduction loss at nominal line and full load
TMAX_HS		90	deg C	Maximum heatsink temperature
Theta J-HS		9.5	deg C/W	Thermal resistance junction to heatsink (with grease and no insulator)
Expected Junction temperature		107	deg C	Expectd Junction temperature
Ta max		50	deg C	Expected max ambient temperature
Theta HS-A		23	deg C/W	Required thermal resistance heatsink to ambient

Figure 6. LCS Device Selection Section from HiperLCS Spreadsheet.

Using Auto selection in the drop-down box of the Device input column selects the minimum device size for the load specification. This yields minimum cost. The maximum recommended device size for 250 kHz operation is approximately 3x larger (1/3rd R_{DS-ON}) than the minimum size. To use larger devices, a lower operating frequency is recommended, due to large MOSFET total C_{OSS} requiring longer ZVS slew times.

C_{PRI} is the parasitic capacitance in parallel with the transformer primary. The sum of C_{OSS} and C_{PRI} influence the maximum recommended L_{PRI}. Larger total capacitance requires larger primary magnetizing current to achieve ZVS at low input voltage, and thus requires a lower L_{PRI}.

$R_{DS-ON(MAX)}$ is used for calculating the device losses, P_{COND_LOSS}. T_{MAX_HS} is the specified maximum HiperLCS heat sink temperature. This temperature, the specified max ambient temperature T_{A-MAX}, and P_{COND_LOSS}, directly affect the required heat sink-to-ambient thermal resistance, θ_{HS-A}. Heat sink physical size is inversely proportional to θ_{HS-A}.

Step 4: LLC Resonant Parameters and Transformer Calculations

LLC Resonant Parameter and Transformer Calculations (generates red curve)				
Po		148	W	Output from LLC converter including diode loss
Vo		24.70	V	Main Output at transformer windings (includes diode drop)
f_target		250	kHz	Desired full load switching frequency of PFC and LLC. 66 kHz to 300 kHz, recommended 250 kHz
Lpar		291	uH	Parallel inductance. (Lpar = Lopen - Lres for integrated transformer; Lpar = Lmag for non-integrated low-leakage transformer)
Lpri		364	uH	Primary open circuit inductance for integrated transformer; for low-leakage transformer it is sum of primary inductance and series inductor. If left blank, auto-calculation shows value necessary for loss of ZVS at 80% of Vnom
Lres		72.8	uH	Series inductance or primary leakage inductance of integrated transformer; if left blank auto-calculation is for K=4
Kratio		4.0		Ratio of Lpar to Lres. Maintain value of K such that 2.1 < K < 11. Preferred Lres is such that K<7.
Cres		5.6	nF	Series resonant capacitor. Red background cells produce red graph. If Lpar, Lres, Cres, and n_RATIO_red_graph are left blank, they will be auto-calculated
Lsec		5.203	uH	Secondary side inductance of one phase of main output; measure and enter value, or adjust value until f_predicted matches what is measured ;
m		50	%	Leakage distribution factor (primary to secondary). 99% signifies most of the leakage is in primary side
n_eq		7.48		Turns ratio of LLC equivalent circuit ideal transformer
Npri		50.2		Primary number of turns; if input is blank, default value is auto-calculation so that f_predicted = f_target
Nsec		6.0		Secondary number of turns (each phase of Main output). Default value is estimate to maintain BAC<=2000 Gauss
f_predicted		250	kHz	Expected frequency at nominal input voltage and full load; Heavily influenced by n_Ratio and primary turns
f_res		250	kHz	Series resonant frequency (defined by series inductance Lres and C)
f_brownout		177	kHz	Switching frequency at VBULK_MIN, full load
f_par		112	kHz	Parallel resonant frequency (defined by Lpar + Lres and C)
f_inversion		161	kHz	Min frequency, at Vbrownout and full load. Set HiperLCS minimum frequency to this value. Operation below this frequency results inoperation in gain inversion region
Vinversion		251	V	Minimum input voltage of LLC power train before low freq gain inversion point. Optimum value is equal Vbrownout

Figure 7. LLC Resonant Parameter and Transformer Calculations Section from HiperLCS Spreadsheet.

Overview

This section pertains to the LLC resonant tank and integrated transformer design. It recommends values for the resonant tank and the transformer, including: primary inductance, series inductance, resonant capacitor, and transformer turns ratio. Recommended values are shown when these input cells are left blank. These values can be over-ridden. The user specifies the target nominal switching frequency $f_{\_TARGET}$.

This section produces the plots of the power train's full-load operating frequency versus bulk voltage characteristic curve with a red trace. To examine the graph, click the tab at the bottom of the spreadsheet. The graph also presents, in blue, the results from the Virtual Transformer Trial section.

General Procedure for Designing the Integrated Transformer and Resonant Tank Parameters

1. Use the spreadsheet to determine an initial design. Examine f_{RES} (series resonant frequency). Adjust N_{PRI} in the spreadsheet in order to adjust $f_{PREDICTED}$ (nominal operating frequency) above or below f_{RES} as desired. An $f_{PREDICTED}$ about 4-9% below f_{RES} (operation below resonance, discontinuous output diode currents) is recommended. Enter a lower resonant capacitance value to raise f_{RES} if a higher $f_{PREDICTED}$ is desired.
2. Build a test transformer to measure leakage inductance. Magnet wire with the same diameter as the recommended Litz can be substituted. Use the Primary and Secondary sections in the spreadsheet to assist in selecting bobbin and Litz wire size.
3. Enter the measured leakage inductance into the spreadsheet to determine if it is acceptable (producing $2.5 < K_{RATIO} < 7$)

   where $$K_{RATIO} = \frac{L_{PRI}}{L_{RES}} - 1$$

Note that the spreadsheet cannot perform calculations with $K_{RATIO} < 2$ or $K_{RATIO} > 12$. An error message will be generated.

4. If leakage inductance is not acceptable, modify transformer design; the Virtual Transformer Trial section can be used to predict the change in leakage inductance from changing primary and secondary turns. If changing secondary turns, maintain the turns ratio.
5. Build actual transformer using Litz wire with one or two extra turns in the primary. It is easier to remove a turn later than to add one. The extra wire can be used to accommodate a current probe.
6. Enter actual N_{PRI}, N_{SEC} measured L_{PRI}, L_{RES} and C_{RES} into the spreadsheet.

7. Power-up the LLC at approximately 50% load and determine in-circuit series resonant frequency by adjusting input voltage until primary current is close to a pure sinusoid (see Figure 25, in the LLC Waveform Analysis section of this document) and note frequency and input voltage; this voltage is called $V_{INPUT(RESONANCE)}$. This assumes the waveforms are normal and don't show asymmetry due to layout and transformer secondary winding problems.
8. Adjust L_{RES} in spreadsheet to reflect actual resonant frequency. This value is accurate because it includes the parasitic inductances in the secondary.
9. Temporarily enter input voltage from step 7 into V_{BULK_NOM}.
10. Adjust the spreadsheet value of L_{SEC} until $f_{PREDICTED}$ and f_{RES} match the actual frequency.
11. At this point the spreadsheet has an accurate model of the transformer, including the leakage distribution factor 'm'. This improves the accuracy of the prediction to "what if" changes in the Virtual Transformer Trial section
12. Change V_{BULK_NOM} back to the nominal value.
13. Open-circuit primary inductance, L_{PRI}, affects the range over which the LLC will operate with full ZVS. Look for the point where slight loss of ZVS due to insufficient magnetizing energy, begins at low-line / full load, and at high-line / full load and minimum load. (See Figures 30 thru 33 in the LLC Waveform Analysis section of this document). Reduce primary inductance if needed, to increase range of ZVS operation, or vice versa. Partial loss of ZVS during brown-out (not steady-state) is acceptable, in order to allow higher primary inductance for increased efficiency. Verify that the dead-time is a reasonable compromise between the needs of low-line full load (short slew time) and high-line light load (long slew time). (See Figures 29 and Figure 34 in the LLC Waveform Analysis section of this document). Shorter dead-times will truncate the slew at high-line light load, causing earlier high-frequency gain inversion and burst mode operation.
14. If changes to the resonant tank are desired, evaluate the design changes in the Virtual Transformer Trial section. Decrease primary turns to increase $f_{PREDICTED}$. Increase C_{RES} to decrease f_{RES}. Note that reducing primary turns will tend to increase the range of ZVS operation for a given L_{PRI}.
15. Build a new transformer with the desired changes. If the initial transformer was wound with an extra one or two primary turns, these may need to be reduced. Note that the spread-sheet may show a required change to the values for the signal pin resistors.
16. Repeat steps 3 to 13 as needed.
17. Measure thermal performance, efficiency, start-up current, and primary current during brown-out. Iterate transformer as needed.

Overview of Integrated Transformer Equivalent Circuit

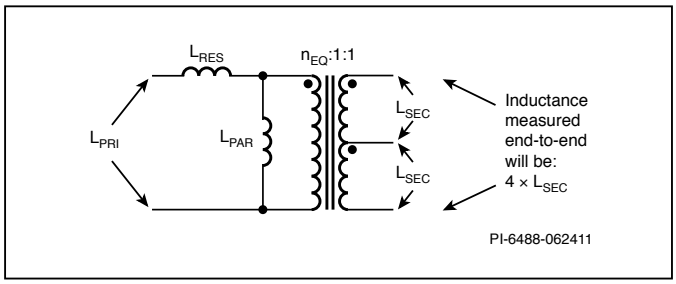

Figure 8. "One Leakage" Integrated Transformer Equivalent Circuit used in the Spreadsheet. Note That Equivalent Circuit Turns Ratio "n_{EQ}" is the Ratio of Virtual Primary Turns to One Phase of the Secondary.

The integrated transformer equivalent circuit that the spread-sheet uses is shown in Figure 8. The transformer is an ideal transformer. Its turns ratio is n_{EQ}:1:1, where n_{EQ} is the "equivalent circuit turns ratio". This is always lower than the actual, physical turns ratio (which is Primary Turns divided by Secondary Turns). Secondary turns is the total number of turns of one phase of the main output, labeled VO_1 in the spreadsheet. L_{PRI} is simply the primary open circuit inductance of the transformer. Series resonant inductance L_{RES} is easily measured by measuring the primary inductance with one phase of the secondary shorted. L_{SEC} is not easily measured due to its very low value. Its value is auto-calculated from the primary inductance, primary and secondary turns, and the leakage distribution factor, m, which defaults to 50% when the L_{SEC} input cell is left blank. To measure L_{SEC}, measure the inductance across both secondary phases together and divide by 4, then enter the value into the spreadsheet. If the user enters a different value of L_{SEC}, a new value of 'm' will be calculated. If a value of L_{SEC} is entered which produces a value of 'm' that is less than 1% or greater than 99%, a warning will appear.

Instead of measuring the actual L_{SEC}, the user can build and test the transformer, and then adjust the value of L_{SEC} in the spreadsheet until $f_{PREDICTED}$ matches the actual circuit operation (assuming the other parameters, L_{PRI}, L_{RES} and C_{RES} are all accurate). This includes the effect of the parasitic layout inductance from the secondary, through the output diode, to the main output capacitors. This improves the spreadsheet model accuracy, which will also improve the accuracy of the "Virtual Transformer Trial" section, used for "what if" scenarios, which the user can use to iterate the design.

The "one leakage inductance" model in Figure 8 is a simplifi-cation of another, more complex, commonly used integrated transformer equivalent circuit, in which the primary and secondary leakage inductances are separated. It is called the "two leakage inductance" model. The 2 models are equivalent to each other, and the one leakage inductance integrated transformer model adequately describes the LLC circuit. The two leakage inductance model is not used here, and is described in the Appendix A for reference only.

Primary inductance

The recommended primary inductance is an estimated value which results in ZVS operation down to approximately 80% of the nominal V_{BULK}, at full load. As input voltage is reduced, an LLC converter will start to lose ZVS operation at some point, depending on primary inductance. The primary inductance of the transformer is adjusted by modifying the size of the core gap. Changing the core gap has little influence on the leakage inductance L_{RES}.

The recommended inductance is a function of target frequency, HiperLCS MOSFET Drain capacitance (C_{OSS}), transformer primary stray capacitance, and rated power. If full ZVS operation is desired down to an even lower input voltage, reduce the primary inductance. This increases primary magnetizing circulating current and thus increases the energy available to charge and discharge the primary capacitances. The disadvantage is increased primary losses and reduced efficiency at nominal input voltage.

The actual input voltage at which partial loss of ZVS begins cannot be accurately predicted because it is highly dependent on many factors including output diode capacitance and secondary layout symmetry. Asymmetry causes one edge to lose ZVS much earlier than the other edge. Partial loss of ZVS at low-line is acceptable if low-line operation is not a steady–state operating condition. Any loss of ZVS at steady-state condition is not recommended. Severe loss of ZVS during a non-steady-state condition is also not recommended. If during testing, it is determined that partial loss of ZVS at some very low input voltages (above $V_{BROWNOUT}$) can be tolerated, then primary inductance can be increased.

Resonant Inductance and Capacitance

The resonant inductance in the spreadsheet, L_{RES}, is shown in Figure 8. It is measured at the primary terminals with one phase of the secondary shorted. This inductance resonates with the resonant capacitance C_{RES}, at the series resonant frequency f_{SER}. If left blank, the spreadsheet auto-calculates a recommended value of L_{RES}, yeilding a K_{RATIO} of 4.

A value of L_{RES} that yields a K_{RATIO} of 2.5 to 7 will produce an acceptable design. A K_{RATIO} much higher than 7 will produce a design that has a low $f_{BROWNOUT}$ (frequency at low-line), high peak and RMS currents at brown-out, and a long slew time at light load. The low $f_{BROWNOUT}$ may be acceptable from the point of view of core saturation and output ripple voltage during brown-out. However, the long slew time at light load may result in an early light load gain inversion point, which may produce burst mode at medium loads.

The following values are calculated in this section:

$f_{PREDICTED}$: This is the predicted switching frequency at full load and V_{BULK_NOM}. The turns ratio has the greatest influence on this value. The recommended turns ratio is calculated such that $f_{PREDICTED}$ is equal to f_{TARGET}. The LLC will operate at resonance, at V_{BULK_NOM}.

N_{PRI}: Transformer primary turns. The suggested value is such that the LLC will operate at resonance, at V_{BULK_NOM}.

N_{SEC}: Transformer secondary turns. This is a user input. If left blank, it shows an auto-calculation based on the selected core and a target AC flux density (B_{AC}) of 120 mT (p-p).

$f_{INVERSION}$ and $V_{INVERSION}$ are the frequency and input voltage at which the power train gain will invert at full load. Do not confuse this with light load gain inversion. This point represents the maximum resonant gain of the LLC power train. $V_{INVERSION}$ must be less than $V_{BROWNOUT}$. Note that loss of ZVS will begin at an input voltage greater than $V_{INVERSION}$. Depending on the value of L_{PRI}, slight loss of ZVS can occur at a voltage higher than $V_{BROWNOUT}$. This is acceptable if it is not a steady-state condition.

Step 5: RMS Currents and Voltages

RMS CURRENTS AND VOLTAGES				
IRMS_LLC_Primary		0.97	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and fnominal_actual
Winding 1 (Lower secondary Voltage) RMS current		4.8	A	Winding 1 (Lower secondary Voltage) RMS current
Lower Secondary Voltage Capacitor RMS current		3.0	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current		0.0	A	Winding 2 (Higher secondary Voltage) RMS current
Higher Secondary Voltage Capacitor RMS current		0.0	A	Higher Secondary Voltage Capacitor RMS current
Cres_Vrms		111	V	Resonant capacitor AC RMS Voltage at full load and nominal input voltage

Figure 9. RMS Currents and Voltages Section from HiperLCS Spreadsheet.

This section calculates the RMS currents in the primary, Winding 1, Winding 2, the output capacitors, and the main resonant capacitor.

Step 6: Virtual Transformer Trial - (generates blue curve)

Virtual Transformer Trial - (generates blue curve)				
New primary turns		50.2		Trial transformer primary turns; default value is from resonant section
New secondary turns		6.0		Trial transformer secondary turns; default value is from resonant section
New Lpri		364	uH	Trial transformer open circuit inductance; default value is from resonant section
New Cres		5.6	nF	Trial value of series capacitor (if left blank calculated value chosen so f_res = f_target
New estimated Lres		72.8	uH	Trial transformer estimated Lres
New estimated Lpar		291	uH	Estimated value of Lpar for trial transformer
New estimated Lsec		5.203	uH	Estimated value of secondary leakahe inductance
New Kratio		4.0		Ratio of Lpar to Lres for trial transformer
New equivalent circuit transformer turns ratio		7.48		Estimated effective transformer turns ratio
V powertrain inversion new		251	V	Voltage on Bulk Capacitor below which ZVS is lost
f_res_trial		250	kHz	New Series resonant frequency
f_predicted_trial		250	kHz	New nominal operating frequency
IRMS_LLC_Primary		0.97	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and f_predicted_trial
Winding 1 (Lower secondary Voltage) RMS current		4.8	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Lower Secondary Voltage Capacitor RMS current		3.0	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current		4.8	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Higher Secondary Voltage Capacitor RMS current		0.0	A	Higher Secondary Voltage Capacitor RMS current

Figure 10. Virtual Transformer Trial Section from HiperLCS Spreadsheet.

This section is for testing changes to the transformer and resonant parameters. The result is plotted in the graph tab, for easy comparison against the red trace generated by the main Resonant Parameter section. The following variables can be modified, from their default values, (which are copied by the spreadsheet from the Main Resonant section), so that the results can be examined: N_{PRI}, N_{SEC}, L_{PRI}, and C_{RES}. The calculated results are shown. This section influences no other sections in the spreadsheet. The default values are the same as the values in the main resonant section, so that the blue trace will be behind the red trace and cannot be seen. Once the user overrides any value, the blue trace will appear. See Figure 22.

Step 7: Transformer Core Calculations

TRANSFORMER CORE CALCULATIONS (calculates from resonant parameter section)				
Transformer Core	**Auto**	**EEL25**		**Transformer Core**
Ae		0.4	cm^2	Enter transformer core cross-sectional area
Ve		3.0	cm^3	Enter the volume of core
Aw		107.9	mm^2	Area of window
Bw		22.0	mm	Total Width of Bobbin
Loss density		200.0	mW/cm^3	Enter the loss per unit volume at the switching frequency and BAC (Units same as kW/m^3)
MLT		3.1	cm	Mean length per turn
N_CHAMBERS		2.0		Number of Bobbin chambers
W_SEP		3.0	mm	Winding separator distance (will result in loss of winding area)
Ploss		0.6	W	Estimated core loss
Bpkfmin		144	mT	First Quadrant peak flux density at minimum frequency.
BAC		204	mT	AC peak to peak flux density (calculated at f_predicted, Vbulk at full load)

Figure 11. Transformer Core Calculations Section from HiperLCS Spreadsheet.

This section calculates core loss and flux density. The user can select the core from the drop-down box. If left blank, the spreadsheet will auto select a core based on the total output power, assuming operation at 250 kHz. A custom core can be entered by overriding the values for the core specifications. These are: core area (A_e), core volume (V_e), winding cross sectional window area (A_W), bobbin winding width (B_W), and mean length per turn (MLT). The auto calculation for primary and secondary turns in the Resonant Section (N_{PRI} and N_{SEC}), is dependent on the core selection.

The variable $n_{CHAMBERS}$ refers to the number of winding chambers in the bobbin. A typical integrated transformer will use two or three chambers. This number, along with the variable W_{SEP} (winding separator thickness), is used to calculate the loss of available winding space due to the divider. This calculation is used to auto calculate the Primary and Secondary wire gauges and to calculate winding losses.

See Figure 12 for photos of 2 and 3 chamber bobbins.

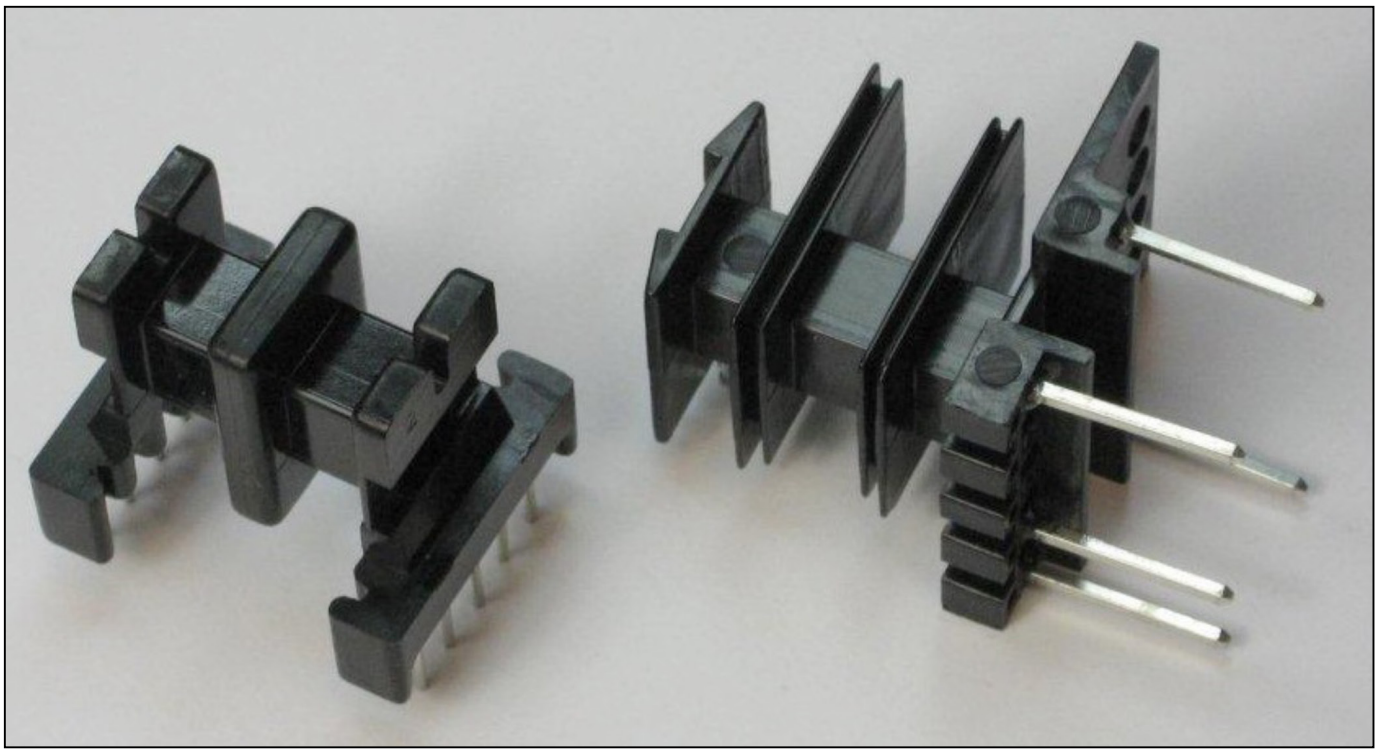

Figure 12. Example of 2-Chamber (left) and 3-Chamber (right) Bobbin.

See Figure 13 for drawings showing examples of 2 and 3 chamber bobbins and also illustrating W_{SEP} of 3 mm.

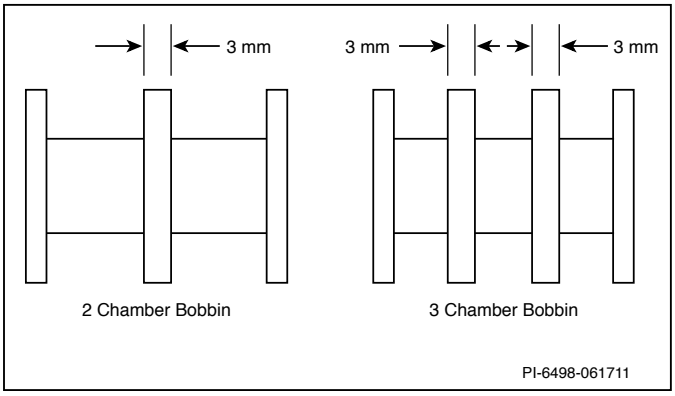

Figure 13. Example of 2-Chamber (left) and 3-Chamber (right) Bobbins with W_{SEP} = 3 mm.

Step 8: Primary Winding

PRIMARY WINDING				
Npri		50.2		Number of primary turns; determined in LLC resonant section
Primary gauge		44	AWG	Individual wire strand gauge used for primary winding
Equivalent Primary Metric Wire gauge		0.050	mm	Equivalent diameter of wire in metric units
Primary litz strands		170		Number of strands in Litz wire; for non-litz primary winding, set to 1
Primary Winding Allocation Factor		50	%	Primary window allocation factor - percentage of winding space allocated to primary
AW_P		47	mm^2	Winding window area for primary
Fill Factor		60%	%	% Fill factor for primary winding (typical max fill is 60%)
Resistivity_25 C_Primary		55.46	m-ohm/m	Resistivity in milli-ohms per meter
Primary DCR 25 C		86.18	m-ohm	Estimated resistance at 25 C
Primary DCR 100 C		115.48	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
Primary RMS current		0.97	A	Measured RMS current through the primary winding
ACR_Trf_Primary		184.77	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Primary copper loss		0.17	W	Total primary winding copper loss at 85 C

Figure 14. Primary Winding Section from HiperLCS Spreadsheet.

This section calculates the recommended primary Litz wire gauge and number of strands, and calculates its power loss. Recommended numbers are shown when the corresponding inputs are left blank. Recommended primary Litz wire gauge is a function of f_{TARGET}; higher frequency requires finer Litz gauge to maintain efficiency. Thicker gauge Litz can be used at the expense of increased copper losses and reduced efficiency. The suggested number of strands of the primary Litz wire is calculated to result in a primary fill factor of 60%. The fill factor is the ratio of total copper area (cross-sectional area of each Litz strand times number of strands times the number of turns), to the total primary winding cross sectional window area (A_{WP}).

Refer to Figure 15 for:

- The primary winding area

$$A_{WP} = (A + C) \times d$$

- The secondary winding area

$$A_{WS} = B \times d$$

- The total winding area

$$A_W = (A + B + C) \times d$$

- Therefore the primary winding allocation factor

$$= \frac{A_{WP}}{A_W}$$

When changing the Litz wire gauge or number of strands, check the fill factor. If it is greater than 60% the wire will probably not fit.

This section also calculates the DCR, ACR (which is calculated as a simple multiplier from DCR), and the resulting primary copper loss.

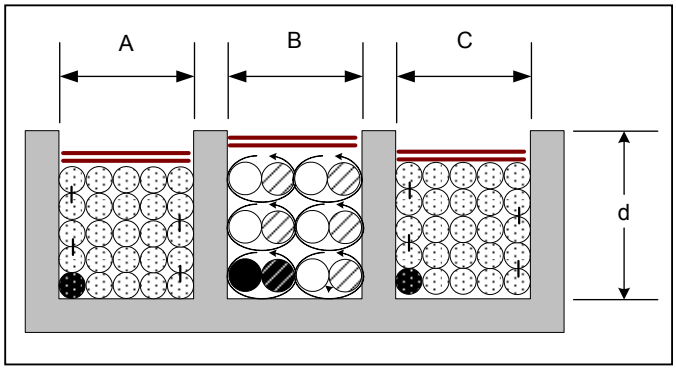

Figure 15. Bobbin Winding Area Allocation Example of a 3 Section Bobbin, Normally A = C.

Step 9: Secondary Winding 1

Secondary winding 1 (Lower secondary voltage OR Single				Note - Power loss calculations are for each winding half of secondary
Output Voltage		24.00	V	Output Voltage (assumes AC stacked windings)
Sec 1 Turns		6.00		Secondary winding turns (each phase)
Sec 1 RMS current (total, AC+DC)		4.8	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Winding current (DC component)		3.00	A	DC component of winding current
Winding current (AC RMS component)		3.70	A	AC component of winding current
Sec 1 Wire gauge		42	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 1 Metric Wire gauge		0.060	mm	Equivalent diameter of wire in metric units
Sec 1 litz strands		494		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec1		12.00	m-ohm/m	Resistivity in milli-ohms per meter
DCR_25C_Sec1		2.23	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec1		2.99	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1		0.22	W	Estimated Power loss due to DC resistance (both secondary phases)
ACR_Sec1		4.78	m-ohm	Measured AC resistance per phase(at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature . Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec1		0.13	W	Estimated AC copper loss (both secondary phases)
Total winding 1 Copper Losses		0.35	W	Total (AC + DC) winding copper loss for both secondary phases
Capacitor RMS current		3.0	A	Output capacitor RMS current
Co1		5.1	uF	Secondary 1 output capacitor
Capacitor ripple voltage		3.0	%	Peak to Peak ripple voltage on secondary 1 output capacitor

Figure 16. Secondary Winding 1 Section from HiperLCS Spreadsheet.

This section is used for either 1 or 2 output designs. For 2 outputs, it pertains to the lower voltage. The next section, "**Secondary Winding 2"**, pertains to the higher voltage winding. Note that in the earlier section **Step 2: "Enter LLC (Secondary) Outputs"**, VO_1 may refer to either the lower or higher output voltage. See Figures 4 and 5. In both Figures, "Section 1 Turns" would be equal to 2.

DC, AC, and total (AC plus DC) RMS currents are calculated. Because AC stacking is recommended and assumed by the spreadsheet, the current in the higher voltage secondary winding (Secondary Winding 2), adds to the current in Secondary Winding 1 (the lower voltage winding).

The recommended Litz wire gauge is a function of switching frequency. Thicker gauge Litz can be substituted at the expense of efficiency. The AC resistance is a simple multiple of DC resistance. Copper loss is calculated from this.

The recommended number of Litz strands calculated for Secondary Winding 1 and Secondary Winding 2, are calculated together, to maximize efficiency. The optimal allocation of space between them is a function of their number of turns and RMS currents. If there is only one output, the whole space for the secondary is allocated to Secondary Winding 1. Section 1 Litz Strands can be changed by the user, but if the change results in a secondary fill factor of >60% when using served Litz, or >75% when using un-served Litz, the windings will probably not fit. Un-served Litz is generally preferred for secondary windings.

Capacitor ripple voltage is the peak-to-peak voltage on the main output capacitors (not the output terminals of the power supply), expressed as a percentage of output voltage, and calculated from the capacitor current wave shape and the capacitive reactance at $f_{PREDICTED}$. This calculation is valid for ceramic capacitors. If electrolytic capacitors are used, their high ESR requires much higher capacitance values. The spreadsheet does not calculate ripple voltage based on ESR. The spread-sheet calculates a recommended value for capacitance, yielding 3% ripple voltage. A smaller capacitance than this yields a larger ripple voltage, which will start to impact efficiency and start to increase output diode reverse voltage stress noticeably. Note that the recommended ceramic dielectric type, X5R, exhibits reduced capacitance with applied voltage. Check the capacitor data sheet for their actual capacitance at the voltage applied in the application.

Step 10: Secondary Winding 2

Secondary winding 2 (Higher secondary voltage)				Note - Power loss calculations are for each winding half of secondary
Output Voltage		0.00	V	Output Voltage (assumes AC stacked windings)
Sec 2 Turns		0.00		Secondary winding turns (each phase) AC stacked on top of secondary winding 1
Sec 2 RMS current (total, AC+DC)		4.8	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Winding current (DC component)		0.0	A	DC component of winding current
Winding current (AC RMS component)		0.0	A	AC component of winding current
Sec 2 Wire gauge		42	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 2 Metric Wire gauge		0.060	mm	Equivalent diameter of wire in metric units
Sec 2 litz strands		0		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec2		59292.53	m-ohm/m	Resistivity in milli-ohms per meter
Transformer Secondary MLT		3.10	cm	Mean length per turn
DCR_25C_Sec2		0.00	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec2		0.00	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1		0.00	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec2		0.00	m-ohm	Measured AC resistance per phase(at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature . Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec2		0.00	W	Estimated AC copper loss (both secondary halves)
Total winding 2 Copper Losses		0.00	W	Total (AC + DC) winding copper loss for both secondary halves
Capacitor RMS current		0.0	A	Output capacitor RMS current
Co2		N/A	uF	Secondary 2 output capacitor
Capacitor ripple voltage		N/A	%	Peak to Peak ripple voltage on secondary 1 output capacitor

Figure 17. Secondary Winding 2 Section from HiperLCS Spreadsheet.

Ignore this section if there is only one output. This section refers to the higher of the two output voltages. For a 2 output design, the spreadsheet assumes AC stacking in performing its calculations. The number of turns "Section 2 Turns" refers to the turns on top of Secondary Winding 1. See Figures 4 and 5. In both Figures, "Section 2 Turns" is equal to 3.

Step 11: Transformer Loss Calculations

Transformer Loss Calculations				Does not include fringing flux loss from gap
Primary copper loss (from Primary section)		0.17	W	Total primary winding copper loss at 85 C
Secondary copper Loss		0.35	W	Total copper loss in secondary winding
Transformer total copper loss		0.52	W	Total copper loss in transformer (primary + secondary)
AW_S		46.59	mm^2	Area of window for secondary winding
Secondary Fill Factor		60%	%	% Fill factor for secondary windings; typical max fill is 60% for served and 75% for unserved Litz

Figure 18. Transformer Loss Calculations Section from HiperLCS Spreadsheet.

This section calculates total secondary copper losses, total transformer copper loss, secondary winding window area (A_{WS}) and Secondary Fill Factor. Cross-sectional area is the area allocated to the secondary, calculated from A_W, B_W, W_{SEP}, $n_{CHAMBERS}$, and Primary Window Allocation Factor. The Secondary Fill Factor is the ratio of the total cross-sectional area of all secondary copper versus the total area available for the secondary.

Step 12: Signal Pins Resistor Values

Signal pins resistor values				
Dead Time		320	ns	Dead time
Burst Mode	Auto	2		Select Burst Mode: 1, 2, and 3 have hysteresis and have different frequency thresholds
f_max		797	kHz	Max internal clock frequency, dependent on dead-time setting
f_burst_start		299	kHz	Lower threshold frequency of burst mode, provides hysteresis. This is switching frequency at restart after a bursting off-period
f_burst_stop		349	kHz	Upper threshold frequency of burst mode; This is switching frequency at which a bursting off-period stops
DT/BF pin upper divider resistor		7.21	k-ohms	Resistor from DT/BF pin to VREF pin
DT/BF pin lower divider resistor		65	k-ohms	Resistor from DT/BF pin to G pin
Rstart		7.21	k-ohms	Start-up resistor - resistor in series with soft-start capacitor; equivalent resistance from FB to VREF pins at startup
Start up delay		0.0	ms	Start-up delay; delay before switching begins. Reduce R_START to increase delay
Rfmin		36.0	k-ohms	Resistor from VREF pin to FB pin, to set min operating frquency; This resistor plus Rstart determine f_MIN
C_softstart		1.0	uF	Softstart capacitor. Recommended values are between 0.1 uF and 10 uF
Ropto		3.7	k-ohms	Resistor in series with opto emitter
OV/UV pin lower resistor		22.0	k-ohm	Lower resistor in OV/UV pin divider
OV/UV pin upper resistor		3.21	M-ohm	Total upper resistance in OV/UV pin divider

Figure 19. Signal Pins Resistor Values Section from HiperLCS Spreadsheet.

This section calculates the values of the resistors on the OV/UV, FEEDBACK, and DT/BF pins. See the schematic in Figure 1.

The majority of designs will require a dead-time between 300 and 360 ns. For a given design, a short dead-time is desirable at low-line and full load, while a longer dead-time is desirable at high-line light load. The dead-time selection will be a compromise between these two. Too long a dead-time at brown-out will cause some loss of ZVS, while too short a dead-time at light load, high-line, will result in early entry into burst mode, by causing the gain to invert (high-frequency gain inversion).

f_{MAX} is an inverse function of the dead-time:

$$f_{MAX}(kHz) = \frac{270000}{Dead - Time(ns)}$$

The part will typically only run at f_{MAX} briefly during start-up. Other than at start-up, it will not switch above $f_{BURST(STOP)}$. Internally, the clock frequency runs at f_{MAX} prior to start-up and during the off period of auto-restart, which is approximately a 131k cycle delay.

There are three Burst Threshold settings: 1, 2, and 3. Burst mode number changes the $f_{BURST(START)}$ and $f_{BURST(STOP)}$ frequencies. They are fixed fractions of f_{MAX}. Refer to the data sheet. $f_{BURST(STOP)}$ minus $f_{BURST(START)}$ is essentially the hysteresis of the burst threshold frequency.

Dead-time and burst mode number are set by a resistor divider on the DT/BF pin from the VREF pin to ground. Dead-time is a function of current entering the DT/BF pin, which has an approximate Thevenin equivalent circuit of 0.66 V and 1.1 kΩ. The burst mode number is a function of the DT/BF pin voltage during a high-impedance voltage detection mode at VCC start-up. Therefore, it is a function of the resistor divider ratio.

R_{START} should be about 10% less than DT/BF pull-up resistor so that the initial frequency at start-up is equal to f_{MAX}. This minimizes primary peak current at start-up. Reducing the value of R_{START} further will introduce an additional start-up delay, which is calculated in the spreadsheet. This is in addition to the 1024 cycle start-up delay at a first start when VCC is applied or in addition to the 131k cycle start-up delay during an auto-restart.

R_{FMIN} + R_{START} set the minimum operating frequency when the optocoupler is completely cut off. This is calculated from $f_{BROWNOUT}$ in the main resonant section.

$C_{SOFTSTART}$ determines the start-up time. The typical value ranges from 0.1 µF to 0.47 µF. The recommended value is the minimum for which the primary start-up current (over 7 consecutive cycles, as opposed to a single-cycle peak) does not exceed the primary current at brown-out and with which start-up ramp up time is not shorter than the PSU's minimum specification. A larger $C_{SOFTSTART}$ than is necessary is not recommended due to the possibility of the HiperLCS not recognizing that it has exited start-up mode. Please see the data sheet.

R_{OPTO} is an optional resistor that improves ESD and surge immunity by reducing the noise current injected into the FEEDBACK (FB) pin. Its maximum value is such that the FEEDBACK pin current is greater than the DT/BF pin current when the optocoupler is completely saturated and the FEEDBACK pin is at 2.0 V. The calculation in the current spreadsheet rev 1.0 contains an error which will be corrected in the next revision. The correct maximum value is:

$$R_{OPTO}(k\Omega) = 400/[(f_{MAX}/2.48) - 1400/(R_{FMIN} + R_{START})]$$

where R_{FMIN} and R_{START} are in kΩ and f_{MAX} is in kHz.

This is to ensure that the design is capable of regulating by bursting at f_{MAX} during start-up mode. This condition occur during unusual circumstances, such as power-up at zero load at very high input voltage. Start-up mode is exited once the device switches at a frequency below $f_{BURST((STOP)}$. Bursting at f_{MAX} should be avoided because it causes severe loss of ZVS and very high internal power dissipation. A smaller $C_{SOFT-START}$ value and a nominal operating frequency below resonance help avoid this condition.

R_{OPTO} also tends to improve output ripple in normal burst mode.

The optocoupler load resistor (R21 in Figure 1), is sized to allow the optocoupler circuit to sink current as needed during burst mode and during large load steps. Without it, the soft-start capacitor will slow down the large signal loop response when the optocoupler needs to cut off, and the output will exhibit large voltage ripple during burst mode, especially at high-line. A 4.7 kΩ value is recommended.

Step 13: LLC Capacitive Divider Current Sense Circuit

LLC capacitive divider current sense circuit				
slow current limit		2.72	A	8-cycle current limit - check postivie half-cycles during brownout and startup
fast current limit		4.89	A	1-cycle current limit - check positive half-cycles during startup
LLC sense capacitor		47	pF	HV sense capacitor, forms current divider with main resonant capacitor
RLLC sense resistor		22.0	ohms	LLC current sense resistor, senses current in sense capacitor
IS pin current limit resistor		220	ohms	Limits current from sense resistor into IS pin when voltage on sense R is < -0.5V
IS pin noise filter capacitor		1.0	nF	IS pin bypass capacitor; forms a pole with IS pin current limit capacitor
IS pin noise filter pole frequency		724	kHz	This pole attenuates IS pin signal

Figure 20. LLC Capacitive Divider Current Sense Circuit Section from HiperLCS Spreadsheet.

The suggested slow current limit is a simple multiple of the nominal primary peak current. It should be adjusted based on actual peak current at brown-out. 15% margin above this value is suggested. The soft-start capacitor value should be large enough so that at start-up, the maximum seven-cycle consecutive peak current is less than the peak current at brown-out. The fast current limit is nominally 1.8x the slow current limit. The first cycle peak current at start-up needs to be below this value. The worst case start-up current is at $V_{OV\_RESTART}$, the bulk voltage at which the HiperLCS restarts after a voltage swell from the AC input.

The HiperLCS IS pin only senses positive current pulses. Negative pulses larger than approximately -0.6 V are clamped. Note that the actual signal reaching the IS pin may be attenuated due to the RC filter formed by the IS pin bypass capacitor and the IS pin series current limiting resistor. (R12 and C7 in Figure 1)

A 47 pF primary current sense capacitor is suggested. This capacitor forms a current divider with the main resonant capacitor. The sense resistor value which sets the target current limit is calculated. (R11 in Figure 1). The IS pin series current limiting resistor is to limit the negative current whenever the primary current swings negative, to acceptable values. The IS pin characteristic resembles a reverse diode to ground when a negative voltage is present. 220 Ω is the minimum acceptable value, and yields the largest acceptable noise filter capacitor which maximizes noise rejection. The IS pin noise filter capacitor has a suggested value of 1.0 nF. Ensure that the resulting pole frequency is high enough that the current sense signal is not attenuated.

"SL" type capacitors which are commonly used in lighting ballast applications, are suitable for the sense capacitance due to their combination of capacitance value range, small size, high current handling capability, low cost, and availability.

Step 14: Loss Budget

LOSS BUDGET				
LCS device Conduction loss		1.8	W	Conduction loss at nominal line and full load
Output diode Loss		4.2	W	Estimated diode losses
Transformer estimated total copper loss		0.52	W	Total copper loss in transformer (primary + secondary)
Transformer estimated total core loss		0.6	W	Estimated core loss
Total transformer losses		1.1	W	Total transformer losses
Total estimated losses		7.1	W	Total losses in LLC stage
Estimated Efficiency		95%	%	Estimated efficiency
PIN		151	W	LLC input power

Figure 21. Loss Budget Section from HiperLCS Spreadsheet.

LCS device conduction loss is calculated from the nominal current and maximum $R_{DS-ON.}$ Diode losses are calculated from the load current and specified diode voltage drops. Transformer estimated copper, core, and total losses are calculated. Total estimated losses, efficiency, and input power are calculated.

Step 15: Examine the Input Voltage vs. Frequency Curves

The designer can examine the input voltage versus frequency curves by clicking the graph tab at the bottom of the spreadsheet. Two traces are presented. The red trace is generated by the main resonant section, and the blue trace is generated by the virtual trial transformer section. $V_{BROWNOUT}$ is also shown on the graph.

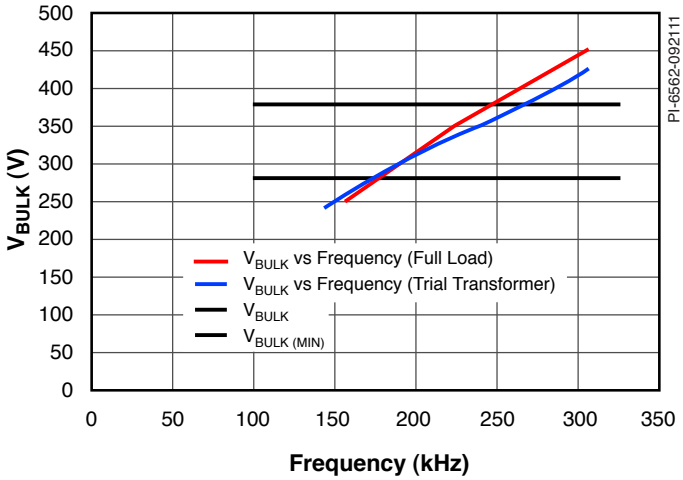

Figure 22. Example of Input Voltage vs Frequency Graph from HiperLCS Spreadsheet. Blue Trace is from Virtual Trial Transformer Section.

Step 16: Optional Section: Secondary Turns Calculator

SECONDARY TURNS AND VOLTAGE CENTERING CALCULATOR				This is to help you choose the secondary turns - Outputs not connected to any other part of spreadsheet
V1		24.00	V	Target regulated output voltage Vo1. Change to see effect on slave output
V1d1		0.70	V	Diode drop voltage for Vo1
N1		6.00		Total number of turns for Vo1
V1_Actaul		24.00	V	Expected output
V2		0.00	V	Target output voltage Vo2
V2d2		0.70	V	Diode drop voltage for Vo2
N2		0.00		Total number of turns for Vo2
V2_Actual		-0.70	V	Expected output voltage

Figure 23. Secondary Turns and Voltage Centering Calculator from HiperLCS Spreadsheet.

This section is not connected to any other part of the spread-sheet. It is used to assist the designer in choosing turns ratios for a two output design. Note that for some voltage ratios, such as 5 V and 12 V, a large number of turns are necessary to achieve the desired voltage centering. This usually does not result in an acceptable transformer design. One possible solution for a 5 V and 12 V requirements is to design an LLC to have 6 V and 12 V outputs, and use a buck converter on 6 V to produce 5 V. Because of the small voltage drop necessary, such a buck converter will be relatively low cost and have high efficiency.

Step 17: Optional Section: Separate Resonant Inductor

Separate Series Inductor (For non-integrated transformer only)				Not applicable if using integrated magnetics - not connected to any other part of spreadsheet
Lsep		72.83	uH	Desired inductance of separate inductor
Ae_Ind		0.53	cm^2	Inductor core cross-sectional area
Inductor turns		13		Number of primary turns
BP_fnom		1554	Gauss	AC flux for core loss calculations (at f_predicted and full load)
Expected peak primary current		2.7	A	Expected peak primary current
BP_fmin		2900	Gauss	Peak flux density, calculated at minimum frequency fmin
Inductor gauge		44	AWG	Individual wire strand gauge used for primary winding
Equivalent Inductor Metric Wire gauge		0.050	mm	Equivalent diameter of wire in metric units
Inductor litz strands		125.00		Number of strands used in Litz wire
Inductor parallel wires		1		Number of parallel individual wires to make up Litz wire
Resistivity_25 C_Sep_Ind		75.4	m-ohm/m	Resistivity in milli-ohms per meter
Inductor MLT		7.00	cm	Mean length per turn
Inductor DCR 25 C		68.6	m-ohm	Estimated resistance at 25 C (for reference)
Inductor DCR 100 C		92.0	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
ACR_Sep_Inductor		147.1	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Inductor copper loss		0.14	W	Total primary winding copper loss at 85 C

Figure 24. Separate Series Inductor Section from HiperLCS Spreadsheet.

This section is not connected to any other part of the spread-sheet. It is used for designing a separate resonant inductor for when a non-integrated transformer is used, or when the desired transformer construction results in excessively low leakage inductance, yielding a K_{RATIO} greater than 7.

How to Use the Spreadsheet Resonant Section when Using a Separate Resonant Inductor

The Resonant Parameters section of the spreadsheet was designed for integrated transformers. However, it can be used for designs with a separate series inductor.

There are two types of designs using a separate resonant inductor:
1. Transformer having near zero leakage inductance, with resonant inductance formed solely by the series inductor.
2. Transformer has some leakage inductance. The resonant inductance is formed by the sum of the series inductor and the transformer primary leakage inductance. The series inductor augments the transformer leakage inductance.

Near-Zero Leakage Inductance Transformer Resonant Tank Design

Referring back to the spreadsheet's one-leakage inductor equivalent circuit in Figure 8, it is obvious that:

1. Resonant inductance (L_{RES}) in the spreadsheet is equal to the value of the separate inductor
2. Parallel inductance (L_{PAR}) in the spreadsheet is equal to the transformer primary inductance; L_{PRI} in the spreadsheet is equal to the sum of the separate inductor and the primary inductance of the transformer. The spreadsheet recommended value of L_{PRI} is still valid.
3. The equivalent turns ratio (n_{EQ}) in the spreadsheet is equal to the transformer's actual turns ratio.

Non-Zero Leakage Inductance Transformer Plus External Series Inductor Resonant Tank Design

In this design the total series resonant inductance is split between an external inductor, and the leakage inductance of the transformer.

Sometimes a designer attempts to build and integrated transformer and ends up with insufficient leakage inductance (K_{RATIO} > 7). If the transformer geometry is not suitable for increasing the leakage inductance, one solution is to add an external inductance.

Referring back to the spreadsheet's one-leakage inductor equivalent circuit in Figure 8, it is obvious that:

4. Resonant inductance (L_{RES}) in the spreadsheet is equal to the sum of the values of the separate inductor and the transformer leakage inductance.
5. Primary inductance (L_{PRI}) in the spreadsheet is equal to the sum of the separate inductor and the primary inductance of the transformer. The spreadsheet recommended value of L_{PRI} is still valid.
6. The equivalent turns ratio (n_{EQ}) in the spreadsheet is less than the transformer's actual physical turns ratio.

Designing with a variable input voltage

For a design with a variable input voltage (such as a 180-265 VAC design with no PFC), set V_{BULK_NOM} to a value halfway between the minimum and maximum AC voltage, in order to design the resonant power train values. First determine the maximum and minimum bulk voltages:

$$V_{HIGH\_LINE} = VAC_{MAX} \times 1.414$$

$$V_{LOW\_LINE} = VAC_{MIN} \times 1.414$$

Then, in order to determine a starting value for N_{PRI}, enter the average of the above 2 values into V_{BULK_NOM}. Adjust N_{PRI} to the next higher integer value so that $f_{PREDICTED}$ is equal to or slightly lower than f_{RES} at this bulk voltage. This will make the LLC operate at resonance halfway between low and high-line. Reducing the primary turns (resonance occurs at a lower voltage), will:

- Reduce peak and RMS currents at low-line
- Increase the required primary inductance to maintain ZVS at low-line
  - This reduces the circulating primary resonant current
- Operate the output diodes more heavily in continuous conduction mode
  - This increases their peak inverse voltage stress
- Increase the operating frequency at high-line.

If VAC_{MIN} is < 70% of VAC_{MAX}, it is recommended that $V_{BROWNOUT}$ is set close to V_{LOW_LINE}:

$$V_{BROWNOUT} = 90\% \times 1.414 \times V_{LOW\_LINE}$$

This choice may generate warning messages but they can be ignored. This means that the B+ UVLO function may have to be disabled or modified with some extra components added to the OV/UV pin resistor divider.

Fix the value of L_{PRI} by copying the recommended value into the input column. In order to examine low-line and high-line operation, enter them one at a time into V_{BULK_NOM}.

Designing with a Variable Output Voltage or with a Constant-Current Output

Battery charger applications require a constant-voltage, constant-current (CV-CC) output. The application should specify the minimum expected output voltage during CC operation. Any number of circuits can be used to implement the constant-current feedback. Please refer to the Power Integrations website for suggested circuits.

Any CC circuitry powered from the main output will need to operate correctly at the minimum output voltage. If the minimum output voltage is very low, an auxiliary supply may be needed to power the CC circuitry.

The power train will have maximum output power at the corner of the CV and CC characteristic curve, and this is the condition that needs to be entered into the spreadsheet in order to design the power train resonant components. In CC mode, as the output voltage goes down, the LLC will run at higher and higher switching frequency. Operation at reduced output voltage can be examined by fixing the power train component values in the spreadsheet, then reducing VO_1.

If the maximum to minimum voltage ratio is < 1.3×, it is recommended that the maximum power point (rated output voltage and current), operate at or slightly below resonance. If the ratio is greater than 1.3, it is recommended to run the maximum power point above resonance (by increasing N_{PRI}), in order to compress the frequency increase required by operation at minimum output voltage. In some cases it may be necessary to set N_{PRI} so that the power train operates at resonance ($f_{PREDICTED} = f_{RES}$) at a point halfway between minimum and maximum output voltage. In extreme cases the LCS will have to enter burst mode at very low output voltages. This may be an acceptable compromise.

LLC Waveform Analysis

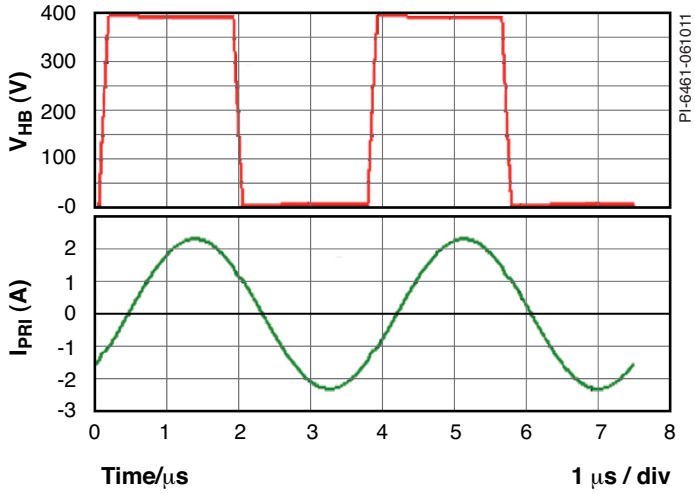

Figure 25. V_{HB} and I_{PRI} Operating at Resonance, Heavy Load.

Note the near-perfect sinusoid of the primary current. The frequency is the primary resonant frequency f_{RES}, and the input voltage at this condition is $V_{INPUT(RESONANCE)}$.

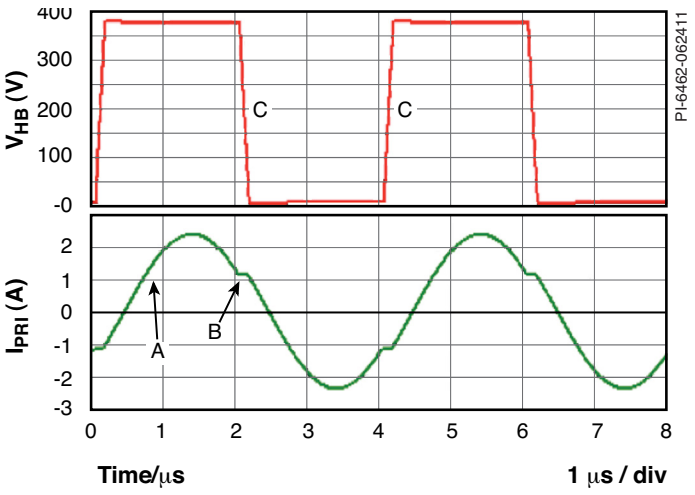

Figure 26. V_{HB} and I_{PRI} Operating Slightly Below Resonance, Heavy Load.

Note that the series resonant current 'A' has "extra time" to finish its "resonant ring" and meet the primary magnetizing current 'B'. ZVS operation is normal. Note the slope in the voltage C.
Note that the series resonant current 'A' has not had enough time to finish its resonant ring before the MOSFETs switch and is truncated, with a near-vertical portion (arrows). ZVS operation is normal. Note the slope in the voltage.

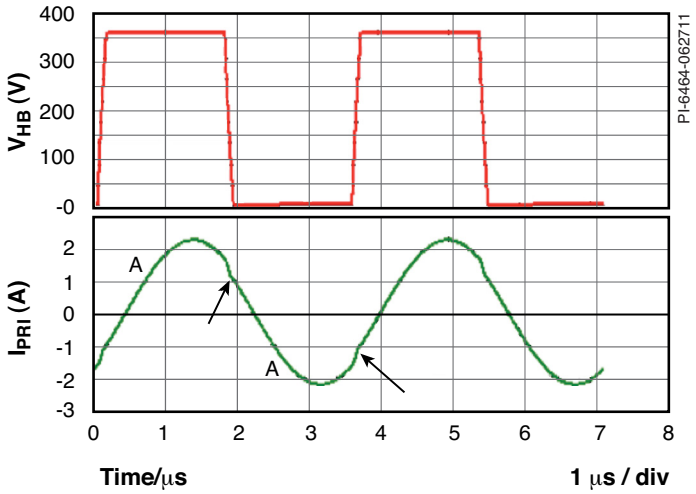

Figure 27. V_{HB} and I_{PRI} Operating Slightly Above Resonance, Heavy Load.

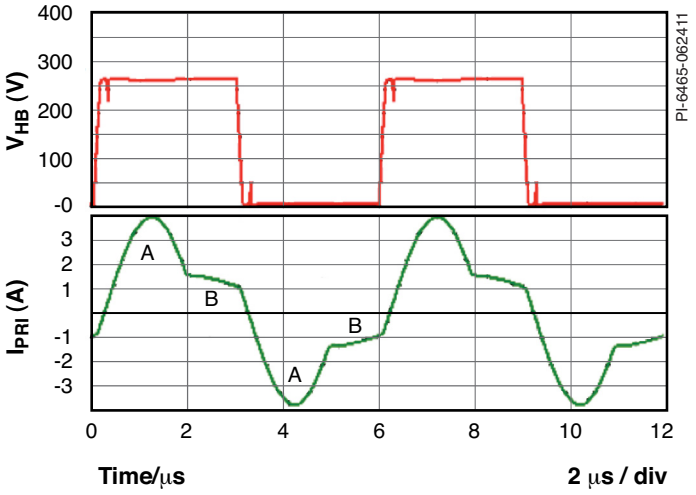

Figure 28. V_{HB} and I_{PRI} Waveforms, Operating at Low Frequency, far Below Resonance (Near Minimum Input Voltage, Heavy Load).

The resonant ring 'A' ends early and the magnetizing ring 'B' is long. Note in this example, dead-time is slightly longer than optimal for this condition.

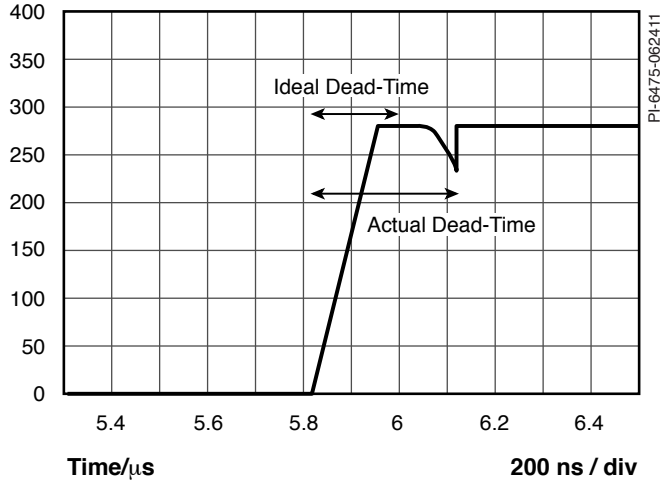

Figure 29. VHB at Low-Line / Full Load, Zoomed into the Switching Edge, Exhibiting a Dead-Time Slightly Longer than Optimal for this Condition.

Dead-time is a compromise; light load/high-line operation requires long dead-times. Low-Line/full load requires shorter dead-times. Figure 29 shows low-line operation with a compromise dead time value. Such a condition is acceptable for non-steady-state conditions. The waveform shows there is sufficient energy in the magnetizing inductance to achieve ZVS, because the sinusoidal ring reaches the opposite rail. In the flat-top part of the sine portion, the voltage is clamped by the upper MOSFET's body diode conduction. The end of the actual dead-time is where the MOSFET gate is turned on. Dead-time is most easily measured at low-line, full-load with the waveform as above. Compare rising and falling edge dead-times; asymmetry in the dead-times can be caused by switching noise entering the DT/BF pin and must be fixed by improving the layout or increasing the DT/BF bypass capacitor (observe the maximum allowable value recommendation).

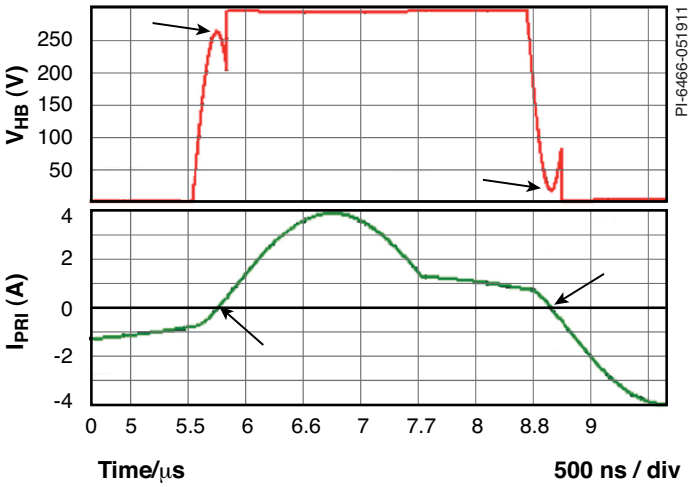

Figure 30. V_{HB} at Low-Line / Full Load, Exhibiting Insufficient Magnetizing Energy and a Dead-Time Longer than Optimal.

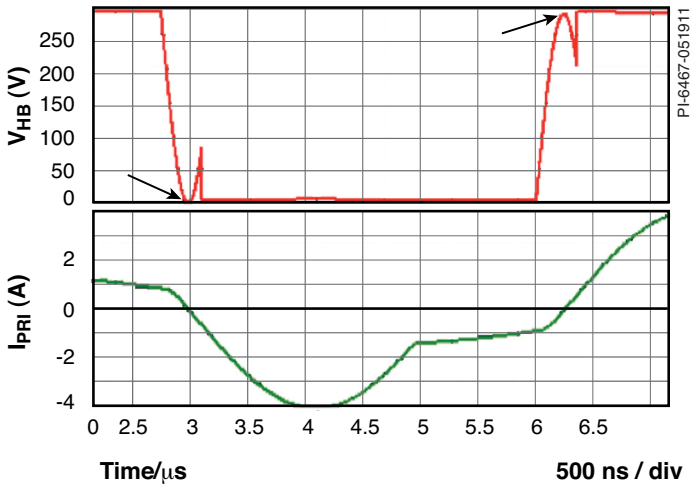

Figure 31. Voltage Waveform Showing Magnetizing Energy is on the Borderline of Being Sufficient for Complete ZVS. See Arrows. The Dead time is Longer than Ideal for this Condition.

Arrows point to top of "sinusoidal ring" which does not reach the opposite rail. The top of the ring coincides with zero crossing of the current (arrows). Such a condition is acceptable for non-steady-state conditions. If full ZVS is desired, primary inductance needs to be reduced.

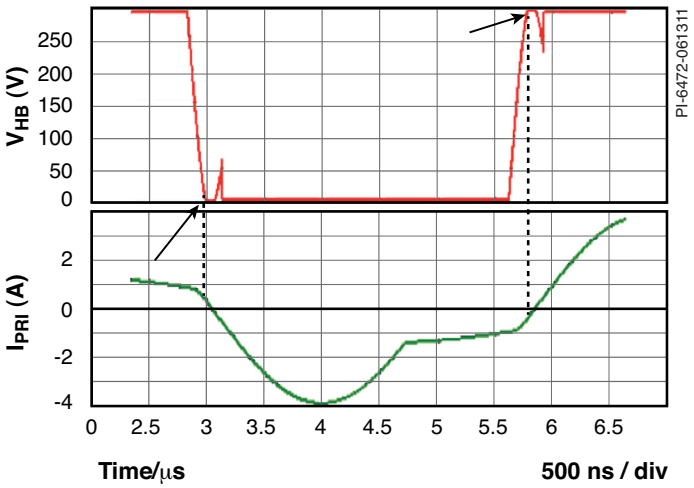

Figure 32. When There is Sufficient Magnetizing Energy for ZVS, the Voltage (arrows) Finishes Slewing Before the Current Crosses Zero (dashed line).

The dead-time is longer than ideal for this condition.

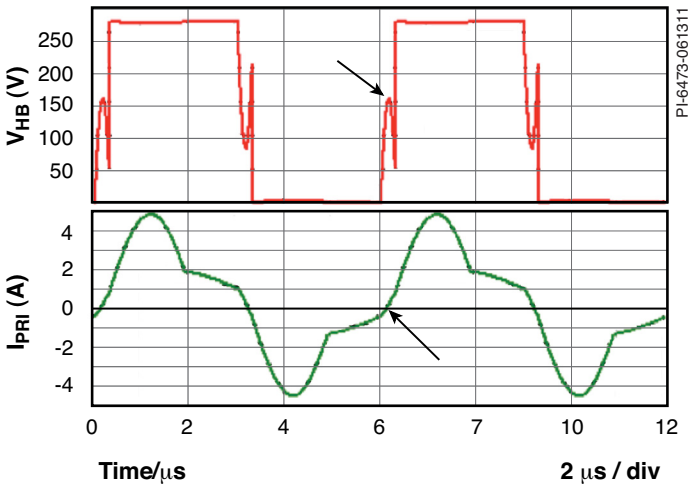

Figure 33 Waveforms Showing Severe Loss of ZVS at Low Frequency (Low-Line), Due to Overload or L_{PRI} too High.

Note how the current crosses zero before the ZVS is completed (arrow).

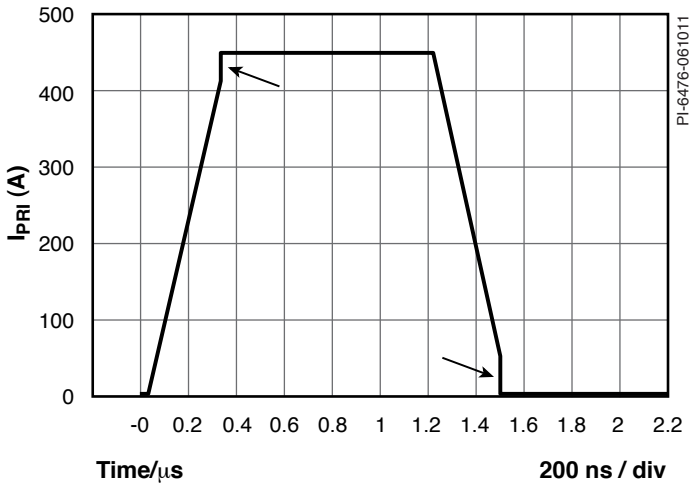

Figure 34. Light Load, High-Line Operation, Showing Long Slew-Times, and Dead-Time Slightly Shorter than Optimal. Arrows Point to Truncated Slew.

As load is decreased at high-line or voltage is increased at light load, the frequency increases and the magnetizing current decreases. This increases the ZVS slew time. When the slew time begins to be greater than the dead-time, the ZVS slew is truncated, as shown. Any further increase in frequency will cause the gain to invert, and the PSU will snap into burst mode. If burst mode occurs too early, some solutions are: increasing primary turns, decreasing primary inductance. It is appropriate to program f_{START} and f_{STOP} (burst frequency thresholds) close to this gain inversion frequency. This is high frequency gain inversion (not to be confused with low frequency gain inversion, at low-line). Setting them much higher can increase output ripple in burst mode and worsen step load response wherein the HiperLCS goes in and out of burst mode, as the feedback loop is forced to swing through a wider control range.

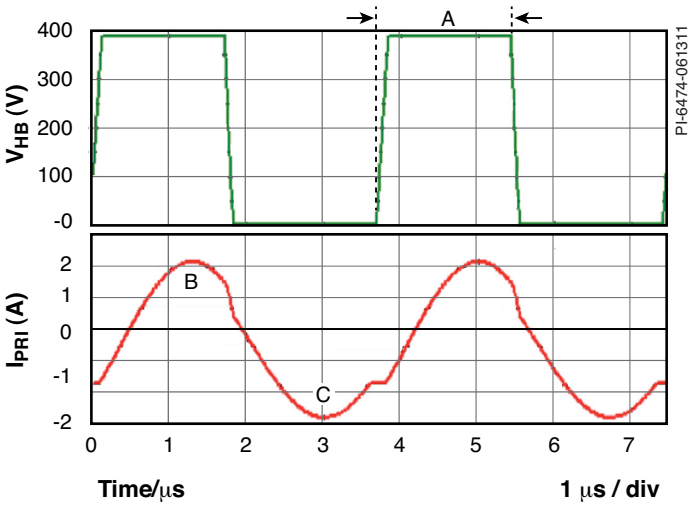

Figure 35. Duty Cycle Asymmetry. Duty Cycle Equals 'A' Divided by Period.

This example waveform has 47% duty cycle instead of 50%. This commonly is caused by switching noise entering the FEEDBACK pin. The current waveform shows a different magnitude for the positive peak and the negative peak. This LLC is operating at resonance, but the positive half 'B' resembles operation above resonance, and the negative half 'C' resembles operation below resonance.

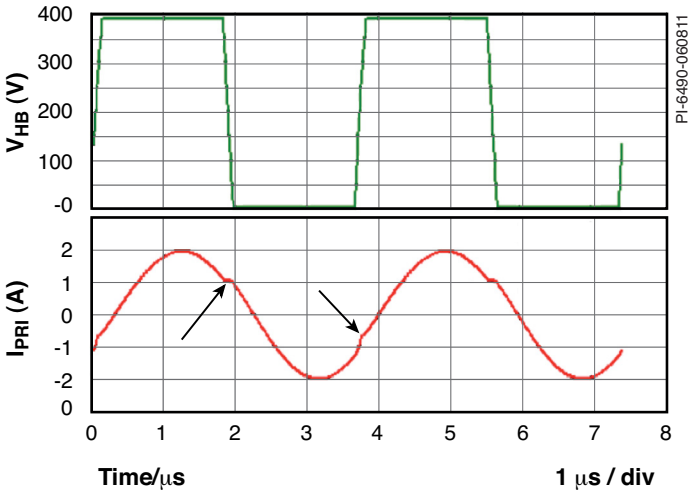

Figure 36. Current Waveform Asymmetry Due to Asymmetry in the Secondaries. Voltage Waveform has 50% Duty Cycle.

This could be caused either by poor, asymmetric secondary layout, or by not twisting the transformer secondary halves together. These measures are critical for high frequency LLC design. In this case the voltage is symmetric, but the positive and negative current pulses appear to have different resonant frequencies, as shown by the arrows. In this case, the leakage inductance measured from the primary, are different when comparing one phase of the secondary shorted, vs. the other phase shorted.

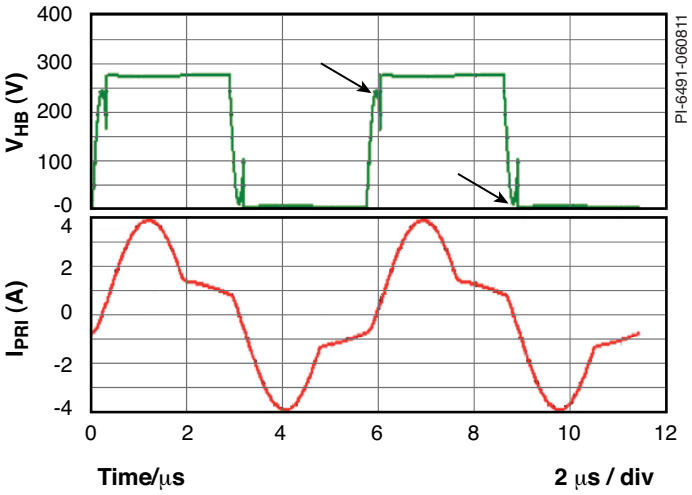

Figure 37. Some Asymmetry Will be Evident at Low-Line even with Careful Layout.

Note how one edge (in this case the rising edge), loses ZVS sooner than the failing edge.

Powering Up HiperLCS and troubleshooting

Do not attempt to power-up the HiperLCS with a high-voltage on the DRAIN pin and the transformer disconnected from the HB pin. The lack of an inductive load will cause hard-switching, and the resulting MOSFET C_{OSS} switching losses will cause overheating.

1. Disable the OV/UV function so that the switching waveforms can be examined even with a very low B+ voltage. Disconnect the resistor that goes from the OV/UV pin to B+. Place a resistor from the OV/UV pin to the VCC pin, so that the resulting temporary voltage divider will apply 2.4 V (the brown-in threshold) on the OV/UV pin when VCC is at ~11 V. If the lower divider resistor is 20 kΩ, use a 75 kΩ resistor.
2. Apply a current-limited 12 V supply to VCC +12 V. Current draw should be <10 mA.
3. Use a current limited high-voltage adjustable supply for B+. Apply a small voltage initially (around 10 V - 20 V), with a current limit of ~0.2 A. Examine the HB pin for switching at f_{MIN}. If the frequency is not close to f_{MIN}, examine the resistor values on the FEEDBACK pin.

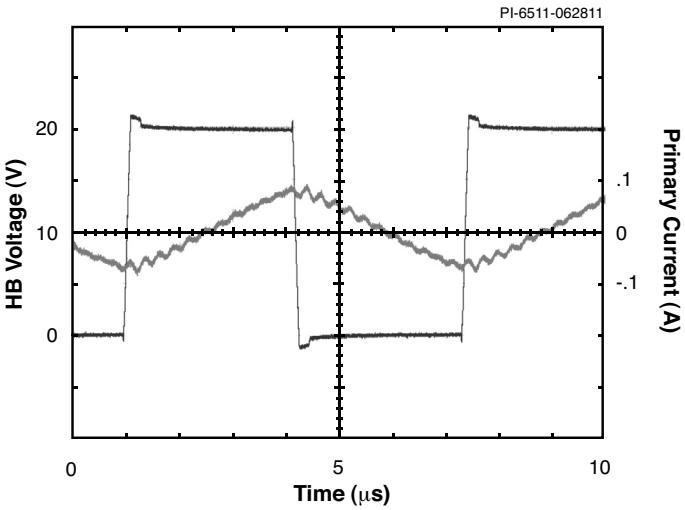

Figure 38. Half-Bridge Voltage and Current with B+ = 20 V.

4. Place a current probe on the primary current. With zero load on the secondary, you should see a triangular wave, which is the magnetizing current. The PSU output should show a very low voltage. The HB pin should exhibit ZVS. Switching frequency should be between f_{MIN} and f_{STOP}. If it is >f_{STOP} then the part has not exited start-up mode (see data sheet). Start-up mode is exited at power-up once f_{SW} drops below f_{STOP}. The soft-start capacitor must be small enough so that start-up mode is exited before the output reaches regulation when HiperLCS is powered up with minimum load.

If there is no switching, probe the voltages on each pin:

- VCC: >11.4 V
- VREF: 3.4 V – if this is not 3.4 V, HiperLCS is off because VCC is below the UVLO threshold
- OV/UV: 2.4 V – 3.1 V
- IS: < 0.5 V peak
- FEEDBACK: 0.9 V – 1.4 V depending on feedback current. If it is 3.4 V, the HiperLCS is in the off state of auto-restart, or is inhibited by the OV/UV or IS pins
- VCCH: should be HB pin + 12 V if measured against Ground. Should be >8.9 V when measured with a differential probe referenced to the HB pin.
- HB pin: switching square wave from B- to B+ with evidence of ZVS: primary current must be negative at the end of the low to high transition of VHB, and positive at the end of the high to low transition. Ensure that the current probe is not connected backwards.

5. Slowly increase the input voltage. The triangular primary current should get larger. The HB pin should continue to show ZVS. The output should rise. With zero load, the input power should not be more than 1-2% of the rated output power. At about 45-70% of nominal input voltage (depending on the resonant tank), the output should reach regulation. Once in regulation, a further increase in input voltage should not show an increase in output voltage. Instead, the frequency should rise to maintain regulation. At this point, increasing the input voltage further should not cause an increase in the primary current triangle waveform because of the increasing frequency.
6. Place a small load on the output. The switching frequency should drop as the output is loaded. The primary current should begin to show the classic LLC waveforms. At low input voltage, the switching frequency should be below resonance. (See Figure 28 in LLC Waveforms Analysis section in this document.) Ensure that the high-voltage bench supply used to power the LLC is not current-limiting.
7. Increase the input voltage to the rated minimum input voltage ($V_{BROWNOUT}$). Increase the load to about 5-10% of rated. Increase the input voltage to the nominal value. (Do not operate the PSU with any significant load below the rated $V_{BROWNOUT}$ because the resulting loss of ZVS can cause very high losses.) Regulation should be maintained. If the output begins to rise, probe the optocoupler's emitter. If it is close to 3.2 V, examine the FEEDBACK pin resistors. If it is <3.2 V and the output rises above regulation, check the optocoupler LED circuit and make sure there is enough current for the LED to drive the photo-transistor into saturation.
8. Check the primary waveforms for symmetry and ZVS. It should show operation close to resonance at some input voltage close to nominal. If not, the turns ratio could be wrong. (See Figure 25 in LLC Waveforms Analysis section in this document.)
9. With ~10% load the HiperLCS should not enter burst mode at nominal input voltage. Slowly reduce the load and observe the frequency. In some cases input voltage may need to be increased above nominal, even at zero load, to force the HiperLCS into burst mode. As input voltage is raised and the frequency rises and reaches f_{STOP}, the HiperLCS will suddenly go into burst mode. Examine the burst mode waveforms.

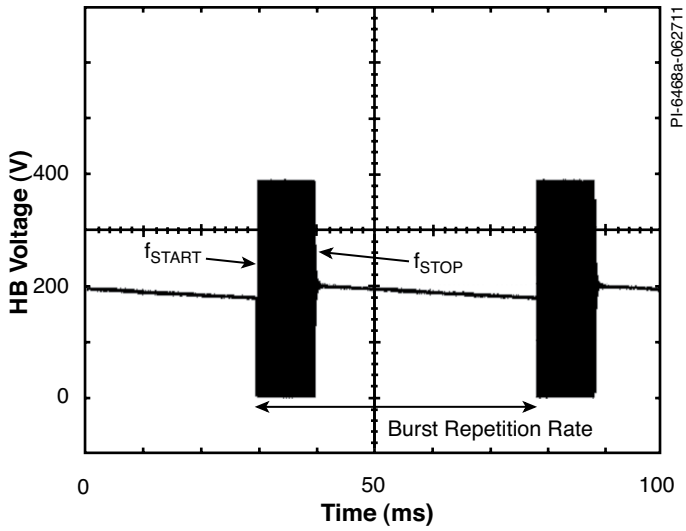

Figure 39. HiperLCS in Burst Mode.

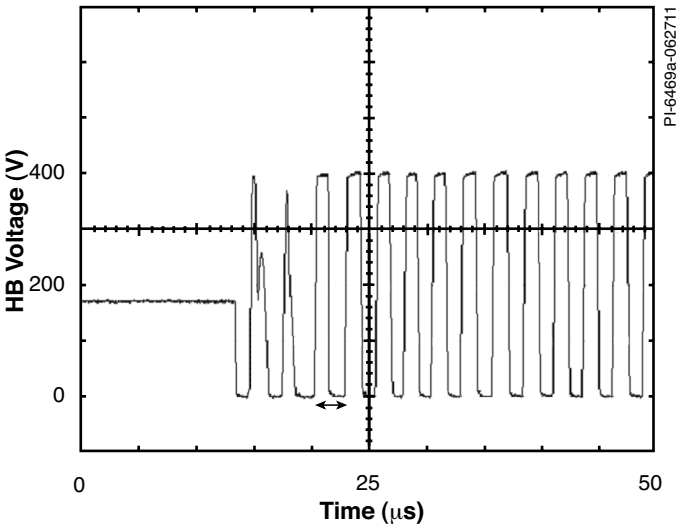

Figure 40. Expanded View of Figure 39 at the Beginning of the Burst Showing F_{START}.

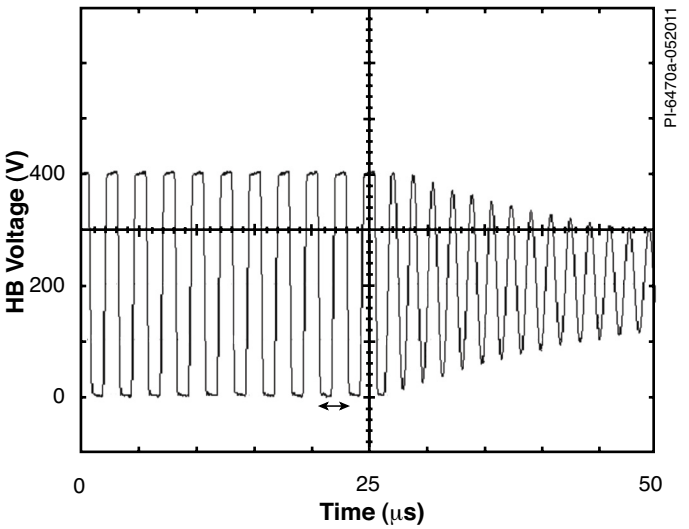

Figure 41. Expanded View of Figure 39 at the End of the Burst Showing F_{STOP}.

10. Re-enable the OV/UV resistor divider and check that the HiperLCS turns on at $V_{BROWNIN}$ and turns off at $V_{BROWNOUT}$.
11. Measure the efficiency of the PSU at 20% load and nominal input voltage. It should be within a few % of targeted full load efficiency. Use a thermal camera to look for parts that are unusually hot.
12. Increase the load to 50% at rated input voltage and repeat efficiency and thermal tests, and again at 100% load.
13. Check the duty cycle and current symmetry at full load, nominal input voltage. See Figure 26 in the LLC Waveform Analysis section of this document for switching with good duty cycle symmetry and Figure 35 for an example of poor duty balance.
14. Use a close-coupled probe and check the p-p ripple voltage on the main output capacitors and verify it is <3% of the output voltage. Greater than 3% can be acceptable if the efficiency, diode PIV stress, capacitor temperature rise and cross-regulation are acceptable .

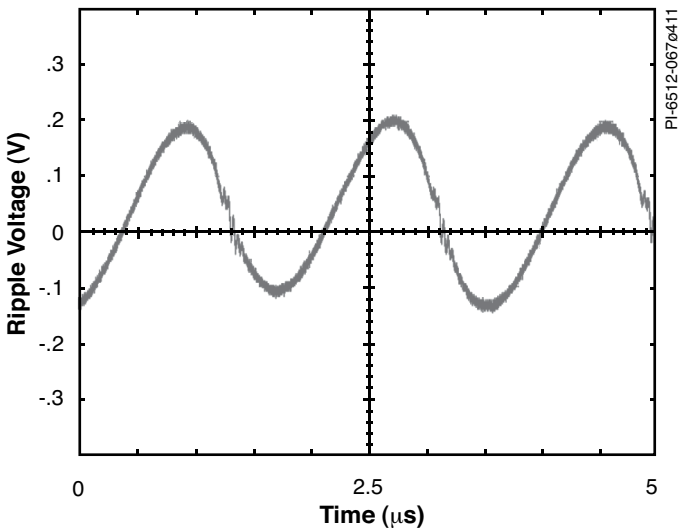

Figure 42. Output Ripple Voltage at Full Load across Ceramic Output Capacitors.

15. Examine HB voltage for proper ZVS operation at full load, as input voltage is reduced down to $V_{BROWNOUT}$. When there is partial loss of ZVS, check to determine if the dead-time is too short or too long, or if the primary inductance is too high (insufficient energy to charge C_{OSS}), or if it can be increased. (See Figures 29-33) Partial loss of ZVS as $V_{BROWNOUT}$ is acceptable. However the losses will be high and caution is necessary. Use a fan to keep the HiperLCS heat sink cool. Note that poor current symmetry, or poor duty cycle symmetry, will cause early loss of ZVS on one edge of the primary voltage.
16. Measure the peak current at low-line / full load, and adjust the current limit resistor (R11 in Figure 1) so that the calculated current limit is ~20% greater.
17. Check the dead-time symmetry during partial loss of ZVS. Compare dead-time of the low and high switching edge vs. the high and low edge. See Figure 37 in LLC Waveforms Analysis section in this document.
18. Check the primary waveforms at short-circuit and ensure that the HiperLCS shuts down properly, and that the Drain current does not exceed the ABS MAX rating for > 460 ns (See Figures 58 and 59).

19. Ceramic SMD bypass capacitors can be delicate and easily damaged during hand soldering. Mis-operation can be caused by faulty capacitors. A bad FEEDBACK pin bypass capacitor will cause noise to enter and produce poor duty cycle symmetry. A bad DT/BF pin bypass capacitor will cause poor dead-time matching (comparing low to high and high to low switching edges).

High Frequency Integrated Transformer Design

High frequency integrated transformer design (180-300 kHz) is not very different than designing for 60-70 kHz. The following are the main differences:

- The core will be smaller.
- The turns will be fewer so less total copper will be used.
- PC44 or equivalent core material is recommended, rather than PC40. PC44 allows 10-20% higher flux density at 250 kHz than PC40 for the same losses. PC40 or equivalent can be used, but PC44 will improve core losses, and in some cases can allow the use of fewer turns or a smaller core. For even higher efficiency, higher performance core material can be used.
- AC flux density will need to be approximately 30% lower at 250 kHz than at 125 kHz. The higher frequency still results in fewer turns and a smaller transformer.
- Symmetry in the half-secondaries is critical – intertwining them before winding, is highly recommended. Poor winding symmetry results in different leakage inductances between each half-secondary to the primary, resulting in poor current symmetry between ½ cycles, increased losses, higher temperatures, and reduced efficiency. (See Figure 36 in LLC Waveforms Analysis section in this document.) Intertwining the secondaries greatly reduces the leakage inductance between secondary halves, which greatly reduces the leakage inductance spike seen by the output rectifiers, and also improves the transformer symmetry. Symmetry can be tested by measuring the leakage inductance on the primary with one phase of the secondary shorted at a time. If symmetry is good, the leakage inductances will be closely matched.
- Finer Litz is recommended - #44 (~0.05 mm) in the primary and #42 (~0.07 mm) in the secondary. However, because the turns are fewer and the core is smaller, than a low frequency design, the total cost is lower.
- In some cases high frequency requires relatively low leakage inductance which cannot be achieved with a 2-section bobbin. One solution is to use a 3-section bobbin. See Figures 12 and 46 for a photo comparing a 2-section bobbin with a 3-section bobbin, with the secondary in the middle section, and the 2 series-connected primary halves in the outer two sections. Another solution is to use a core with a larger cross-sectional area. This allows fewer turns, reducing leakage inductance.
- Flat and long cores/bobbins tend to have higher leakage inductance than shorter, more square-shaped cores.

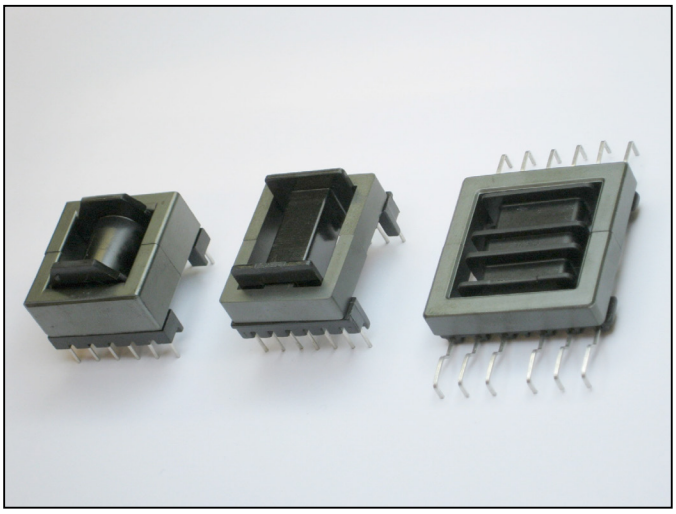

Figure 43. Comparing, from Left to Right, the EER28, EEL25 Core Which is Long and Thin, and the EFD35 Flat Core. The Long and Thin, and Flat Cores, will have Greater Leakage Inductance than the EER28, for the Same Number of Winding Sections. All are Good for ~150 W at 250 kHz.

The following guidelines should be followed in the transformer design:

- Secondary winding halves should be intertwined before being wound on the core. (See Figure 44)

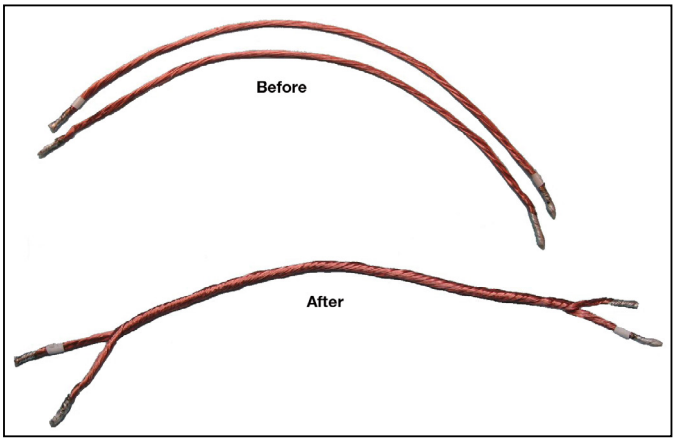

Figure 44. Intertwining Litz Bundles for the Secondary Halves. This Technique is Extremely Effective for Improving Transformer Symmetry (Inductance from each Half to the Primary), and for Reducing Output Rectifier Voltage Spikes Due to Leakage Inductance Between Halves.

- If there are 2 outputs, each output's half-secondary pairs should be intertwined with each other (see Figure 45).

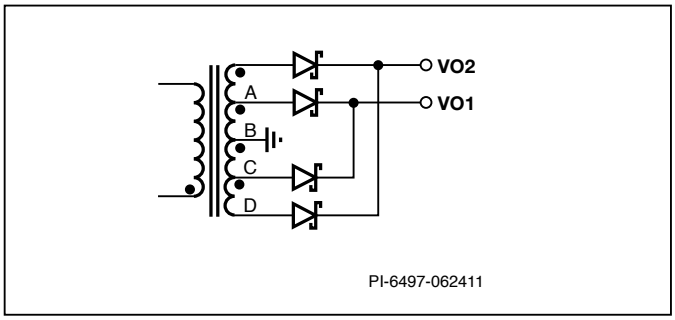

Figure 45. Windings 'B' and 'C' are Intertwined Together. Windings 'A' and 'D' are Intertwined Together. The Resulting Bundles A+D and B+C do not Need to be Intertwined. However, Winding them Bi-Filar Style (Winding Them at the Same Time) can Improve Cross-Regulation.

- Use Litz with strand insulation that solder-strips (so that tinning strips the insulation).
- Litz wire requires proper tinning of the ends. If the solder doesn't penetrate all the way through the Litz bundle, some of the strands will not conduct any current and losses will greatly increase. As a test for proper solder penetration, measure the DC resistance at the pins and use it in the production specification. For high current secondaries, use a proper 4-wire Kelvin measurement.
- For high current secondaries (e.g. 20 A), do not terminate the Litz wire on transformer pins. It is far better to have the Litz come down into large holes in the PCB to be soldered directly.

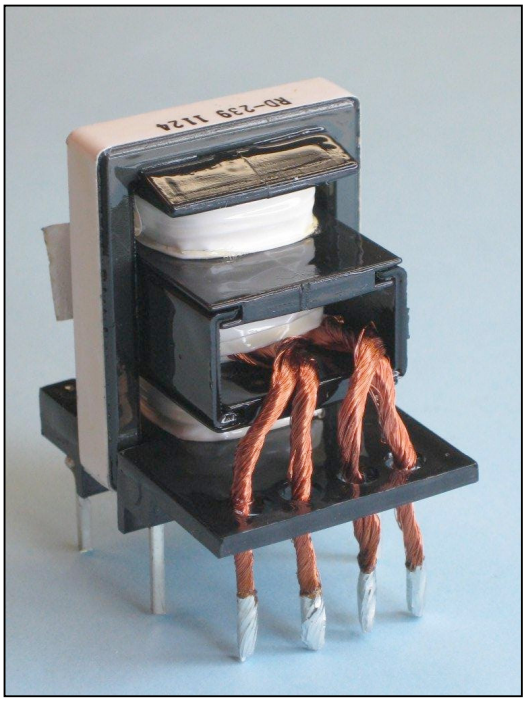

Figure 46. Transformer with Litz Secondaries Tinned and Ready for Insertion into Holes in the PCB. Do not Terminate High Current Litz Secondaries on Transformer Pins.

- DO NOT parallel Litz bundles (in the way that non-Litz transformers can use multiple parallel strands of wire). Instead, use Litz with more strands as needed. Paralleling wires or Litz bundles in a transformer with a high leakage inductance will cause high losses because the strong leakage flux produces a slight voltage difference (due to slightly different effective turns because the 2 bundles don't occupy the same space). This causes large circulating currents between the paralleled wires, as the wire with the higher effective turns forces current into the other wire.
- Served (wrapped) Litz is preferred in the primary due to large layer-to-layer voltage differentials. Un-served Litz is preferred in the secondary, for better packing density.

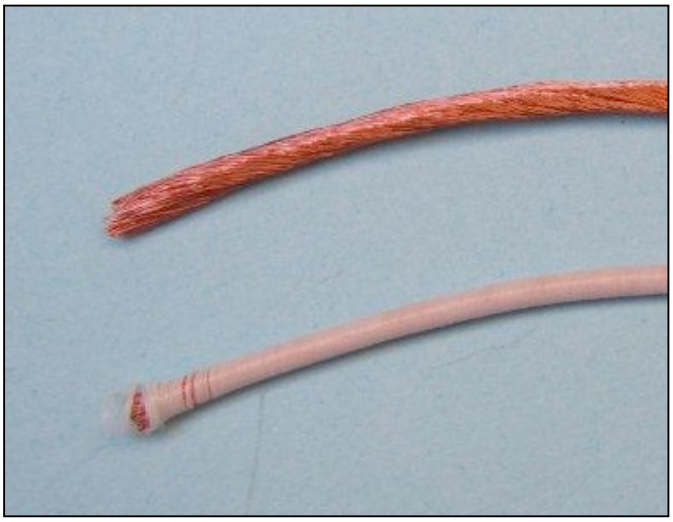

Figure 47. Un-Served (Upper Image) and Served (Lower Image) Litz Wire.

Effect of Resonant Tank Tolerances

The leakage inductance of an integrated transformer will show tight tolerance over production if the mechanical construction is well controlled, typically ±5%. Because of this tight tolerance the primary leakage inductance measurement is a good indicator that the transformer was wound with the correct number of primary turns. The magnetizing inductance is dependent on the size of the core gap and has a typical, looser tolerance of ±7%. The tolerance of the gap has very little effect on the leakage inductance.

The tolerance of the leakage inductance and of the resonant capacitor will affect the resonant frequency. Because resonant frequency

$$f_{RES} = \frac{1}{2 \times \pi \times \sqrt{L \times C}}$$

is inversely proportional to the square root of inductance and capacitance, a change in inductance or capacitance produces only half the change in resonant frequency. i.e. a 5% change in capacitance or inductance produces a 2.5% change in resonant frequency.

The greatest influence on f_{RATIO} at nominal input voltage, where f_{RATIO} is defined as

$$f_{RATIO} = \frac{f_{SW}}{f_{RES}}$$

is the transformer turns ratio. Resonant inductance and capacitance tolerance will affect f_{RES} but not f_{RATIO}. For example, if a design operates nominally slightly below resonance (diodes switch slightly discontinuously), then the design will continue to do so despite the tolerances of the leakage inductance and capacitance. The operating frequency, however, will change.

The tolerance of the magnetizing (transformer primary open-circuit circuit) inductance has a significant effect on the loss of ZVS point at low-line. For this reason it is recommended that when adjusting the primary inductance with respect to loss of ZVS, the maximum permissible inductance value be determined. This value should be used as the maximum value in the transformer specification.

Tuning Burst Mode

In burst mode, the HiperLCS simply stops switching when the switching frequency rises and f_{STOP} is reached. The output voltage begins to droop, and switching starts again when the frequency commanded by the feedback loop drops down to f_{START}. Because the switching frequency of an LLC is a function of both input voltage and load, it is not possible to design burst mode such that burst mode will occur at a fixed load threshold independent of input voltage. If burst mode must always occur below a given load, e.g. 5%, testing must be performed across the entire range of input voltage set-point tolerance. The tolerance of the resonant inductance and capacitance must also be considered.

The main consideration in tuning burst mode is setting f_{START}. Please see the data sheet. Figure 19 and Table 5 of the data sheet show that f_{START} is a continuous, inverse function of the dead-time setting and a discrete function of the burst setting number. Because the dead-time for the majority of designs varies between 290 ns and 360 ns, available f_{START} varies more with burst setting number than with dead-time. Therefore the BT# selection is the "coarse" setting, and dead-time can be used as the "fine" adjustment, if necessary. BT3 is suitable for designs with f_{NOM} < ~180 kHz, BT2 for 180~280 kHz designs, and BT1 for >230 kHz designs. For approximately 230~280 kHz, BT1 and BT2 can be suitable.

Setting $f_{NOM} < f_{RES}$ tends to yield the best efficiency, EMI, and PIV stress on the output diodes. However, such designs may not enter burst mode at nominal input voltage, even with zero load. This is because the switching frequency does not need to increase very much to maintain regulation. At higher input voltage, it may then enter burst mode. With a design with $f_{NOM} > f_{RES}$, switching frequency will rise faster as load is reduced.

A higher K_{RATIO} (smaller resonant inductance) will also require a larger frequency change with a change in line voltage and load.

A large parasitic rectifier capacitance, coupled with a dead-time that is shorter than optimal at light load, (see Figure 34), will also cause burst mode to engage sooner.

The PSU will exhibit hysteresis in entering and exiting burst mode. For example, at zero load, as input voltage is raised, the PSU may enter burst mode at 410 VDC. After entering burst mode, then input voltage is lowered, it may exit burst mode at 390 VDC.

Selecting the Resonant Capacitor

High frequency operation reduces the capacitance required for the resonant capacitor. However, the ripple current requirements remain a function of the input voltage and power, and do not change much with operating frequency. Many capacitor vendors show an RMS voltage vs. frequency graph instead of specifying the ripple current capability. An example is below in Figure 48.

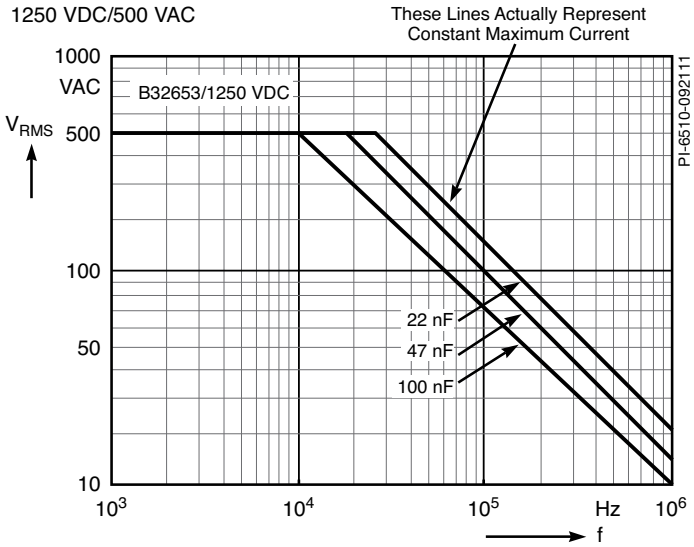

Figure 48. Example of Operating Voltage vs Frequency Graph for Resonant Capacitor.

For any given frequency, the current can be calculated from the voltage on the graph, and the impedance:

$$I_{RMS} = 2 \times \pi \times f \times C \times V_{RMS}$$

The downward slope in the typical specification such as Figure 48 means a relatively flat current with frequency – the capacitor current capability does not go down with increasing frequency.

Output Post-Filter

The output post-filter formed by L1 and C16 in Figure 51 attenuates the ripple on the ceramic capacitors, which typically has a p-p value of 2-3% of the output voltage. When using ceramic output capacitors, the post-filter electrolytic capacitor plays an important role in damping a resonance in the output impedance.

Feedback Loop Design

The HiperLCS's high frequency capability can produce a design with a high loop gain crossover frequency and fast response, but the use of ceramic capacitors requires some special attention in the design of the feedback loop.

The ceramic capacitors and the LLC output impedance form an impedance peak which can appear between 10 kHz and 50 kHz depending on the capacitance value and the LLC power train characteristics. The frequency of this peak is too high for the feedback loop to damp effectively. In order to damp this peak, a post-filter electrolytic capacitor (C16 in Figure 51) is necessary. This capacitor also has a direct impact on the output response to a load step with a fast edge.

The equivalent circuit illustrating the output impedance of an LLC converter is in Figure 49.

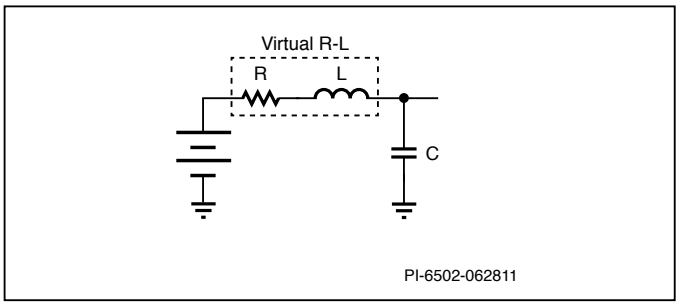

Figure 49. LLC Output Impedance Equivalent Circuit.

The "virtual" series R-L is dependent on the power train parameters. C is the main output ceramic capacitors. The value of the series R is low, on the order of 1-10% of the load impedance.

The shape of the LLC output impedance is shown in Figure 50.

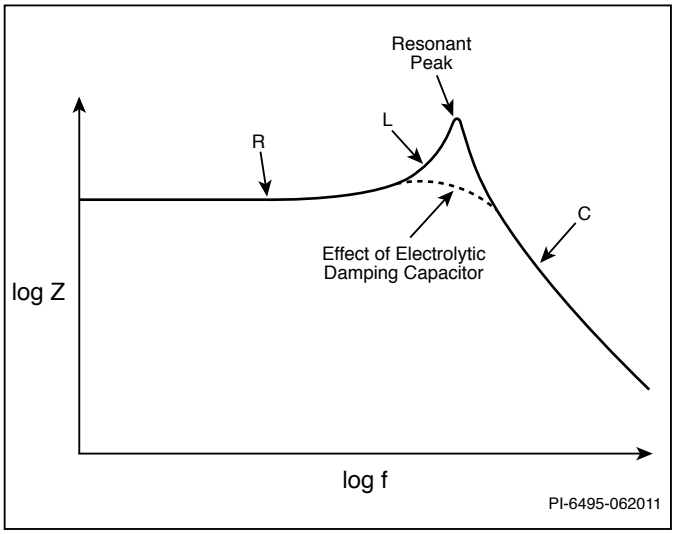

Figure 50. LLC output impedance. The dashed Line Represents the Damping Provided by the Electrolytic Capacitor in the Post-Filter.

The use of ceramic output capacitors without a post-filter electrolytic capacitor, will produce ringing in response to a fast load step, due to the output impedance peak, even when the feedback loop is made very slow.

This output impedance peak can cause instability and oscillation. The impedance peak produces a similar peak in the feedback loop response, visible in the gain/phase plot.

In order to damp the peak, the post-filter electrolytic capacitor's ESR needs to be lower than the characteristic impedance of the ringing:

$$ESR < \frac{1}{2 \times \pi \times f_{RING} \times C}$$

Where f_{RING} is the natural frequency of the peak, and C is the ceramic output capacitance.

The capacitance must be such that the capacitive reactance at the ringing frequency is less than half of the ESR. Put another way, the "zero frequency" of the capacitor must be less than half of the ringing frequency:

$$\frac{1}{2 \times \pi \times ESR \times C} < \frac{f_{RING}}{2}$$

Ultra-low ESR capacitors tend to have high "zero frequencies", approximately 10 kHz, which may be too high in some cases. In this situation a capacitor with higher ESR or higher capacitance may be more effective to damp the ringing.

The post-filter inductance (typically 150-300 nH for a 180-250 kHz design) forms a pole with the electrolytic capacitor ESR at a frequency that is much higher than the ringing frequency and thus is a virtual short-circuit at the frequencies of interest, and does not play a role in the feedback compensation. The inductor's impedance at f_{RING} must be much lower than the ESR. For this reason this inductor value cannot be increased arbitrarily because it will defeat the electrolytic capacitor's ability to damp the peak in the converter's output impedance, and can result in oscillation.

In practice the electrolytic cap may be sized by large step load requirements and burst mode output ripple performance. The resulting capacitor would be larger than is necessary for output damping.

Special attention is also required in the design of the primary and secondary feedback circuits to achieve the high gain crossover frequency and fast response objectives. See Figure 51.

TL431 Circuit

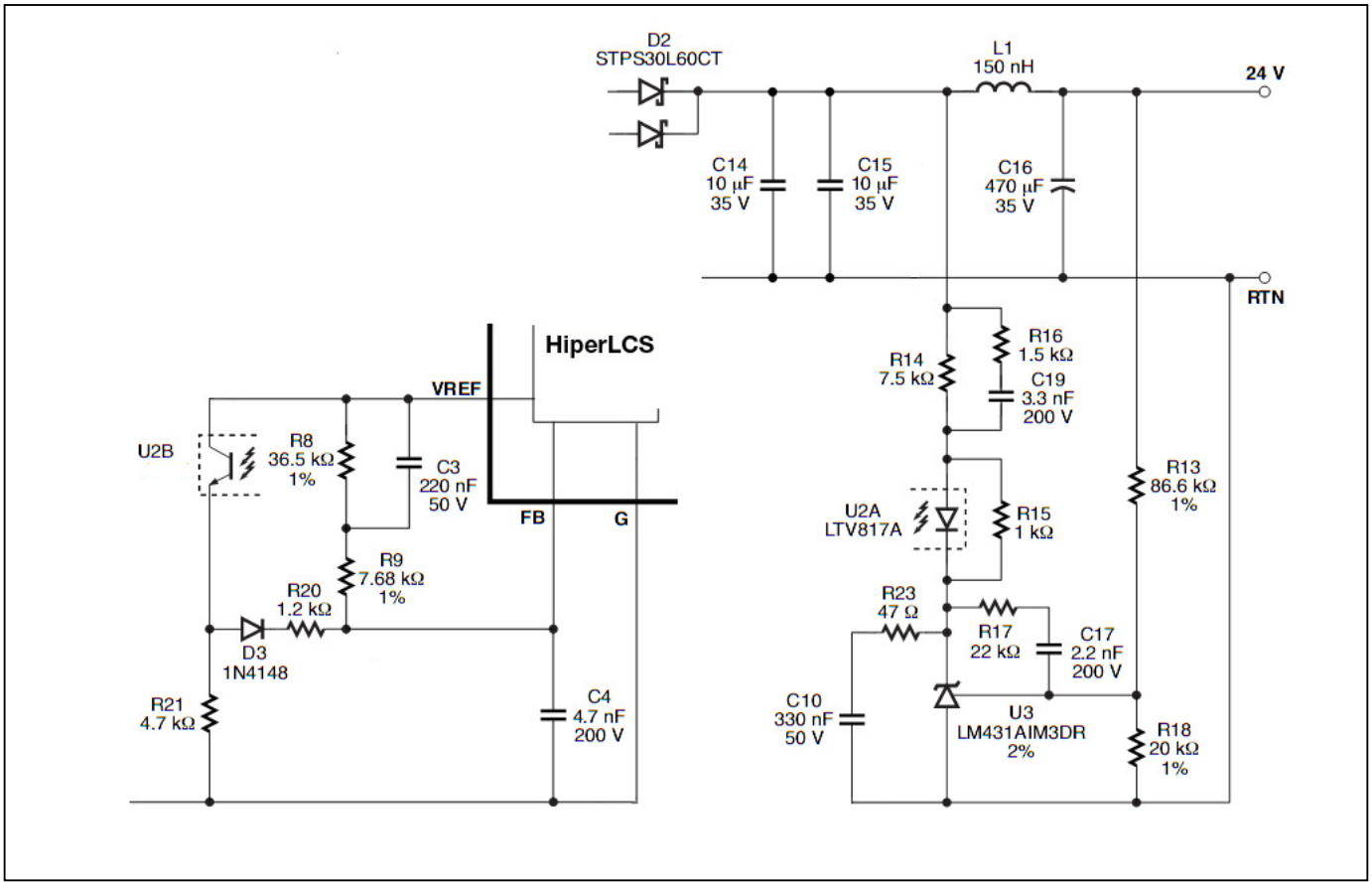

Figure 51. Primary and Secondary Feedback Circuits.

Ensure that the series current-limiting resistor (R14 in Figure 51), is small enough that when the TL431 is saturated, the opto-coupler transistor is capable of saturating even at the minimum CTR specification, assuming 2.0 V on the FEEDBACK pin (worst case condition, bursting at switching frequency equal to f_{MAX}), and FEEDBACK pin current = I_{FMAX} (current at f_{MAX}). If there is insufficient DC gain the output voltage will rise above the regulation set point at zero load, high-line. R15 sets a minimum current for the TL431 as per its data sheet. This current is equal to the V_F of the optocoupler diode, divided by R15's value.

R14 and R21 (optocoupler load), are the main gain setting components. R21 forms a current divider with the sum of R20 and the parallel combination of R9 and the FEEDBACK pin input resistance, which is nominally 2.5 kΩ.

If R21 is reduced or R14 is increased, the AC and DC gain will decrease, and the designer must ensure that there is enough gain in the optocoupler to drive the FEEDBACK pin to 2.0 V at I_{FMAX}.

If a gain reduction is necessary but the optocoupler has insufficient DC gain, then a series RC network across R21 can be used. See Figure 52.

The values shown are typical. The network is used to increase the gain margin by adding a pole near the point where the output impedance begins to rise towards the peak (see Figure 50).

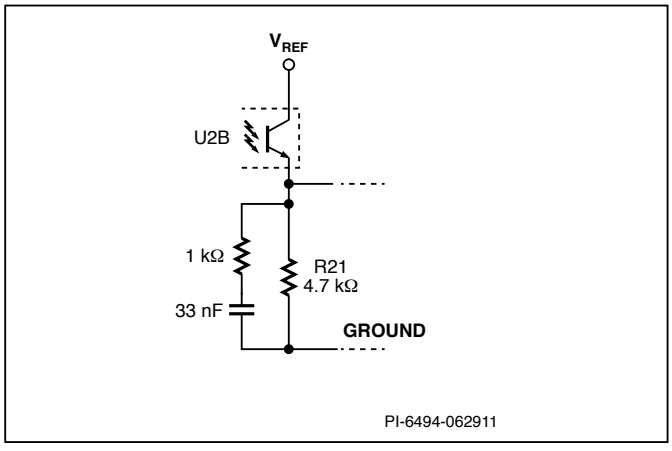

Figure 52. High-Frequency Gain Reduction Circuit.

In many cases, when the gain reduction circuit in Figure 52 is used, the RC "phase lead" network (R16 and C19 in Figure 51) should be removed.

R16 and C19 form a high frequency phase-lead network which is used to increase the phase margin and the gain crossover frequency. Its effect is the opposite of the gain reduction circuit in Figure 52.

TL431 feedback network R17 and C17 shape the low frequency gain (R16 and C19 override it at higher frequencies). C10 is a "soft-finish" capacitor which reduces output voltage overshoot at start-up. R23 merely prevents C10 from appearing as a load to the TL431. C10 has no impact on the small-signal response of the circuit because the output impedance of the TL431 at its cathode is very small compared to the value of R23.

R17 may have only a small effect on the gain/phase plot but it improves start-up overshoot significantly.

The LLC shows maximum DC and low frequency gain at low-line, full load, so any stability issues will usually appear at this condition. Ensure that the LLC does not burst into oscillation during hold-up time due to the increased gain at low input voltage.

The bypass capacitor on the FEEDBACK pin forms a pole with the FEEDBACK pin input resistance (which is nominally 2.5 kΩ). This pole can insert a significant phase shift at the gain cross-over frequency, which is typically 2-10 kHz for a 250 kHz design. This pole can be compensated for with the phase lead RC network (R16 and C19 in Figure 51) on the TL431.

Ceramic Bypass Capacitors

SMD bypass capacitors for HiperLCS are preferred because the small size allows for a very tight layout. Ceramic SMD capacitors are prone to mechanical damage during hand soldering and assembly.

Output Diodes

The output diode peak inverse voltage, not counting the voltage spike, in an LLC, is

$$PIV = 2 \times (V_O + V_D)$$

With careful layout and intertwined secondary halves, and if the LLC only operates slightly above resonance at high-line, the PIV increase due to the voltage spike can be as little as 20%. This voltage will also increase if there is significant switching frequency ripple (See Figure 42 for sinusoidal waveshape at 2x the switching frequency) on the main output capacitors.

Special low forward-voltage Schottky diodes often begin to show increased total losses at T_J > 85 °C, due to increased reverse leakage losses, and thus need to be run at lower temperatures than standard Schottkys in order to achieve high efficiency.

Synchronous Rectifiers

Synchronous rectifiers can be used with HiperLCS. The key features necessary for high frequency operation are:

- Controller has high frequency capability – long propagation delays will reduce the potential efficiency gains
- Synchronous MOSFETs for high-frequency must have low Q_{GS}. Lower voltage MOSFETs have a lower Q_{GS} for a given R_{DS-ON}. If a Q_{GS} vs. voltage graph is used using several values of V_{DS}, use the value for V_{DS} = 0, because the turn-on of a synchronous MOSFET happens at V_{DS} = 0. A good figure of merit is $Q_{GS} \times R_{DS}$

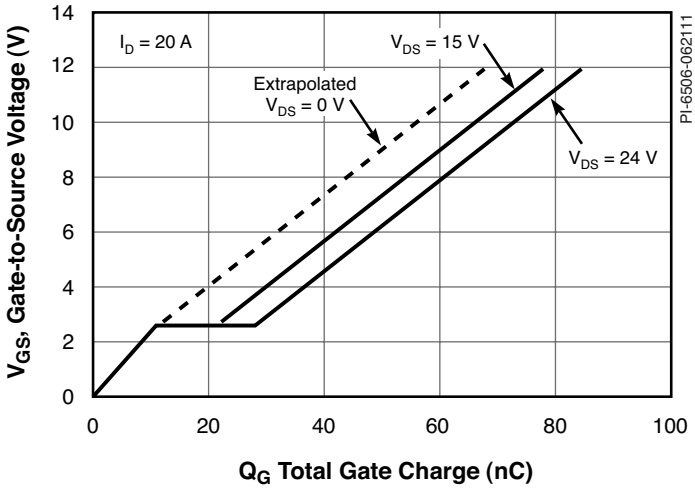

Figure 53. Showing Typical Gate Charge Curve, for a 5 MΩ Sync-Rec MOSFET Suitable for a 12 V / 20 A Output. Extrapolate the Curve for VDS = 0. The Useful Figure of Merit in this Example is 5 MΩ × 65 nC = 325 pΩ-C.

- Tight layout – this reduces the Drain voltage spike, allowing lower voltage MOSFETs, and the controllers require accurate sensing for high-frequency operation
- Layout symmetry of the secondary halves is crucial for proper Sync-Rec operation at light load.
- A controller with a bi-phase output is preferred (both MOSFETs controlled by a single controller). This significantly eases the problem of proper operation at light load

Because N-channel MOSFET gate drives are simplest with their Source grounded, synchronous rectifiers are not well suited for multiple outputs with AC Stacking.

Bootstrap Diode

An ultrafast diode (≤ 75 ns) is necessary for the VCCH bootstrap diode (D1 in Figure 1) due to the large reverse-recovery currents seen during the first few cycles of start-up. Double check reverse recovery peak currents at power-up at high temperature.

Auxiliary Supply

The auxiliary supply providing VCC should be regulated to between 11.4 V (maximum VCC turn-on threshold) and 15 V (VCC ABS MAX). A simple Zener + BJT series regulator will work well. (See Figure 56). If the auxiliary supply also provides an output for the PSU, such as a 5 V standby output, the auxiliary supply will need a large output capacitor (220 ~ 470 μF) before the series regulator to provide ride-through energy during a load dump on the standby output. During a load dump, the standby supply may stop switching momentarily, and the capacitor will provide energy to maintain the VCC voltage.

EMI, ESD and Surge Considerations

Integrated transformers have low primary-to-secondary capacitance which reduces EMI common-mode currents. It also makes passing ESD tests easier.

The "start" end of the Primary winding (the end of the primary that will be on the inside) should be the end connected to the HB pin. The other (outside) end of the winding should be the end connected to the resonant capacitor or to B-. The HB node has high dv/dt (fast edges) and will couple dv/dt noise capacitively to the outside and increase EMI. If this end is on the inside, the turns on top of it will act as a Faraday shield.

The core should be electrically grounded to B-. Do not use a "belly band" (shorted outside turn) on an integrated transformer. It will short the strong leakage flux, reduce efficiency, and change the transformer characteristics. For this reason also, avoid mounting the transformer near a wall of a metallic enclosure.

Other recommendations to improve ESD and common-mode surge immunity:

The auxiliary PSU VCC return should be routed to the bulk capacitor B- and not to the HiperLCS S pins. This is so that ESD and surge currents flowing across the auxiliary PSU transformer has a path to the bulk capacitor B- and to the AC inlet. See Figure 55.

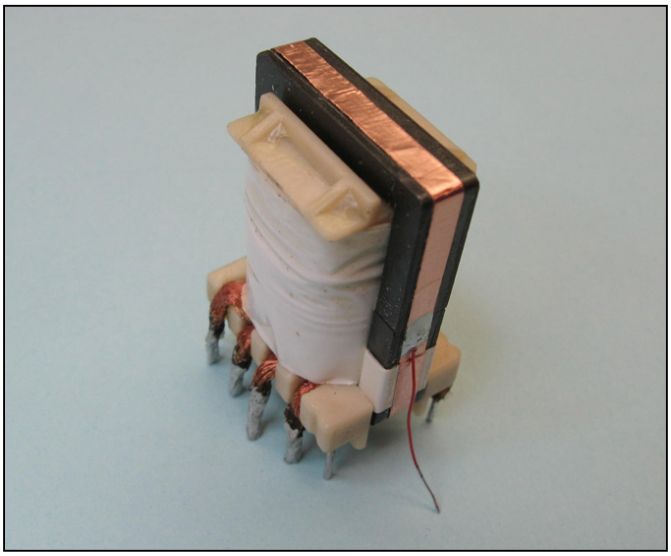

Figure 54. Photo Showing Core Grounding Strap with Pigtail for Soldering to B- Point in PCB.

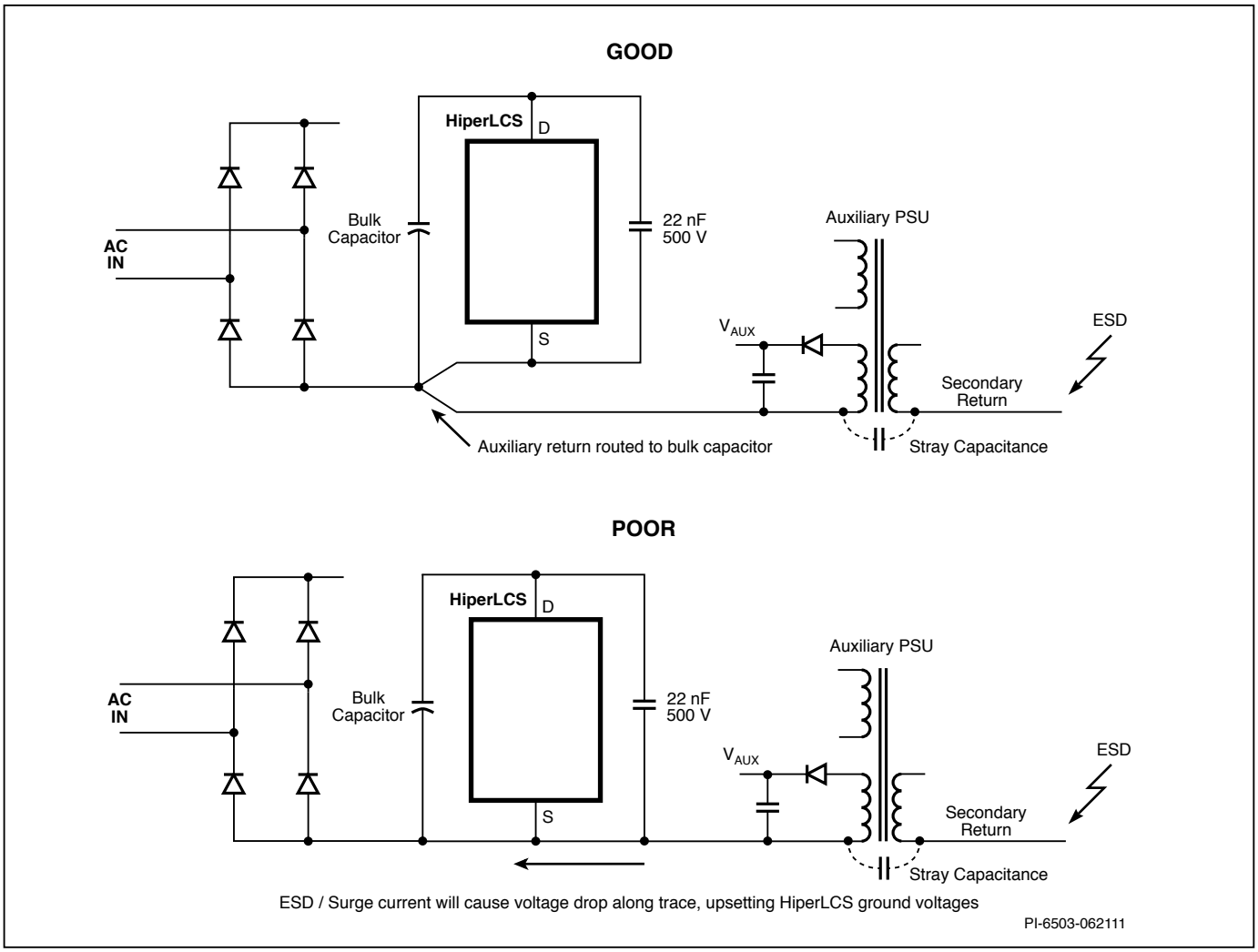

Figure 55. Auxiliary PSU Transformer Return Should be Routed to Bulk Capacitor B- to Improve ESD and Common-Mode Surge Immunity. ESD and Surge Currents Flow from Secondary Through Transformer Stray Capacitance and Back to AC Inlet. See Figure 56 for V_{AUX} Connection to VCC Pin.

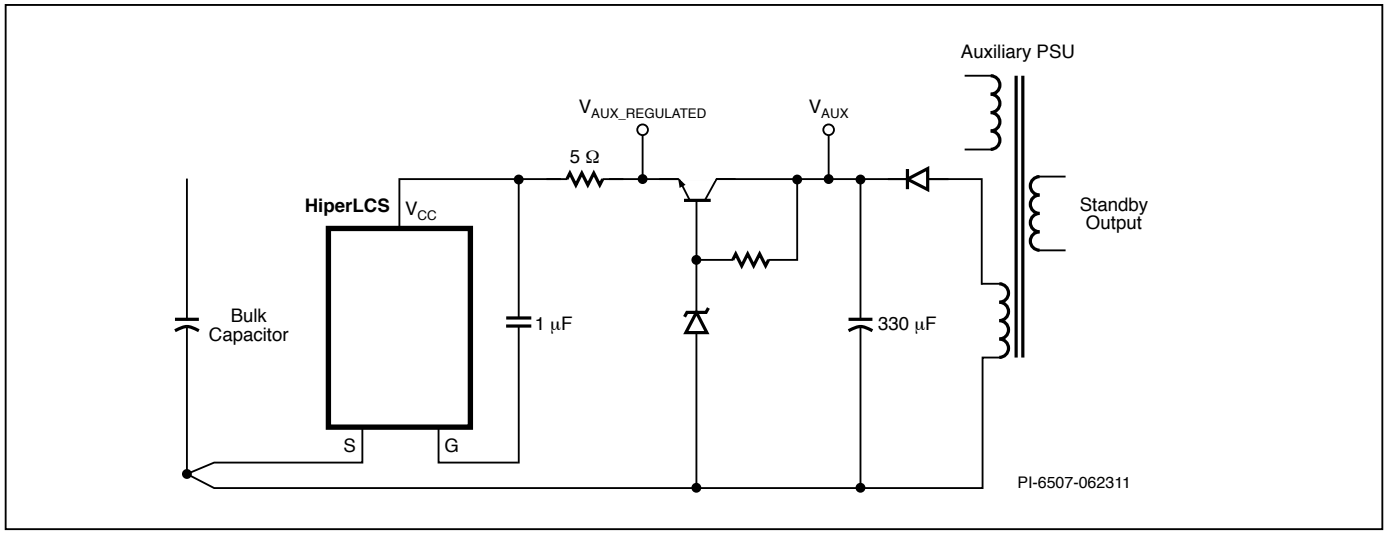

Figure 56. Diagram Showing Auxiliary PSU to HiperLCS VCC Connection. HiperLCS has S and G Pins Internally Connected. Do Not Connect them Externally in the PCB Layout. BJT + Zener Voltage Regulator is Shown. 5 Ω Resistor with 1µF Capacitor Provide Proper VCC Decoupling. 330 µF Capacitor Provides "Hold-Up" during a Load Dump on the Auxiliary Output.

HiperLCS has S and G pins internally connected. Do not connect them externally in the PCB layout. BJT + Zener voltage regulator is shown in Figure 56. The 5 Ω resistor and 1 µF capacitor provide proper VCC decoupling. The 330 µF capacitor provides "hold-up" during a load dump on the auxiliary output.

The Y capacitor connection on the primary should also be routed to the bulk capacitor B- terminal.

The Y capacitor trace connecting to the bulk capacitor B- must not be run close to the optocoupler or FEEDBACK and DT/BF pin PCB traces. If possible, run them on the opposite side of the transformer (see Figure 57). This will reduce inductive coupling of the surge currents into the FEEDBACK pin circuitry.

For improved Surge immunity the transformer must have reinforced isolation from primary to secondary, primary to core and secondary to core. The transformer should pass a Hi-Pot test at the rated surge voltage.

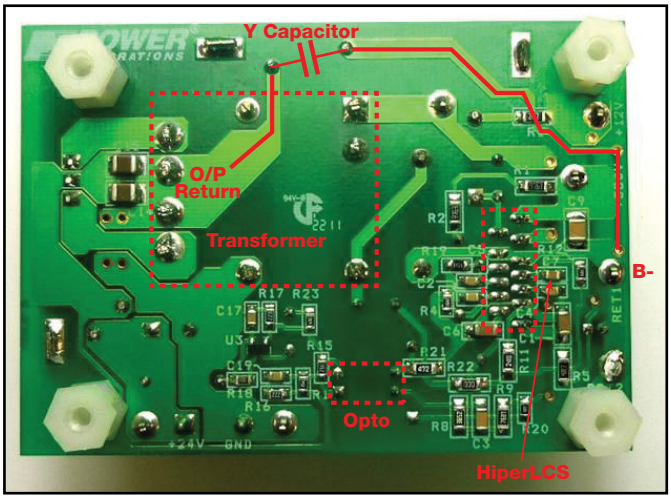

Figure 57. Y Capacitor Returned to B-. Traces run on Opposite Side of Transformer from the Optocoupler and FEEDBACK Pin Circuitry.

Peak Current and SOA Considerations

The Drain and HB MAX repetitive currents can be exceeded during short-circuit testing provided T_J < 100 °C, VD < 400 VDC, for t <460 ns:

Figure 58 is an example of a short circuit waveform where the ABS MAX repetitive peak Drain current of the LCS700 was exceeded.

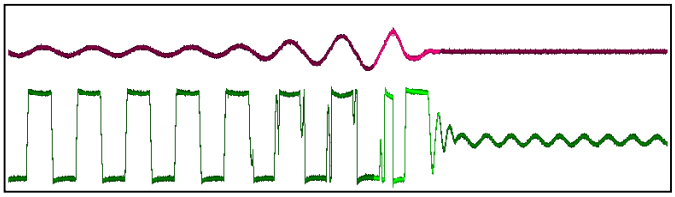

Figure 58. Short-Circuit Waveform.

The waveform is shown zoomed in Figure 59.

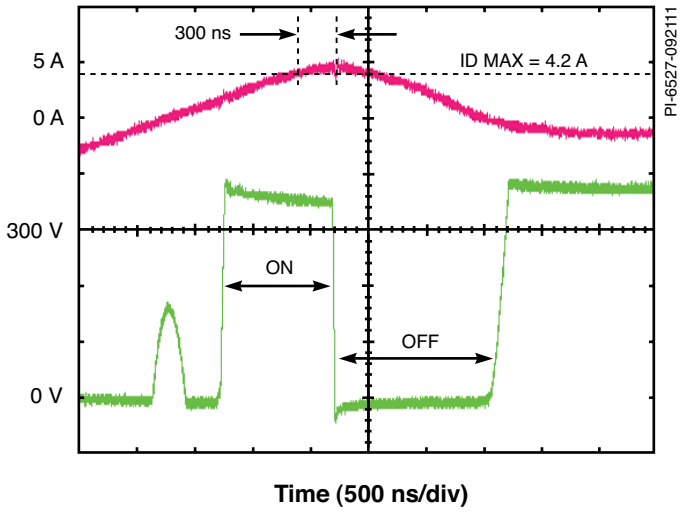

Figure 59. Enlarged Version of Figure 58. Waveforms Showing Correct Measurement of Time During Which I_{MAX} is Exceeded. The I_{MAX} Specification is Exceeded While the High-Side MOSFET is On. "On" and "Off" Refer to the High-Side MOSFET State. The Measured Time is ~ 300 ns.

The time must be measured during the ON-state of the MOSFET. See Figure 59. The current just after the indicated measurement interval flows in the lower MOSFET's body diode and does not stress the MOSFET's SOA capability. In this example t = 300 ns, which is acceptable.

APPENDIX A

Two-Leakage Inductance Model

In this model, turns ratio n is equal to the physical turns ratio, Primary Turns divided by Secondary Turns:

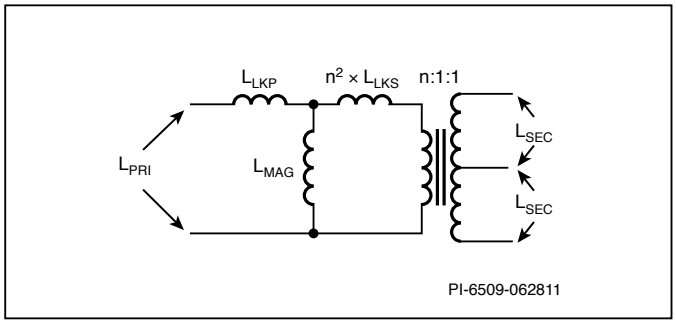

Figure 60. Two-Leakage Integrated Transformer Equivalent Circuit has Separate Primary and Secondary Leakage Inductance. n = Physical Turns Ratio: Primary Turns Divided by Secondary Turns. L_{LKP} is the Primary Leakage Inductance and L_{LKS} is the Secondary Leakage Inductance. It is Shown Reflected to the Primary via Turns Ratio n.

The factor 'm', leakage inductance distribution factor, relates the one-leakage and two-leakage models (see Figure 8), and is calculated from L_{LKP} and L_{LKS}:

$$m = \frac{L_{LKP}}{L_{LKP} + n^2 \times L_{LKS}}$$

m varies from 0~100%. A percentage >50% means that most of the total leakage inductance, as measured from the primary winding, (L_{RES} in Figure 8), is in L_{LKP}. If the location of the transformer gap is closer to the primary, m will decrease, L_{PRI} will decrease, and L_{SEC} will increase, and the transformer will require more turns, than if m = 50%.

L_{SEC} is an input in the spreadsheet (with a default value if left blank), and m is an output. Entering an accurate measured value of L_{SEC} will calculate the actual m and make all the other spreadsheet calculations more accurate.

The valid range of m (1-99%) places a constraint on the valid range of L_{SEC}. If the user enters a value for L_{SEC} outside of this valid range, a warning will appear.

Because n_{EQ} is dependent on L_{SEC}, and $f_{PREDICTED}$ is heavily dependent on n_{EQ}, changing L_{SEC} will change $f_{PREDICTED}$. The accuracy of $f_{PREDICTED}$ is dependent on an accurate value of L_{SEC}.

APPENDIX B

Alternate Secondary Winding Arrangements

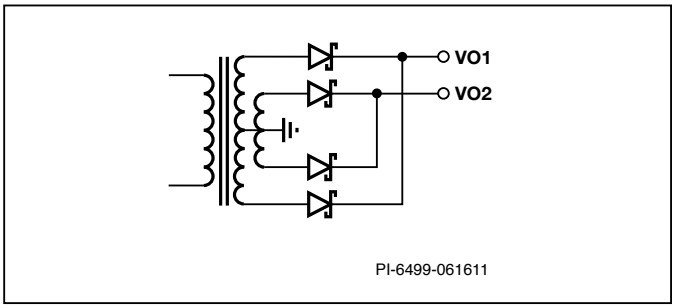

Figure 61. Independent Secondary Windings" for a Two Output Secondary Winding Arrangement.

The output configuration shown in Figure 61 has almost no advantage, thus is non-preferred, over AC Stacking (Figures 4 and 5). The cross-regulation is poorer, and the copper utilization is poor (high losses for a given amount of total copper used). The only time to use this arrangement is if VO_2 is a lower voltage and very low current. It eliminates the need for additional high current pin terminations, which would increase losses. If VO_2 is higher voltage than VO_1 then it is better to simply AC-stack it on top of VO_1.

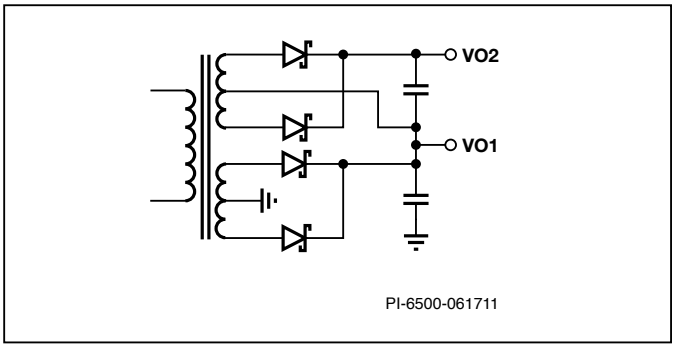

Figure 62. "DC Stacking" Secondary Winding Arrangement for a Two Output Secondary Winding. If the Two Outputs are not Connected it can be Used for Floating, Independent Outputs.

Figure 62 shows the "DC Stacking" winding arrangement. It has lower efficiency than AC Stacking because VO_2 load current passes through two sets of output diodes instead of just one in the case of AC Stacking. This configuration is also non-preferred. It is used if the 2 outputs are isolated from each other – the two windings are simply independent outputs.

Full Bridge

Figure 63 shows the full-bridge secondary arrangement. The secondary current flows through 2 diodes in series, reducing efficiency. The diode voltage stress is approximately equal to the output voltage (as compared to ~ 2 × output voltage for center-tapped secondaries). For these reasons it suited for very high-voltage outputs where the lower voltage diodes have much better reverse recovery characteristics than diodes with double the PIV rating. This will be an advantage for designs which need to run above resonance as diodes are in continuous mode. It also has the advantage of better secondary copper utilization but in most applications this is negated by the total diode drop. Another small advantage is the lack of secondary winding symmetry issues.

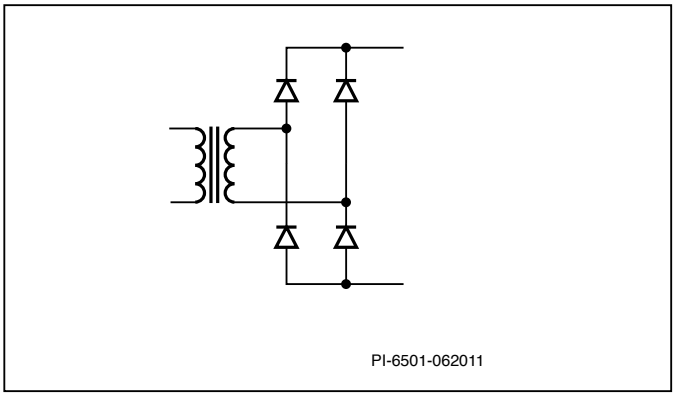

Figure 63. Full-Bridge Secondary Arrangement.

Revision	Notes	Date
A	Initial Release.	06/11
B	Modified Figures 21, 47 and 58. Renumbered Figures starting on page 11.	09/11
C	Updated with new PI style.	09/17

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