Application Note AN-75
LYTSwitch-6 Family

Design Guide

Introduction

The LYTSwitch™-6 series family of ICs dramatically simplifies the development and manufacturing of off-line LED drivers, particularly those in compact enclosures or with high efficiency requirements. The LYTSwitch-6 IC-based architecture is revolutionary, incorporating both primary and secondary controllers, with sense elements and a safety-rated feedback mechanism into a single IC.

Close component proximity and innovative use of the integrated communication link, FluxLink™, permits accurate control of a secondary-side synchronous rectification MOSFET and quasi-resonant switching of the primary integrated high-voltage MOSFET. This together with a proprietary adaptive current limit, variable frequency control scheme maintains high efficiency across the entire load range.

The revolutionary control architecture of LYTSwitch-6 IC allows simple implementation of 3-in-1 and DALI dimming. High power factor is also easy to achieve by a passive single-stage Switched Valley-Fill Power Factor Correction (SVFS^{2}PFC) circuit.

Scope

This application note is intended for engineers designing an isolated AC-DC single-stage switched valley-fill power factor correction (SVFS^{2}PFC) flyback power supply using the LYTSwitch-6 family of devices. It provides a step-by-step design procedure for the selection of all circuit components.

This application note makes use of the PIXls Designer, a spreadsheet based application that gives the power supply engineer more control during the design process. The software is part of the PI Expert™ design software suite which can be downloaded from http://www.power.com/en/design-support/pi-expert-design-software. Online version is also available at http://piexpertonline.power.com.

In addition to this application note the designer may also refer to the many design examples found at www.power.com. They are useful as a starting point for a new design.

Quick Start

Readers familiar with power supply design and Power Integrations design software may elect to skip the step-by-step design approach and use the following information to quickly design the transformer and select the components necessary for a first prototype. For this approach, only the information described below needs to be entered into the PIXls spreadsheet. Other parameters will be automatically selected based on typical design requirements. References to spreadsheet cell locations are provided in square brackets [cell reference].

- Enter AC input voltage range and line frequency, V_{ACMIN} [C3], V_{ACNOM} [C4], V_{ACMAX} [C5], FL [C6], [C7]
- Enter nominal output voltage, V_O [C10]
- Enter continuous output current, I_O [C11]
- Select current limit mode, DEVICE_MODE [C20]
  - Choose between Standard or Increased
- Select LYTSwitch-6 device from drop down list or enter directly [C21]
  - Select the device according to output power and input voltage. (see table 3)
- Enter minimum switching frequency, FS_{MIN} [C38]
  - Choose a value below 50 kHz (optimizes SVFS^{2}PFC)
- Enter the PFC inductance to Flyback inductance ratio, RATIO_LBST_LFB [C50]
  - Starting value of 0.8 for low-line / wide-range application
  - Starting value of 1 for high-line only applications
- Select boost inductor core type, CR_TYPE_BOOST [C56]
- Enter the number of boost layers, L_BOOST [C72]
- Enter desired reflected output voltage, V_{OR} [C78]
- Select flyback transformer core type, CR_TYPE [C84]
- Enter the number of primary layers, L [C102]
  - Adjust the layers if there is a warning on BOBFILLFACTOR [D94]
  - Adjust the layers if there is a warning or info on CMA [D106]

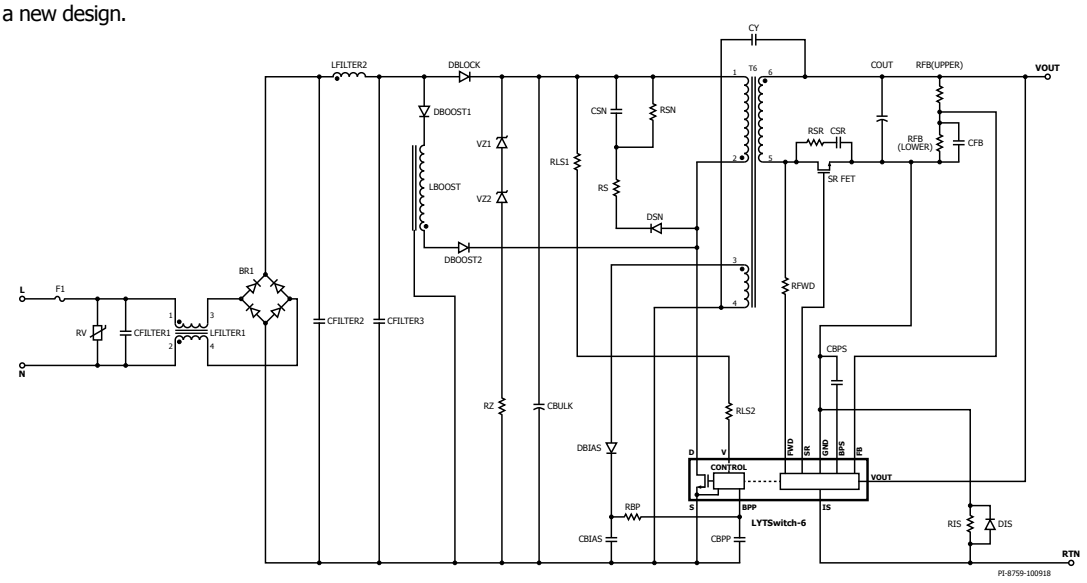


Figure 1. Typical Application Schematic for V_O <24 V.

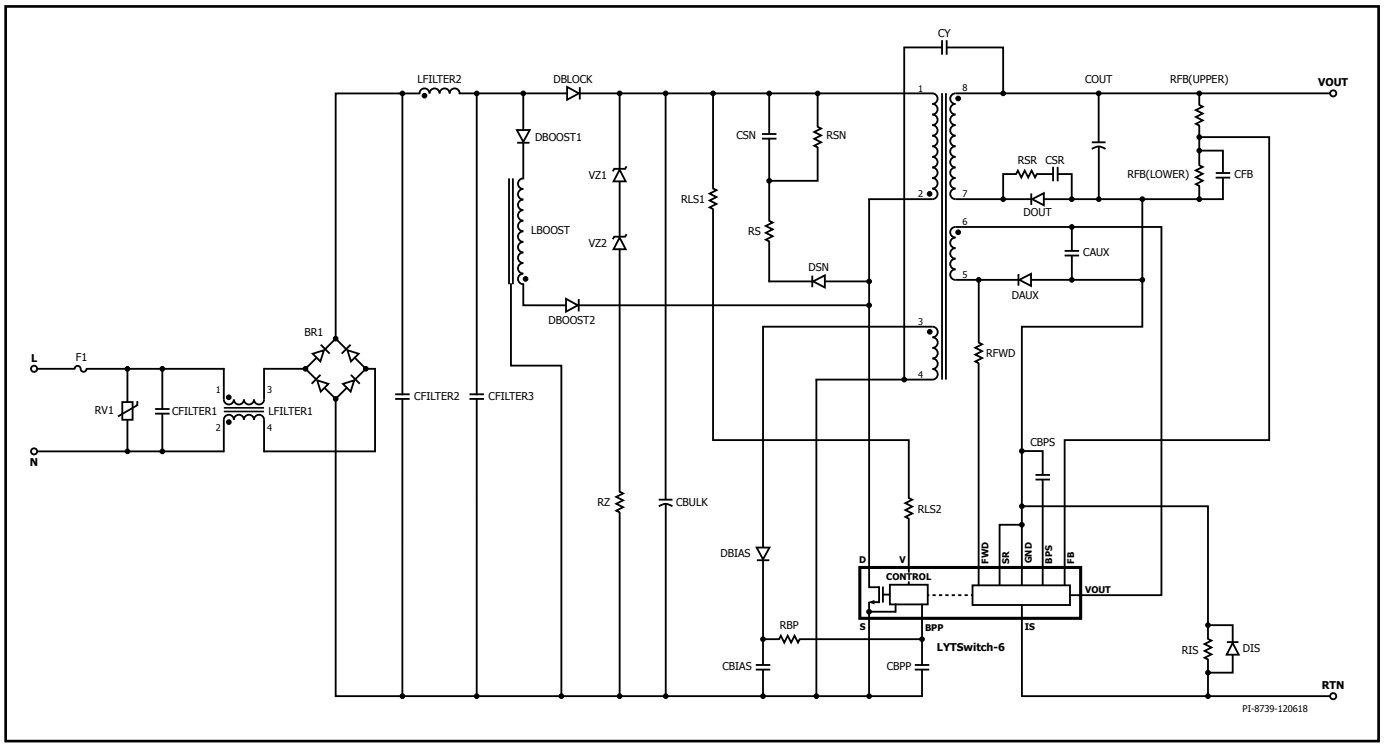


Figure 2. Typical Application Schematic for V_O >24 V.

Step-by-Step Design Procedure

Step 1 – Application Variables

Enter: VACMIN, VACNOM, VACMAX, FL, CIN, VO, IO, n, Z

1	*ACDC_Flyback_PF_LYTSwitch-6_040618; Rev.1.3; Copyright Power Integrations 2018*	*INPUT*	*INFO*	*OUTPUT*	*UNITS*	*Switched Valley-Fill Single Stage PFC (SVF S^2PFC)*
2	**Application Variables**					
3	VACMIN			90	V	Minimum Input AC Voltage
4	VACNOM			230	V	Nominal Input AC Voltage
5	VACMAX			265	V	Maximum Input AC Voltage
6	VACRANGE			UNIVERSAL		Input Voltage Range
7	FL			50	Hz	Line Frequency
8	CIN			60.02	µF	Minimum Input Capacitance
9	V_CIN			450	V	Input Capacitance Recommended Voltage Rating
10	VO	40.00		40.00	V	Output Voltage
11	IO	1.00		1.00	A	Output Current
12	PO			40.01	W	Total Output Power
13	N			88.00	%	Estimated Efficiency
14	Z			0.50		Loss Allocation Factor

Figure 3. Application Variable Section of the Design Spreadsheet.

Input Voltage and Line Frequency:
V_{ACMIN} (V), V_{ACNOM} (V), V_{ACMAX} (V), F_L (Hz)
Determine the input voltage range and line frequency from Table 1.

Region	Nominal Input Voltage (VAC)	Minimum Input Voltage (VAC)	Maximum Input Voltage (VAC)	Nominal Line Frequency (Hz)
Japan	100	85	132	50 / 60
United States, Canada	120	90	132	60
Australia, China, European Union Countries, India, Korea, Malaysia, Russia	230	185	265	50
Indonesia, Thailand, Vietnam	220	185	265	50
Rest of Europe, Asia, Africa, Americas and rest of the world	115, 120, 127	90	155	50 / 60
	220, 230	185	265	50 / 60
	240	185	265	50
Visit: https://en.wikipedia.org/wiki/Mains_electricity_by_country				

Table 1. Input Line Voltage Ranges and Line Frequencies.

Use table 2 as guidance for selecting the bulk capacitance. The recommended voltage rating is given by V_CIN.

Input Voltage (VAC)	Input Bulk Capacitance per Watt Output Power (µF/W)
100 / 115	1 to 1.5
230	0.5 to 1
85 - 265	1 to 1.5

Table 2. Recommended Bulk Capacitance.

Nominal Output Voltage, VO (V)
Enter the nominal output voltage of the main output in the constant voltage operating region. This value is recommended to be at least 3 V higher than the maximum LED voltage.

Output Current, I_o (A)
Enter the maximum continuous LED load current.

Output Power, PO (W)
This is a calculated value based on the output voltage and current.

Estimated Efficiency, n
The default value is 88%. Once the prototype is completed, update value with the measured efficiency and fine tune the components.

Loss Allocation Factor, Z
This factor represents the proportion of losses in the primary and in the secondary of the power supply. Z factor is used together with efficiency to determine the actual power that must be delivered by the power stage. For example, losses in the input stage (EMI filter, rectification, etc.) are not processed by the power stage (transferred through the transformer). Although they reduce efficiency, the transformer design is not effected by these losses.

For designs that do not have peak power requirement, a value of 0.5 is recommended. For designs with a peak power requirement enter 0.65. A higher number indicates a larger proportion of secondary-side losses.

$$Z = \frac{\text{Secondary Losses}}{\text{Total Losses}}$$

Step 2 – Parametric Calculation Basis

Select: PARcalcBASIS, Flyback_Ind_Basis, Boost_Ind_Basis

1	*ACDC_Flyback_PF_LYTSwitch-6_040618; Rev.1.3; Copyright Power Integrations 2018*	*INPUT*	*INFO*	*OUTPUT*	*UNITS*	*Switched Valley-Fill Single Stage PFC (SVFS^2PFC)*
15	Calculations Basis					
16	PARcalcBASIS	Worst_Case		Worst_Case		Calculated Results Based on Selected VAC - VACNOM,VACMAX,VACMIN or Worst Case only
17	Flyback_Ind_Basis	Nom		Nom		Calculated Results Based on Selected LP - Min = LP_MIN, Nom = LP_NOM, Max = LP_MAX
18	Boost_Ind_Basis	Nom		Nom		Calculated Results Based on Selected LBOOST - Min = LBOOSTMIN,Nom = LBOOSTNOM,Max = LBOOSTMAX

Figure 4. Parametric Calculation Basis Section of the Design Spreadsheet.

1	*ACDC_Flyback_PF_LYTSwitch-6_040618; Rev.1.3; Copyright Power Integrations 2018*	*INPUT*	*INFO*	*OUTPUT*	*UNITS*	*Switched Valley-Fill Single Stage PFC (SVFS^2PFC)*
30	Calculated Electrical Parameters Based on Specified Basis					
31	Boost Converter					
32	IBOOSTRMS			439.72	mA	Boost RMS current
33	IBOOSTMAX			1092.16	mA	Boost PEAK current
34	IBOOSTAVG			313.88	mA	Boost AVG current
35	IINRMS			673.27	mA	Input RMS current
36	PF_est			0.7524		Estimated Power Factor

Figure 5. Calculated Electrical Parameters Section of the Design Spreadsheet.

Parametric Calculation Basis, PARcalcBASIS
This parameter provides information about the converter electrical parameters at a set input voltage. This affects the values of boost current, FET current, flyback transformer current (RMS, max, average), as well as the estimated power factor and K_P.

The selection of 'Worst_Case' is recommended in order to confirm that critical parameters like K_P and FS_{MAX} are within acceptable limits under worst-case conditions.

Flyback Inductance Basis, Flyback_Ind_Basis
Select the flyback inductance tolerance that will be used in the calculation. It is set to nominal (Nom) by default.

Boost Inductance Basis, Boost_Ind_Basis
Select the boost inductance tolerance that will be used in the calculation. It is set to nominal (Nom) by default.

PF Estimate, PF_est
The estimated power factor, PF_est, might appear low if the calculation is made at the worst-case input voltage and component tolerances. Unless PF needs to be guaranteed at the minimum input voltage, it is recommended to perform the calculation using VACNOM when estimating for power factor and verify actual values during prototype testing.

Step 3 – Primary Controller Section

Enter: Device Name, Current Limit Mode, Breakdown Voltage

1	*ACDC_Flyback_PF_LYTSwitch-6_040618; Rev.1.3; Copyright Power Integrations 2018*	*INPUT*	*INFO*	*OUTPUT*	*UNITS*	*Switched Valley-Fill Single Stage PFC (SVFS^2PFC)*
19	Primary Controller Section					
20	DEVICE_MODE	Increased		Increased		Device Current Limit Mode
21	DEVNAME	LYT6068C		LYT6068C		PI Device Name
22	RDSON			1.53	Ohm	Device RDSON at 100degC
23	ILIMITMIN			1.683	A	Minimum Current Limit
24	ILIMITTYP			1.850	A	Typical Current Limit
25	ILIMITMAX			2.017	A	Maximum Current Limit
26	POUT_MAX			55.000	W	Power Capability of the Device based on Thermal Performance
27	BVDSS	Auto		650	V	Peak Drain to Source Breakdown Voltage
28	VDS			2.00	V	On state Drain to Source Voltage
29	VDRAIN			544.77	V	Peak Drain to Source Voltage during Fet turn off

Figure 6. Parametric Calculation Basis Section of the Design Spreadsheet.

Device Current Limit Mode, DEVICE_MODE
The device has two current limit options – STANDARD or INCREASED. By default, DEVICE_MODE is set to STANDARD. For designs where lowest cost is a critical requirement, choose INCREASED current limit mode to enable the same device to operate at higher power. Ensure that thermal performance is acceptable.

Device Code, DEVNAME
The power table on LYTSwitch-6 data sheet is based on a non-PF configuration. With the addition of SVFS²PFC circuit, a 20% power derating is recommended when choosing the LYTSwitch-6 device for best efficiency and for optimizing thermal management.

Breakdown Voltage Selection, BV_{DSS} (V)
LYTSwitch-6 ICs are available with 650 V or 725 V primary switch options. For example, LYT6063C describes a 650 V MOSFET device and LYT6073C denotes 725 V.

This option is applicable only when the device code DEVNAME is set to AUTO.

Product	277 VAC ± 15%	85-305 VAC	380 VDC / 450 VDC
	Recommended Power Rating With SVFS²PFC		
LYT6063C / 6073C	12 W	9.6 W	20 W
LYT6065C / 6075C	24 W	20 W	32 W
LYT6067C / 6077C	40 W	36 W	48 W
LYT6068C	55 W	45 W	

Table 3. Device Selection Based on Operating with an SVFS²PFC Stage.

Step 4 – Enter Minimum Switching Frequency

1	*ACDC_Flyback_PF_LYTSwitch-6_040618; Rev.1.3; Copyright Power Integrations 2018*	*INPUT*	*INFO*	*OUTPUT*	*UNITS*	*Switched Valley-Fill Single Stage PFC (SVF S^2PFC)*
37	Flyback Converter					
38	FSMIN	45000		45000	Hz	Minimum Switching Frequency in a Line Period
39	FSMAX			108744.24	Hz	Maximum Switching Frequency in a Line Period
40	KPmin			0.5187		Minimum KP in a Line Period for VAC specified by PARcalcBASIS
41	IFETRMS			803.16	mA	Fet RMS current
42	IFETMAX			1864.84	mA	Fet PEAK current
43	IPRIRMS			0.6058	A	Primary Winding RMS current
44	IPRIMAX			1.6647	A	Primary Winding PEAK current
45	IPRIAVG			0.2479	A	Primary Winding AVG current
46	IPRIMIN			929.59	mA	Primary Winding Minimum current
47	ISECRMS			1.69	A	Secondary RMS current
48	ISECMAX			4.31	A	Secondary PEAK current

Figure 7. Flyback Converter Section of the Design Spreadsheet.

Minimum Switching Frequency, FSMIN (Hz)
Figure 8 shows the typical LYTSwitch-6 + SVFS²PFC switching profile. The minimum frequency occurs at the zero-crossing and increases with line. It resembles an M-shape in a ½ line cycle. It is recommended to set FSMIN below 50 kHz to minimize switching losses. Adjust FSMIN if there is a warning flag on FSMAX.

Maximum Switching Frequency, FSMAX (Hz)
This parameter is the calculated maximum operating frequency based on the chosen FSMIN and parametric calculations. Ideally, FSMAX should be <100 kHz to minimize switching losses. Higher frequency is permitted but regulation, efficiency, and thermal performance should be verified via bench testing.

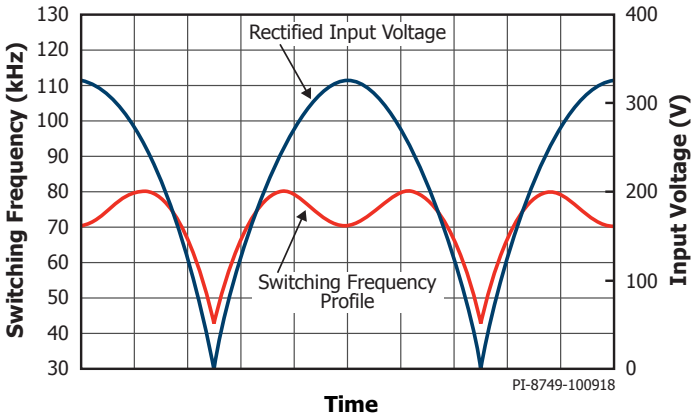


Figure 8. LYTSwitch-6 + SVFS²PFC Switching Profile (Simulated).

Mode of Operation, KP
KP is a measure of how discontinuous or continuous switching is. KP > 1 denotes discontinuous conduction mode (DCM), while KP <1 corresponds to continuous conduction mode (CCM).

KP < 1
In continuous conduction mode (CCM), KP is defined as the ratio of ripple current to the primary peak current.

$$KP \equiv KRP = \frac{I_R}{I_P}$$

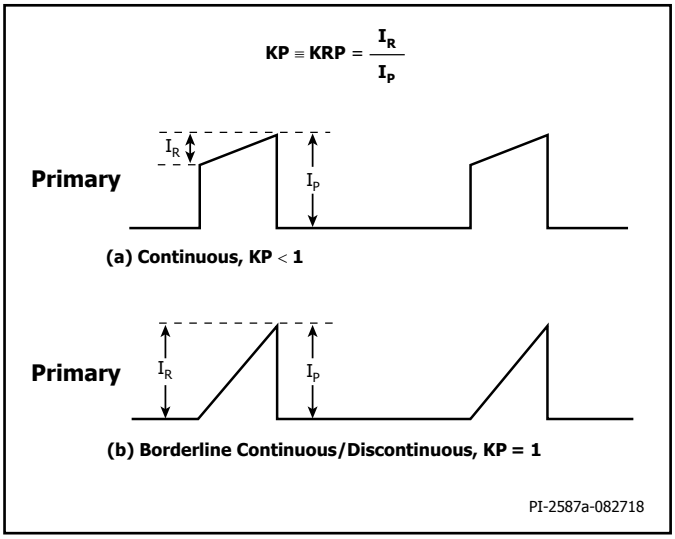


Figure 9. Continuous Conduction Mode Current Waveform, KP < 1.

KP > 1

If the KP >1, it indicates that the converter is operating in discontinuous conduction mode (DCM). In this case, KP is defined as the ratio of the primary MOSFET off time to the secondary rectifier conduction time.

$$KP \equiv KDP = \frac{(1-D)\times T}{t} = \frac{V_{OR}\times(1-D_{MAX})}{(V_{MIN}-V_{DS})\times D_{MAX}}$$

Minimum KP, KPMIN

KPMIN provides information on minimum operating KP based on the selected parameters.

A value of >1 is ideal and usually results in highest efficiency. However, for a universal input, high-power design, KP <1 may be unavoidable. Verify KP_{MIN} at worst-case condition and target KP_{MIN} to be above 0.5. The more continuous operation becomes, the more likely that the PFC inductor will operate in CCM. The PFC inductor needs to operate in DCM for proper operation so if KPMIN is too low, this will force the boost-inductance-to-flyback-inductance ratio (RATIO_LBST_LFB) to also be lower, which could degrade the efficiency.

To increase KP_{MIN}:

- Use INCREASED current limit
- Use larger device
- Increase V_{OR}
- Increase bulk capacitance

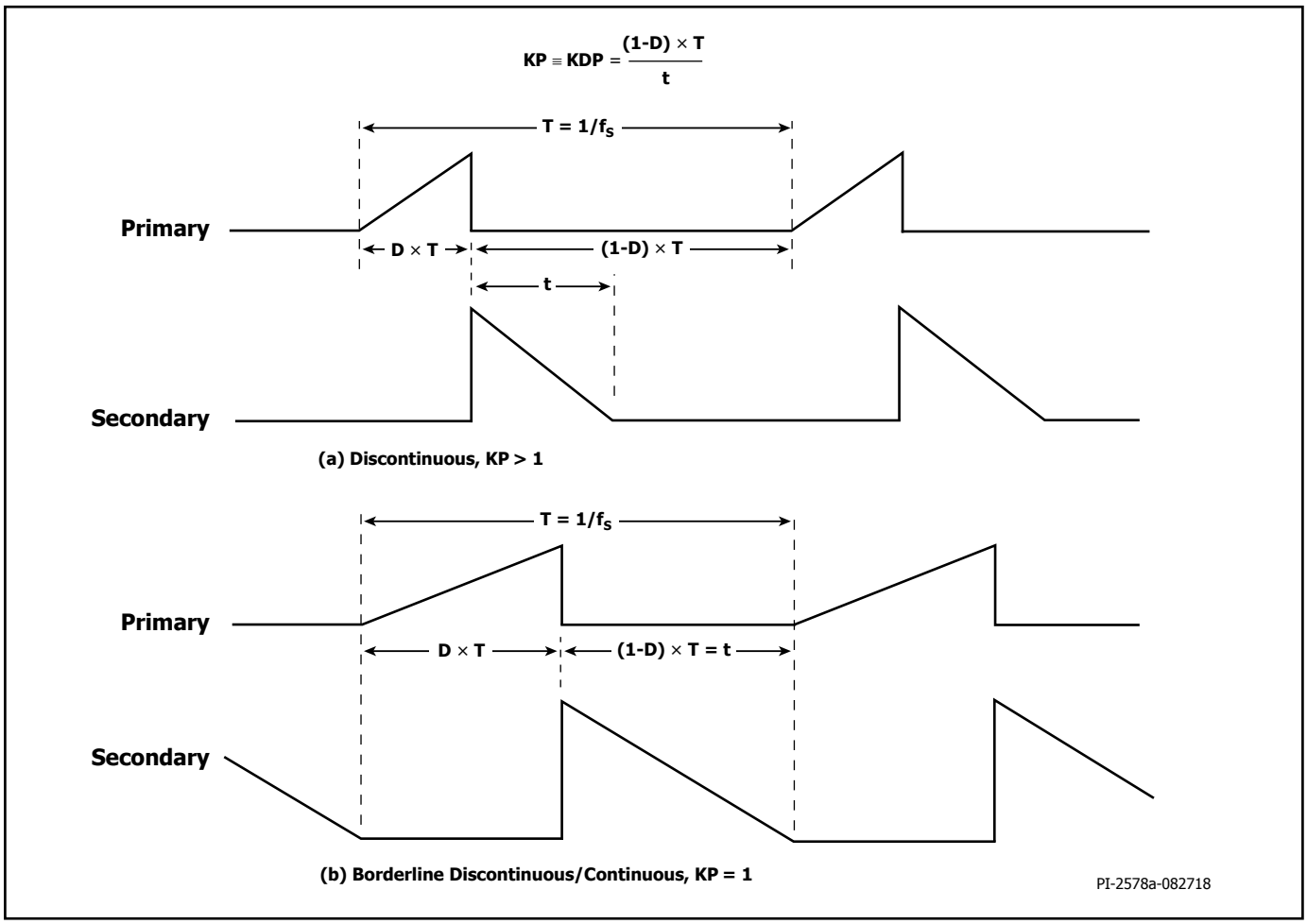


Figure 10. Discontinuous Conduction Mode Current Waveform, K_p > 1.

Step 5 – PFC (Boost) Parameters

Enter: RATIO_LBST_LFB, LBOOSTTOL

1	*ACDC_Flyback_PF_LYTSwitch-6_040618; Rev.1.3; Copyright Power Integrations 2018*	*INPUT*	*INFO*	*OUTPUT*	*UNITS*	*Switched Valley-Fill Single Stage PFC (SVFS^2PFC)*
49	Boost Choke Construction Parameters					
50	RATIO_LBST_LFB	0.8		0.8000		Boost Inductance and Flyback Primary Inductance Ratio
51	LBOOSTMIN			512.07	µH	Minimum Boost Inductance
52	LBOOSTNOM			568.96	µH	Nominal Boost Inductance
53	LBOOSTMAX			625.86	µH	Maximum Boost Inductance
54	LBOOSTTOL			10.00	%	Boost Inductance Tolerance

Figure 11. PFC (Boost) Inductor Section of the Design Spreadsheet.

Boost Inductance to Flyback Primary Inductance Ratio, RATIO_LBST_LFB

The selected FSMIN determines the required flyback primary inductance. The PFC (boost) inductance is determined by the value in the RATIO_LBST_LFB cell, the ratio between the boost inductance (LBOOST_NOM) and the flyback inductance (LP_NOM).

$$RATIO\_LBST\_LFB = \frac{LBOOSTNOM}{LPNOM}$$

The default value for low-line/universal input is 0.8. For high-line, the default value is 1. A lower ratio increases the PF (Figure 12), but degrades efficiency (Figure 13). Table 4 summarizes the benefits and disadvantages selecting a lower ratio.

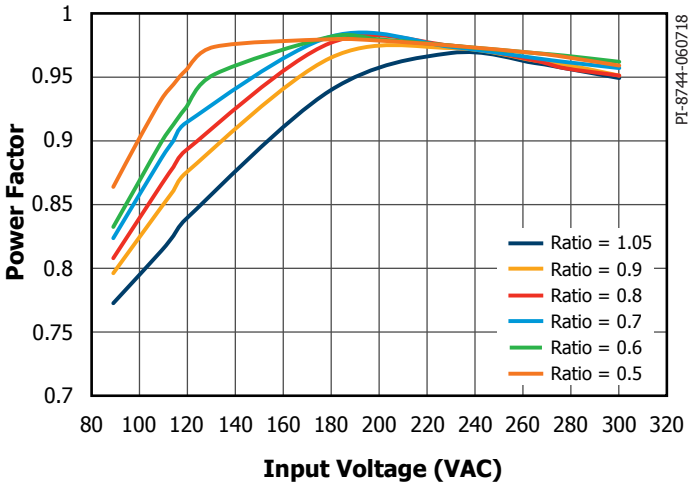


Figure 12. Power Factor vs. RATIO_LBST_LFB.

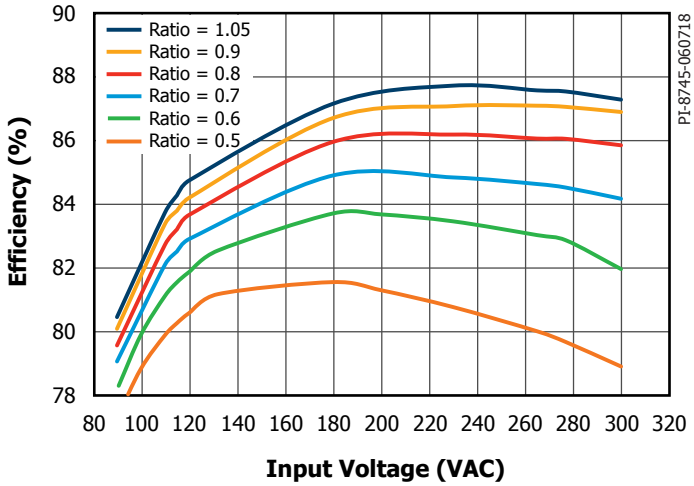


Figure 13. Efficiency vs. RATIO_LBST_LFB.

Effect of Lower RATIO_LBST_LFB Value on Various Parameters

Parameter	Impact
Power Factor	Higher
Efficiency	Lower
A-THD	Lower
No-Load Input Power	Higher
No-Load Bulk Voltage	Higher
Maximum Operating Switching Frequency	Higher

Table 4. Effect of Lower RATIO_LBST_LFB on Various Parameters.

Nominal Boost Inductance, LBOOST_NOM

This is the target value for the typical boost inductance. This value is dependent on RATIO_LBST_LFB and the flyback inductance. The boost inductor should operate in discontinuous conduction mode (DCM).

Boost Inductance Tolerance, LBOOST_TOL

This parameter is the assumed tolerance for boost inductance. A value of 10% is used by default, a different value may be entered in the grey override cell. A value of 10% is easy to meet for most magnetics vendors, but a lower value will help increase production tolerance.

Step 6 – Boost Inductor Design

Enter: Boost Parameters (AE, LE, AL, VE, AW, BW, NBOOST, L_BOOST, AWG_BOOST)

1	*ACDC_Flyback_PF_LYTSwitch-6_040618; Rev.1.3; Copyright Power Integrations 2018*	*INPUT*	*INFO*	*OUTPUT*	*UNITS*	*Switched Valley-Fill Single Stage PFC (SVFS^2PFC)*
56	CR_TYPE_BOOST	Auto		EE13		Boost Core
57	CR_PN_BOOST			PC40EE13-Z		Boost Core Code
58	AE_BOOST			17.10	mm^2	Boost Core Cross Sectional Area
59	LE_BOOST			30.20	mm	Boost Core Magnetic Path Length
60	AL_BOOST			1130.00	nH/turns^2	Boost Core Ungapped Core Effective Inductance
61	VE_BOOST			517.00	mm^3	Boost Core Volume
62	BOBBINID_BOOST			548		Bobbin
63	AW_BOOST			22.20	mm^2	Window Area of Bobbin
64	BW_BOOST			7.40	mm	Bobbin Width
65	MARGIN_BOOST			0.00	mm	Safety Margin Width
66	BOBFILLFACTOR_Boost			84.21	%	Boost Bobbin Fill Factor
67	Boost Winding Details					
68	NBOOST			107.00		Boost Choke Turns
69	BP_BOOST			3735.79	Gauss	Boost Peak Flux Density
70	ALG_BOOST			49.70	nH/turns^2	Boost Core Ungapped Core Effective Inductance
71	LG_BOOST			0.41	mm	Boost Core Gap Length
72	L_BOOST			6.50		Number of Boost Layers
73	AWG_BOOST			27		Boost Winding Wire AWG
74	OD_BOOST_INSULATED			0.418	mm	Boost Winding Wire Output Diameter with Insulation
75	OD_BOOST_BARE			0.361	mm	Boost Winding Wire Output Diameter without Insulation
76	CMA_BOOST			471.92	Circular Mils/A	Boost Winding Wire CMA

Figure 14. Boost Inductor Construction Section of the Design Spreadsheet.

Boost Inductor Core Type, CR_TYPE_BOOST
By default, the spreadsheet will select the smallest commonly available core suitable for the specified output power. Different core types and sizes from the drop down list are available and if the user-preferred core is not available, the grey override cells (AE_BOOST, LE_BOOST, AL_BOOST, VE_BOOST, AW_BOOST and BW_BOOST) can be used to enter the core and bobbin parameters directly.

Table 5 provides core selection guidelines based on output power. Off-the-shelf drum-type inductors may be used, but a shielded type is recommended to minimize EMI emission.

Boost Inductor Turns, NBOOST
This is the number of turns for the boost winding calculated based on required boost inductance.

Boost Layers, L_BOOST; Boost Winding Wire Gauge, AWG_BOOST
Either boost layers L_BOOST or AWG_BOOST can be set by the user in order to optimize the bobbin fill BOBFILLFACTOR_Boost and winding current capacity CMA_BOOST a value between 200 and 500 Cmil/A is recommended.

	Core and Bobbin Table								
	Core						Bobbin		
Output Power at 75 kHz	Core	Code	AE (mm^2)	LE (mm)	AL (nH/T^2)	VE (mm^3)	Code	AW (mm^2)	BW (mm)
< 15 W	EE8.3	B-EE8-H	7.0	19.2	610	154	B-EE8.3-H	6.96	4.78
15 W – 30 W	EE10	PC47EE10-Z	12.1	26.1	850	300	B-EE10-H	12.21	6.60
30 W – 45 W	EE13	PC47EE13-Z	17.1	30.2	1130	517	B-EE13-H	18.43	7.60
> 45 W	EE16	PC47EE16-Z	19.2	35.0	1140	795	B-EE16-H	14.76	8.50

Table 5. Commonly Available Cores and Power Levels at Which These Cores can be used for Typical Boost Inductor Design.

Step 7 – Design the Flyback Transformer

Enter: VOR, Core Parameters, L, AWG, NS

1	*ACDC_Flyback_PF_LYTSwitch-6_040618; Rev.1.3; Copyright Power Integrations 2018*	*INPUT*	*INFO*	*OUTPUT*	*UNITS*	*Switched Valley-Fill Single Stage PFC (SVF S^2PFC)*
77	Flyback Transformer Construction Parameters					
78	VOR	100.00		100.00	V	Secondary Voltage Reflected in the Primary Winding
79	LP_MIN			640.08	µH	Minimum Flyback Inductance
80	LP_NOM			711.20	µH	Nominal Flyback Inductance
81	LP_MAX			782.33	µH	Maximum Flyback Inductance
82	LP_TOL			10.00	%	Flyback Inductance Tolerance
83	Flyback Core and Bobbin Selection					
84	CR_TYPE	PQ26/20		PQ26/20		Flyback Core
85	CR_PN			PQ26/20-3F3		Flyback Core Code
86	AE			121.00	mm^2	Flyback Core Cross Sectional Area
87	LE			45.00	mm	Flyback Core Magnetic Path Length
88	AL			5200.00	nH/turns^2	Flyback Core Ungapped Core Effective Inductance
89	VE			5470.00	mm^3	Flyback Core Volume
90	BOBBINID			BPQ26/20-1112CPFR		Flyback Bobbin
91	AW			31.10	mm^2	Flyback Window Area of Bobbin
92	BW			9.00	mm	Flyback Bobbin Width
93	MARGIN			0.00	mm	Safety Margin Width
94	BOBFILLFACTOR			58.69	%	Flyback Bobbin Fill Factor
95	Flyback Winding Details					
96	NP			37.00		Primary Turns
97	BP			3630.38	Gauss	Flyback Peak Flux Density
98	BM			3484.88	Gauss	Flyback Maximum Flux Density
99	BAC			1408.39	Gauss	Flyback AC Flux Density
100	ALG			519.51	nH/turns^2	Flyback Core Ungapped Core Effective Inductance
101	LG			0.26	mm	Flyback Core Gap Length
102	L			2.00		Number of Flyback Layers
103	AWG			26		Primary Winding Wire AWG
104	OD			0.465	mm	Primary Winding Wire Output Diameter with Insulation
105	DIA			0.405	mm	Primary Winding Wire Output Diameter without Insulation
106	CMA			467.83	Circular Mils/A	Primary Winding Wire CMA
107	NB			5.00		Bias Turns
108	AWGpBias			32		Bias Wire AWG
109	NS			15.00		Secondary Turns
110	AWGS			25		Secondary Winding Wire AWG
111	ODS			0.760	mm	Secondary Winding Wire Output Diameter with Insulation
112	DIAS			0.455	mm	Secondary Winding Wire Output Diameter without Insulation
113	CMAS			200.71	Circular Mils/A	Secondary Winding Wire CMA

Figure 15. Flyback Transformer Construction Section of the Design Spreadsheet.

Reflected Output Voltage, VOR
This parameter is the voltage seen across the secondary winding during the diode / synchronous rectifier MOSFET (SR FET) conduction-time, reflected back to the primary through the turns ratio of the transformer. VOR can be adjusted to limit Drain-Source voltage of the primary-side MOSFET. VOR should be adjusted to eliminate warnings on the spreadsheet. For design optimization purposes, the following should be considered:

- Higher VOR reduces voltage stress on the output diodes and SR MOSFETs. In some cases this may allow a lower voltage rating and higher efficiency.
- Higher VOR increases leakage inductance which reduces power supply efficiency.
- Higher VOR increases secondary-side peak and RMS current which may increase secondary-side copper, diode and SR MOSFET losses and reduce efficiency.
- Higher VOR makes the KP higher (more Discontinuous or less Continuous) helpful in preventing the device from going into deep CCM at VACMIN.

It should be noted that there are exceptions to the above, especially for very high output currents where the VOR should be depressed to get high efficiency, and higher output voltages above 15 V should be supported with higher VOR to maintain acceptable peak inverse voltage (PIV) across the output SR FET. Optimal selection of VOR depends on the specific application and should be based on a compromise between the factors described above.

Nominal Flyback Inductance, LP_NOM
This is the target value for the nominal transformer primary inductance.

Flyback Inductance Tolerance, LP_TOL
This parameter is the assumed tolerance for the transformer primary inductance. A value of 10% is used by default, a different value may be entered in the grey override cell. While a value of 10% is easy to meet a lower value will reduce production challenges.

Flyback Transformer Core Type, CR_TYPE
By default, the spreadsheet will select the smallest commonly available core suitable for the specified output power. Different core types and sizes may be chosen from the drop-down list. If the user preferred core is not available, the grey override cells (AE, LE, AL, VE, AW and BW) can be used to enter the core and bobbin parameters directly.

	Core and Bobbin Table								
	Core						Bobbin		
Output Power at 75 kHz	Core	Code	AE	LE	AL	VE	Code	AW	BW
			(mm^2)	(mm)	(nH/T^2)	(mm^3)		(mm^2)	(mm)
0 W – 10 W	EE10	PC47EE10-Z	12.1	26.1	850	300	B-EE10-H	12.21	6.60
0 W – 10 W	EE13	PC47EE13-Z	17.1	30.2	1130	517	B-EE13-H	18.43	7.60
0 W – 10 W	EE16	PC47EE16-Z	19.2	35.0	1140	795	B-EE16-H	14.76	8.50
0 W – 10 W	EE19	PC47EE19-Z	23.0	39.4	1250	954	B-EE19-H	29.04	8.80
10 W – 20 W	EE22	PC47EE22-Z	41.0	39.4	1610	1620	B-EE22-H	19.44	8.45
10 W – 20 W	EE25	PC47EE25-Z	41.0	47.0	2140	1962	B-EE25-H	62.40	11.60
20 W – 50 W	EE30	PC47EE30-Z	111.0	58.0	4690	6290	B-EE30-H	41.79	13.20
0 W – 10 W	RM5	PC95RM05Z	24.8	23.2	2000	574	B-RM05-V	10.17	4.90
10 W – 20 W	RM6	PC95RM06Z	37.0	29.2	2150	1090	B-RM06-V	15.52	6.20
20 W – 30 W	RM8	PC95RM08Z	64.0	38.0	5290	2430	B-RM08-V	30.00	8.80
30 W – 50 W	RM10	PC95RM10Z	96.6	44.6	4050	4310	B-RM10-V	45.69	10.00
20 W – 30 W	PQ2020	PQ20/20-3F3	62.6	45.7	2650	2850	P-2036	36.0	12.0
30 W – 50 W	PQ2620	PQ26/20-3F3	121.0	45.0	5200	5470	BPQ26/20	31.1	9.0

Table 6. Commonly Available Cores and Associated Power Ranges Supported for Typical Flyback Transformer Designs.

Safety Margin, MARGIN (mm)
By default, the safety margin is set to 0 which assumes that triple insulated wire will be used for secondary windings. If triple insulated wire is not used, then enter 3.1 for 230 VAC or universal input designs and 1.5 for low-line input (only) designs.

Flyback Primary Turns, NP
This is the number of turns for the main winding of the transformer calculated based on VOR and Secondary Turns NS.

Peak Flux Density, BP
A maximum value of 3600 gauss is recommended to limit the peak flux density at maximum current limit and 132 kHz operation. During an output short, the output voltage is low and little reset of the transformer occurs during the MOSFET off-time. This allows the transformer flux density to staircase, and rise above the normal operating limit, however a value of 3600 gauss at the maximum current limit of the selected device, together with the built-in protection features of LYTSwitch-6 ICs provides sufficient margin to prevent core saturation under these short-circuit conditions.

Maximum Flux Density, B_{MAX} (Gauss)
The low frequency operation resulting from light load can generate audible frequency components which will be amplified by the structure of the transformer, especially if a long core is used. To limit audible noise generation, the transformer should be designed such that the maximum core flux density is below 3000 gauss in normal operation. Following this guideline and using the standard transformer production technique of dip-varnishing practically eliminates audible noise, but optimization of audible noise should be undertaken using simple production transformer alternatives before finalizing the design.

AC Flux Density, BAC (Gauss)
The BAC value can be used for core loss calculation.

Gapped Core Effective Inductance, ALG (nH/N²)
Used to specify the core gap.

Flyback Primary Layers, L
The number of primary layers should be between 1 and 3 and should meet the current capacity guideline of 200 – 500 circular mils/A in designs without forced air cooling. Values above 3 layers are possible but the increased leakage inductance as well as physical fit should be considered.

Primary Winding Wire Gauge, AWG
If the override cell is left blank, then the spreadsheet will calculate the AWG wire size based on the specified number of primary layers **L**.

Primary Bias Turns, NB
Determined by:

$$NB = Ceiling\left(NS \times \frac{VBIAS}{VO} \right)$$

Secondary Turns, N_S
By default, the minimum number of secondary turns is calculated such that the peak operating flux density BP is kept below the recommended maximum of 3600 gauss. Generally, it is not necessary to enter a number in the override cell except in designs where a lower operating flux density is desired.

Step 8 – Primary Components Selection

Enter: Brown-In Voltage, V_{BIAS}, $VF_{\_BIAS}$, Zener Clamp

1	*ACDC_Flyback_PF_LYTSwitch-6_040618; Rev.1.3; Copyright Power Integrations 2018*	*INPUT*	*INFO*	*OUTPUT*	*UNITS*	*Switched Valley-Fill Single Stage PFC (SVF S^2PFC)*
114	Primary Components Selection					
115	Line Undervoltage					
116	BROWN_IN_REQUIRED	70.00		70.00	V	Required AC RMS line voltage brown-in threshold
117	RLS			1.74	MOhm	Two Resistors of this Value in Series to the V-pin
118	BROWN_IN_ACTUAL			69.80	V	Actual AC RMS brown-in threshold
119	Line Overvoltage					
120	OVERVOLTAGE_LINE			290.83	V	Actual AC RMS line over-voltage threshold
121	Bias Voltage					
122	VBIAS			12.00	V	Rectified Bias Voltage
123	VF_BIASDIODE			0.70	V	Bias Winding Diode Forward Drop
124	VRRM_BIASDIODE			62.64	V	Bias diode reverse voltage
125	CBIAS			22.00	µF	Bias winding rectification capacitor
126	CBPP			4.70	µF	BPP pin capacitor
127	Bulk Capacitor Zener Clamp					
128	Use Clamp	Yes		Yes		Bulk Capacitor Clamp Needed? Yes, No or N/A
129	VZ1_V			200.00	V	Zener 1 Voltage Rating (In Series with Zener 2)
130	PZ1_W			1.25	W	Zener 1 Minimum Power Rating
131	VZ2_V			200.00	V	Zener 2 Voltage Rating
132	PZ2_W			1.25	W	Zener 2 Minimum Power Rating
133	RZ			4700.00	Ohm	Resistor in series with Zener 1 and Zener 2

Figure 16. Primary Components Selection Section of the Design Spreadsheet.

Brown-in Voltage, BROWN_IN_REQUIRED (V)
This is the input AC voltage at which the power supply will turn on once the brown-in threshold (I_{UV+}) is exceeded.

Line Sense Resistor, RLS (MΩ)
Line sense resistor RLS sets the brown-in voltage and line overvoltage thresholds. It is typically shown as two resistors in series RLS1 and RLS2 and is connected to the bulk capacitor.

$$RLS = \frac{V_{BROWN\_IN\_REQUIRED} \times \sqrt{2}}{I_{UV+}}$$

Line Overvoltage, OVERVOLTAGE_LINE (V)
This is the input AC voltage at which the power supply will stop switching as soon as the overvoltage threshold (I_{OV-}) is exceeded. Switching is re-enabled when the line overvoltage hysteresis ($I_{OV(H)}$) is reached.

$$OVERVOLTAGE\_LINE = \frac{I_{OV-} \times RLS}{\sqrt{2}}$$

Rectified Bias Voltage, VBIAS (V)
A default value of 12 V is assumed. The voltage may be set to different values, for example when the bias winding output is also used as a primary-side (non-isolated) auxiliary output. Higher voltages typically increase no-load power consumption. Values below 10 V are not recommended since at light load there may be insufficient voltage to supply current to the PRIMARY BYPASS pin which could lead to a significant increase in no-load input power consumption.

Bias Diode Forward Drop, VF_BIASDIODE (V)
A default value of 0.7 V is used. This should be changed depending on the type of diode used for bias winding rectification.

BPP Pin Capacitor, CBPP (µF)
CBPP determines the ILIMIT_MODE of operation for the device. Use 0.47 µF for STANDARD current limit and 4.7 µF for INCREASED current limit. The capacitor can either be an electrolytic or a ceramic type. Surface mount multi-layer ceramic capacitors are preferred for use with double-sided boards as they enable the capacitors to be placed close to the IC. Ceramic X7R (or better) capacitors of at least 25 V voltage rating are recommended.

Primary Bias Supply Components (CBIAS, DBIAS, RBP)
While the PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the voltage on the DRAIN pin whenever the power MOSFET is off, an external bias supply via an additional primary auxiliary winding is commonly employed. This will reduce the no-load power consumption of the IC.

A 22 µF, 50 V, low ESR electrolytic aluminum capacitor is recommended for the bias supply filter, CBIAS. The use of a low ESR electrolytic capacitor is recommended as it reduces no-load input power. Use of ceramic surface mount capacitor is not recommended as this can cause audible noise due to a piezoelectric effect from the capacitor's mechanical structure.

The bias winding rectifier diode DBIAS can either be a standard recovery or a fast recovery type. The former tends to give lower radiated EMI while the latter results to lower no-load input power.

The resistor RBP is selected to ensure that the current supplied by the primary bias supply is higher than the PRIMARY BYPASS pin supply current I_{SSW}. I_{SSW} is calculated as follows:

$$I_{SSW} = \frac{F_{SW}}{132\,kHz} \times (I_{S2} - I_{S1}) + I_{S1}$$

Where:

I_{SSW}: PRIMARY BYPASS pin supply current at operating switching frequency.
F_{SW}: Operating switching frequency (kHz) – the average between FSMIN and FSMAX.
I_{S1}: Non-switching PRIMARY BYPASS pin current (refer to data sheet).
I_{S2}: PRIMARY BYPASS pin supply current at 132 kHz (refer to data sheet).

The BPP voltage will be ~5.3 V if bias current is higher than PRIMARY BYPASS pin supply current. If BPP voltage is ~5.0 V, this indicates that the current through RBP is less than the required PRIMARY BYPASS pin supply current. Ensure that the voltage at the PRIMARY BYPASS pin never falls below 5.0 V except during start-up.

RBP is determined by:

$$RBP = \left(\frac{VBIAS_{NO-LOAD} - 5.3\,V}{I_{SSW}} \right)$$

Bulk Capacitor Zener Clamp Selection
When set to yes, the spreadsheet will calculate the Zener voltage rating (VZ1_V, VZ2_V), the power rating (PZ1_W, PZ2_W), and the series resistor RZ.

PFC Diodes, DBOOST1 and DBOOST2
The PFC diodes (DBOOST1, DBOOST2), placed in series with the PFC inductor LBOOST, provide a current path for the energy stored in the PFC inductor that must be transferred to the secondary-side during the MOSFET off-time. However, the resonant voltage ring from the PFC inductor when the MOSFET turns off will cause a large voltage ring across the PFC diode. Select the PFC diode based on the following:

- For high-line / universal input, use 2 x 600 V, ultrafast-recovery diodes in series.
- For low-line input, use 1 x 600 V, ultrafast-recovery diode.
- A current rating of 1 A is sufficient in most applications but a higher rating may be used to reduce device temperature if necessary.

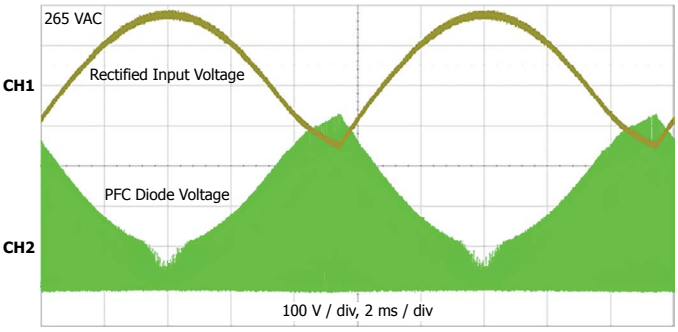


Figure 17. Voltage Stress across the PFC Diode.

Blocking Diode to the Bulk Capacitor, DBLOCK
The blocking diode DBLOCK isolates the rectified AC input from the bulk capacitor. It provides current path for charging the bulk capacitor which improves efficiency especially at low-line.

A standard recovery diode with a voltage rating of 600 V and current rating of 1 A is recommended.

Step 9 – Secondary Controller Components Selection

1	*ACDC_Flyback_PF_LYTSwitch-6_040618; Rev.1.3; Copyright Power Integrations 2018*	*INPUT*	*INFO*	*OUTPUT*	*UNITS*	*Switched Valley-Fill Single Stage PFC (SVF S^2PFC)*
134	Secondary Components Selection					
135	IS pin Components					
136	R_ISpin			33.60	mOhm	Non Standard Value of IS pin 1% resistor
137	Feedback Components					
138	RFB_UPPER			102.00	kOhm	Upper feedback 1% resistor
139	RFB_LOWER			3.30	kOhm	Lower feedback 1% resistor
140	CFB_LOWER			330.00	pF	Lower feedback resistor decoupling at least 5V-rating capacitor
141	CBPS			2.20	µF	BPS pin capacitor

Figure 18. Secondary Components Selection from the Design Spreadsheet.

Current Sense Resistor, RIS (mΩ)
The external current sense resistor, R_ISPIN, sets the constant current (CC) threshold. In the spreadsheet, it is assumed that the specified output current IO is also the CC threshold. The current sense resistor value is therefore calculated as;

$$R\_ISPIN = \frac{I_{SV(TH)}}{IO}; I_{SV(TH)} = 35.9\,mV$$

Current Sense Protection Diode, DIS
This diode is connected across the current sense resistor to protect the device during output short-circuit.

Upper Feedback Resistor, RFB_UPPER (kΩ)
The mid-point of an external resistor divider network (RFB_UPPER, RFB_LOWER) connected between the OUTPUT VOLTAGE and SECONDARY GROUND pins is tied to the FEEDBACK pin to regulate output voltage. The internal voltage comparator reference voltage is V_{REF} (1.265 V).

The default value for RFB_UPPER is 102 kΩ. However, for applications that have stringent no-load input power requirements, this value may be adjusted to reduce no-load consumption especially if the rated output voltage is above 20 V.

Lower Feedback Resistor, RFB_LOWER (kΩ)
The RFB_LOWER resistor is calculated using the RFB_UPPER value.

Lower Feedback Resistor Decoupling Capacitor, CFB_LOWER (pF)
A 330 pF, surface-mount, X7R ceramic capacitor, connected close to the FEEDBACK and GROUND pins of the IC, is recommended.

Secondary Bypass Pin Capacitor, CBPS (µF)
This capacitor works as a voltage supply decoupling capacitor for the integrated secondary-side controller. A surface-mount, 2.2 µF, 25 V, X5R or X7R, ceramic capacitor is recommended.

Forward Pin Resistor, RFWD (Ω)
The FORWARD pin is connected to the Drain terminal of the synchronous rectifier FET (SR FET). This pin is used to sense the Drain voltage of the SR FET and precisely turn-on and turn-off the device. It is also used to provide charge to the SECONDARY BYPASS pin capacitor (CBPS) whenever the output voltage falls below the SECONDARY BYPASS pin voltage.

A 47 Ω, 5% resistor is recommended to ensure sufficient IC supply current and works across a very wide range of output voltages. Changing this value may adversely effect the timing of the synchronous rectifier drive. Care should be taken to ensure that the voltage on the FORWARD pin never exceeds its absolute maximum voltage. If the FORWARD pin voltage exceeds the FORWARD pin absolute maximum voltage (see data sheet), the IC will be damaged.

If secondary auxiliary winding is used, such as when the output voltage is >24 V, then the FORWARD pin is typically connected to the auxiliary winding through RFWD.

Step 10 – Secondary Auxiliary Design

Enter: VAUX, VF_AUX, CAUX

1	*ACDC_Flyback_PF_LYTSwitch-6_040618; Rev.1.3; Copyright Power Integrations 2018*	*INPUT*	*INFO*	*OUTPUT*	*UNITS*	*Switched Valley-Fill Single Stage PFC (SVF S^2PFC)*
142	Secondary Auxiliary Section - For VO > 24V ONLY					
143	Sec Aux Diode					
144	VAUX			12.00	V	Rectified auxiliary voltage
145	VF_AUX			0.70	V	Auxiliary winding diode forward drop
146	VRRM_AUXDIODE			62.64	V	Auxiliary diode reverse voltage
147	CAUX			22.00	µF	Auxiliary winding rectification capacitor
148	NAUX_SEC			5.00		Secondary Aux Turns
149	AWGSAUX			32		Secondary Aux Winding AWG

Figure 19. Secondary Auxiliary Section of the Design Spreadsheet.

Secondary Auxiliary Voltage, VAUX (V)
The OUTPUT VOLTAGE (VOUT) pin has a maximum voltage rating of 27 V. For designs with higher than 24 V output voltage requirements, adding an auxiliary winding for VOUT and FWD pin sensing is recommended.

By default, the secondary auxiliary voltage is set to 12 V.

Auxiliary Diode Forward Drop, VF_AUX (V)
A default value of 0.7 V is used but should be changed on the type of diode used for auxiliary winding rectification.

Auxiliary Rectifier Reverse Voltage, VRRM_AUXDIODE (V)
This parameter is the maximum voltage stress on the secondary rectifier at the maximum input voltage – neglecting the effect of leakage spikes.

Secondary Bias Supply Components (CAUX, DAUX)
A 22 µF, 50 V, low ESR electrolytic aluminum capacitor is recommended for the secondary auxiliary supply filter, CAUX.

The secondary auxiliary winding rectifier diode, DAUX, should be a standard recovery type with a voltage rating of 200 V. While the calculated VRRM_AUXDIODE may be low, the leakage spike may exceed 100 V in conditions such as cold start-up. It should not exceed 150 V which is the FORWARD (FWD) pin maximum voltage rating. Even a short pulse exceeding this value may cause damage to the IC. The R-C snubber on the main output rectifier is usually sufficient to prevent this. Adding an R-C snubber across DAUX is optional, but it should be considered if the leakage spike approaches the 150 V limit.

Step 11 – Output Rectifier and Capacitor Selection

1	*ACDC_Flyback_PF_LYTSwitch-6_040618; Rev.1.3; Copyright Power Integrations 2018*	*INPUT*	*INFO*	*OUTPUT*	*UNITS*	*Switched Valley-Fill Single Stage PFC (SVF S^2PFC)*
154	Output Components					
155	VF			0.70	V	Output diode forward drop
156	VRRM			191.93	V	Output diode reverse voltage
157	COUT			222.22	µF	Output Capacitor - Capacitance
158	COUT_VOpercentRip			2.50	%	Output Capacitor Ripple % of VOUT
159	ICOUTrms			1.37	A	Output Capacitor Estimated Ripple Current
160	ESRmax			232.28	mOhm	Output Capacitor Maximum Recommended ESR

Figure 20. Output Rectifier and Capacitor Section of the Design Spreadsheet.

Output Rectifier Forward Drop, VF (V)
A default value of 0.7 V is used but should be changed to a different type of diode used for rectification of the secondary main output winding.

Output Rectifier Reverse Voltage, VRRM (V)
This parameter is the maximum voltage stress on the secondary rectifier at the maximum input voltage neglecting the effect of leakage spikes. Extra margin must be provided when choosing the voltage rating of the device to account for leakage spikes.

$$VRRM = VOUT + VACMAX \times 1.414 \times \frac{NS}{NP}$$

Output Rectifier, DOUT
Use synchronous rectifier FET (SR FET) whenever possible to get highest efficiency. The SR pin drive voltage has a typical value of 4.4 V. A gate threshold voltage of 1.5 V – 2.5 V is ideal when choosing the SR FET. MOSFETs with a threshold voltage as high as 4 V may be used provided that the data sheet specified $R_{DS(ON)}$ across temperature for a gate voltage of 4.5 V.

For a high output voltage design with a calculated VRRM of >150 V, the SYNCHRONOUS RECTIFIER DRIVE pin needs to be connected to the SECONDARY GROUND pin to allow the use of a low-cost ultrafast diode instead of an SR FET.

Output Rectifier Snubber, RSR (Ω), CSR (nF)
The interaction between the leakage reactance of the output winding and the output capacitance (C_{OSS}) of the output rectifier leads to voltage ringing at the instant of winding voltage reversal when the primary MOSFET turns on. This ringing can be suppressed using an RC snubber connected across the output rectifier. A snubber resistor in the range of 10 Ω to 47 Ω should be used (higher resistance values lead to a noticeable drop in efficiency). A capacitor value of 1 nF to 2.2 nF is adequate for most designs.

Target Output Voltage Ripple for Capacitor Sizing, COUT_VOpercentRip (%)
This parameter sets the target output voltage ripple percentage which is used to calculate the minimum output capacitance.

Output Capacitance, COUT (µF)
The minimum recommended output capacitance, COUT, is calculated based on the target voltage ripple COUT_VOpercentRip. Higher capacitance may be used if lower output current ripple is required. Verification with an actual LED load is needed. Different LED strings have different dynamic impedance characteristics which determine the actual ripple current. A low ESR type capacitor is typically used to reduce output voltage ripple.

Step 12 – Other Key Components Selection

Primary Clamp Network (DSN, RS, RSN, and CSN)

A primary clamp is recommended to ensure that the BV_{DSS} rating of the IC is not exceeded under worst-case conditions (such as output short-circuit at maximum input voltage).

Figure 21 shows three common clamp configurations in the design. Table 7 lists the benefits and disadvantages of each circuit approach.

Common Primary Clamp Configurations

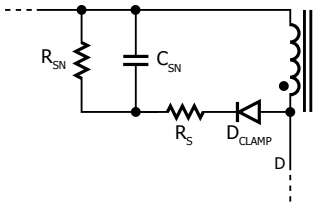
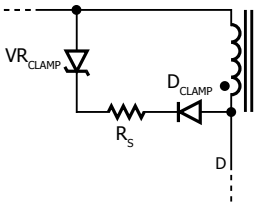
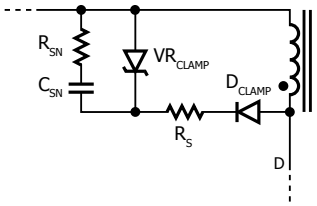
R2CD	Zener	R2CD + Zener
		
PI-8502-041818	PI-8504-041818	PI-8503-041818

Figure 21. Recommended Primary Clamp Components.

Primary Clamp Circuit			
Benefits	**R2CD**	**Zener**	**R2CD + Zener**
Component Cost	Low	Medium	High
No-Load Input Power	High	Low	Medium
Light-Load Efficiency	Low	High	Medium
EMI Suppression	High	Low	Medium

Table 7. Benefits of Primary Clamp Circuits.

Input Filter and Protection

Figure 22 shows the typical input protection components and EMI filter component arrangements used in a typical LYTSwitch-6 design.

Fuse F1 provides over-current protection and isolates the power supply from the AC line in case of catastrophic failure. A time-lag fuse is commonly used to prevent tripping during start-up due to high inrush current from the charging of the bulk capacitor. Use 250 VAC rating for a 230 / 240 VAC input system and 300 VAC rating for a 277 VAC input system. The rated current should be greater than the maximum current at minimum input voltage. Ensure that the I^2t rating is greater than the I^2t measured during inrush and surge events.

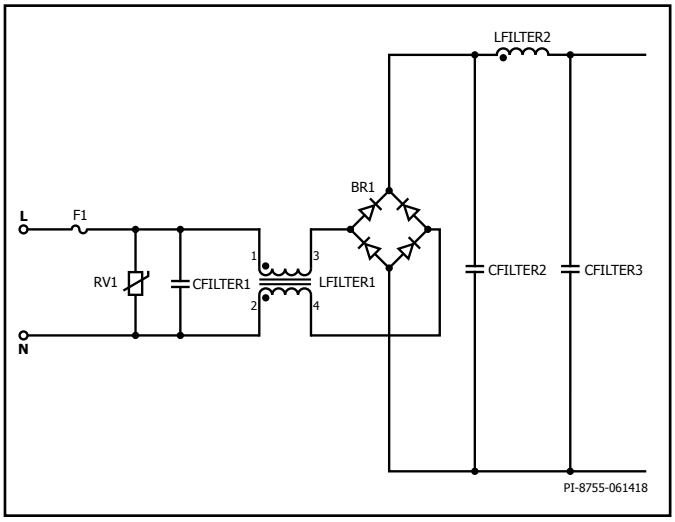


Figure 22. Input Filter Configuration in LYTSwitch-6 Designs.

Bridge rectifier BR1 rectifies the AC line. The voltage rating of the bridge is recommended to be 1 kV especially if 2.5 kV ring-wave immunity is required. The current rating should be greater than the maximum operating current. Choose the appropriate package size based on power dissipation and thermal measurements.

Varistor VR1 protects the unit during a surge event. Its voltage rating should be higher than the maximum AC line voltage.

The EMI filter usually consists of CFILTER1, LFILTER1, CFILTER2, LFILTER2, and CFILTER3. CFILTER2 should be placed after the bridge rectifier especially if a large value of $L_{FILTER2}$ is required. During a line surge or ring-wave, LFILTER2 excitation might create significant oscillation that could exceed the voltage rating of the bridge rectifier.

In order to maintain high power factor, the total input capacitance cannot be made too large. A suitable approximation, use 10 nF/W when sizing the filter capacitance.

Key Application Design Considerations

Bulk Voltage During No-load / Light-load Operation
In every switching period, the bulk capacitor discharges (when it is supplying power) then recharges. The stored energy in the boost inductor will be transferred to the output and also charge the capacitor.

At no-load or very light-load condition (<10% of rated power), the bulk voltage has a tendency to creep-up because the energy from the boost inductor (charging the bulk capacitor) is greater than the converter demands.

If auto-restart is allowed during no-load, then the integrated line overvoltage protection is sufficient. However, in applications such as 3-in-1 dimming or DALI in which the load can vary from 0 to 100%, auto-restart is not allowed.

There are several ways to minimize bulk voltage creep-up:

1. **Use a higher RATIO_LBST_LFB value**. As shown on Figure 23, the no-load bulk voltage is higher as the ratio is decreased. Unless lower ratio is needed to meet the required PF or THD, it is important not to set the ratio lower as this affects the no-load bulk voltage.

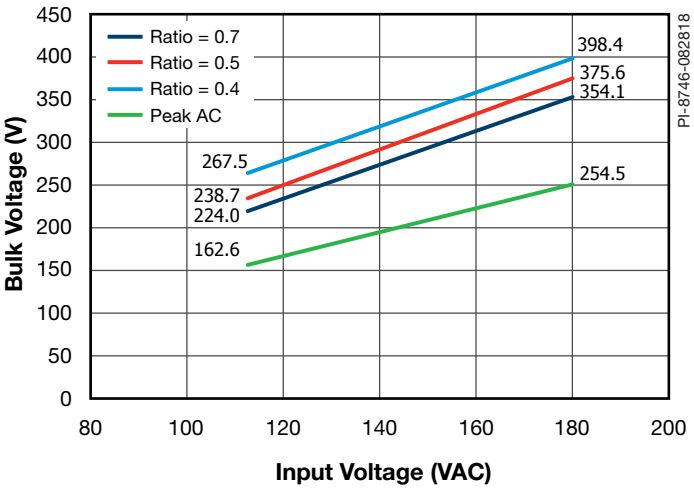


Figure 23. No-Load Bulk Voltage vs LPFC/NOM Ratio.

2. **Use higher rated capacitor**. Increasing the voltage rating of the bulk capacitor may be sufficient in low power designs.
3. **Connect an R-C-D clamp across Drain to Source**. This is a cost-effective solution but results to lower efficiency and higher no-load power.

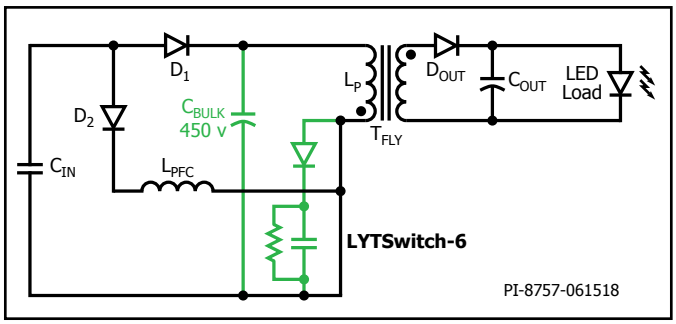


Figure 24. RCD Clamp Connected from Drain to Source.

4. **Connect a Zener clamp across the bulk capacitor**. This provides the best performance at the expense of adding two high-voltage Zener diodes and a resistor.

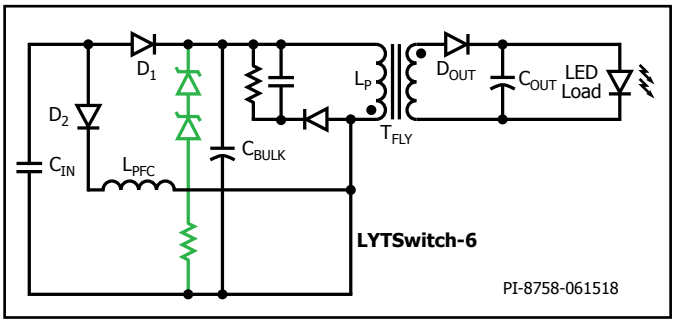


Figure 25. Zener Clamp Connected Across Bulk Capacitor.

Power Delivery in CCM Design When Using Auxiliary Winding for VOUT Pin and FWD Pin Sensing
In DCM operation, the peak voltage on the FWD pin as it rises above the output voltage level is used to gate secondary requests for an "ON" cycle in the primary controller. This feature, called Intelligent Quasi-Resonant Mode Switching, is disabled if the design moves to CCM.

If the FWD pin voltage sensing is done through an auxiliary winding, there is a risk that the controller will not enter CCM because the information given by the auxiliary winding does not match the actual state of the secondary diode. In typical scenario, the main rectifier is still conducting but the secondary controller determines that it is in DCM (the FWD pin voltage crosses 0 V which tells the controller that the current through the rectifier already fallen to 0). When this happens, the converter will be prevented from entering CCM which results to reduced power delivery. Figure 30 shows the effect of CCM mis-detection on output current regulation.

There are two ways to address this condition:

1. Use standard-recovery diode for the auxiliary circuit. Figure 27 shows the FWD pin voltage waveform using standard-recovery diode. Compare that to Figure 28 which shows the same waveform using ultrafast diode. The slow reverse recovery response enables the secondary controller to initiate a switching request while the rectifier is still conducting (CCM). With an ultrafast diode, the FWD pin voltage crosses 0 V which causes the secondary controller to assume that it is in DCM operation. In this case a switching request will not happen until the FWD pin exceeds VO pin voltage.
2. Use sandwich auxiliary winding technique (Figure 26). The coupling between the secondary and auxiliary windings allows the current signal to be sensed by the controller. Figure 29 shows the FWD pin voltage waveform when using sandwiched auxiliary technique.

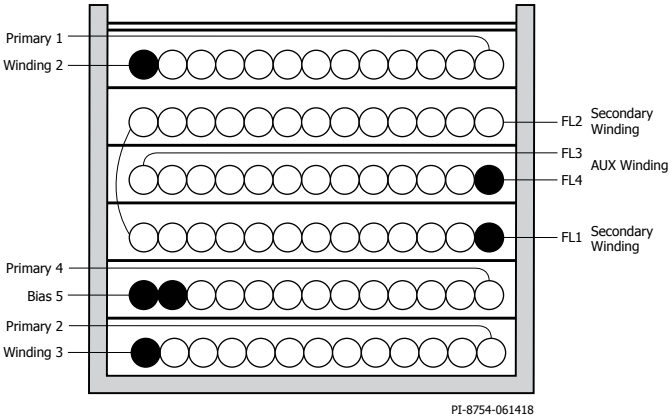


Figure 26. Sandwiched Secondary Auxiliary Winding Transformer Construction.

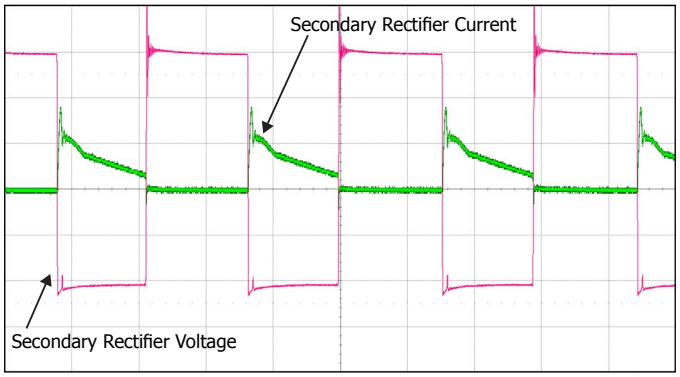


Figure 27. Secondary Rectifier Waveforms with Slow-Recovery Diode.

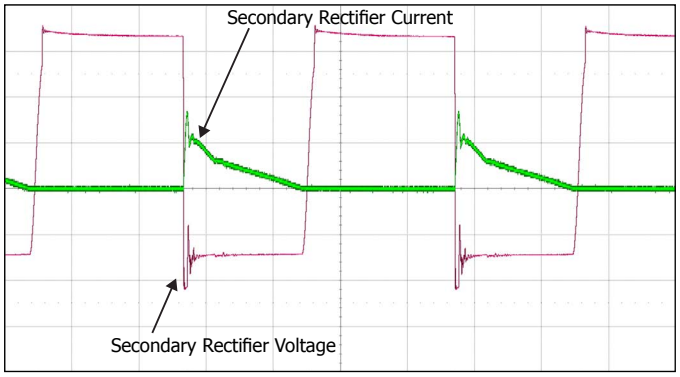


Figure 28. Secondary Rectifier Waveforms with Ultrafast Diode.

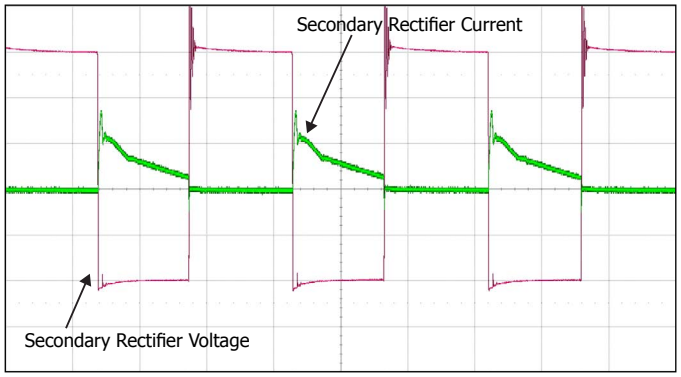


Figure 29. Secondary Rectifier Waveforms with Ultrafast Diode and Sandwiched Auxiliary Windings.

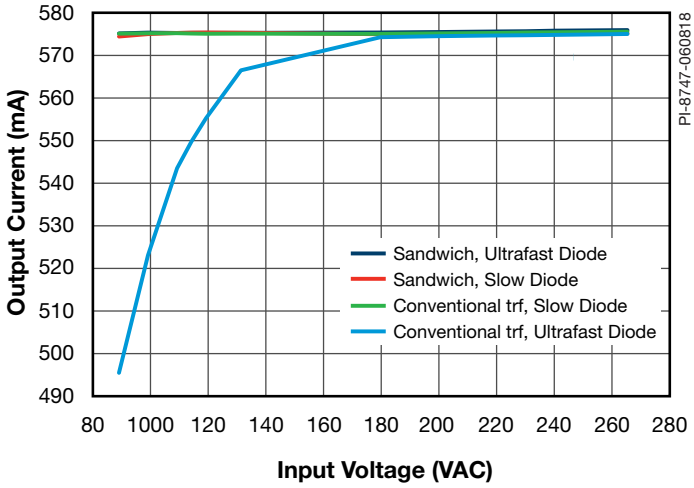


Figure 30. Line Regulation Comparison.

Recommendations For Reducing A-THD

- Use actual LED load.
- Use lower RATIO_LBST_LFB.
- Select a different VOR. Operate close to KP = 1.
- Reduce input filter capacitance and increase filter inductance.

Recommendations For Increasing Power Factor (or Factors affecting PF)

- Use an actual LED load for testing.
- Use lower RATIO_LBST_LFB.
- Reduce input filter capacitance and increase filter inductance.
- Verify that the boost inductor is operating in DCM.
- Increase bulk capacitance.

Recommendations For Reducing No-load Consumption

- Adjust RFB(UPPER) and RFB(LOWER).
- Adjust RBP value.
- Reduce primary clamp capacitance.
- Use schottky or ultrafast diode for bias supply rectifier DBIAS.
- Use low ESR capacitor for bias supply filter capacitor, CBIAS.
- Reduce SR FET RC snubber capacitor, CSR.
- Add tape between primary winding layers, and multi-layer tapes between primary and secondary windings to reduce inter-winding capacitance.

Recommendations For EMI Reduction

- Appropriate component placement and ensuring small loop areas for the primary and secondary power circuits will help minimize radiated and conducted EMI. Care should be taken to achieve compact loop areas.
- A small capacitor in parallel with the clamp diode on the primary-side will help reduce radiated EMI.
- A resistor (2 – 47 Ω) in series with the bias winding helps reduce radiated EMI.
- A small resistor and a ceramic capacitor (<22 pF) in series across primary and/or across secondary main winding (<100 pF) may help reduce conducted and/or radiated EMI. Note that more capacitance will affect no-load consumption.
- Common mode chokes are typically required at the input of the power supply to attenuate common mode noise. The same performance can be achieved by using shield windings in the transformer. Shield windings can also be used in conjunction with the common-mode filter inductors at the input to reduce conducted and radiated EMI.
- Adjusting SR FET RC snubber component values can help reduce high frequency radiated and conducted EMI.
- A pi filter comprising differential inductors and capacitors can be used after the input rectifier circuit to reduce low frequency differential EMI. A ferrite bead can be added to further improve EMI margin with minimal cost.
- A resistor across the differential inductor reduces the Q factor which can reduce EMI above 10 MHz. This may cause low frequency EMI below 5 MHz to slightly increase.
- A 1 μF ceramic capacitor connected at the output of the power supply may help reduce radiated EMI.
- A slow diode (i.e. 250 ns < t_{RR} < 500 ns) as the bias rectifier (D_{BIAS}) is generally good for conducted EMI >20 MHz and radiated EMI >30 MHz.

Thermal Management Considerations

The SOURCE pin is internally connected to the IC lead frame and provides the main path to remove heat from the device. Therefore the SOURCE pin should be connected to copper area underneath the IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, this area can be maximized for good heat sinking. Similarly, for the output SR FET, maximize the PCB area connected to the pins on the package through which heat is dissipated.

Sufficient copper area should be provided on the board to keep the IC temperature below absolute maximum limits. It is recommended that the copper area provided for the copper plane on which the SOURCE pin of the IC is soldered is sufficiently large to keep the IC temperature below 90 °C when operating the power supply at full rated load and at the lowest rated input AC supply voltage. Further de-rating can be applied depending as appropriate.

Quick Design Checklist

As with any power supply, the operation of all LYTSwitch-6 designs should be verified on the bench to make sure that component limits are not exceeded under worst-case conditions. As a minimum it is recommended that the following tests be performed:

Maximum Drain Voltage – Verify that V_{DS} of LYTSwitch-6 IC and SR FET do not exceed 90% of breakdown voltages at the highest input voltage and peak (overload) output power, both in normal operation and during start-up.

Maximum Drain Current – At maximum ambient temperature, maximum input voltage and peak output (overload) power. Review Drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up and in steady-state. Under all conditions, the maximum Drain current for the primary MOSFET should be below the absolute maximum ratings specified in the data sheet.

Thermal Check – Performed at specified maximum output power, minimum input voltage and maximum ambient temperature. Verify that temperature specification limits for LYTSwitch-6 IC, transformer, output SR FET, and output capacitors are not exceeded. Enough thermal margins should be allowed for part-to-part variation of LYTSwitch-6 primary MOSFET $R_{DS(ON)}$. Under low-line, maximum power conditions, a maximum LYTSwitch-6 SOURCE pin temperature of 110 °C is recommended to allow for this variation.

PCB Layout Recommendations

Single-Point Grounding
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pin.

Bypass Capacitors
The PRIMARY BYPASS (CBPP), SECONDARY BYPASS (CBPS) and feedback decoupling capacitors must be located directly adjacent to the PRIMARY BYPASS – SOURCE, SECONDARY BYPASS – SECONDARY GROUND and FEEDBACK – SECONDARY GROUND pins. Connections to these capacitors should be routed with short traces.

Signal Components
External components RLS, RBP, RFB(UPPER), RFB(LOWER) and RIS which are used for monitoring feedback information must be placed as close as possible to the IC pin with short traces.

Critical Loop Area
Circuits where high dv/dt or di/dt occurs should be kept as small and as compact as possible. The area of the primary loop that connects the input filter capacitor, transformer primary and IC should also be kept as small as possible. Ideally, no loop area should be placed inside another loop. This will minimize cross-talk between circuits.

Primary Clamp Circuit
A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener diode (~200 V) and diode clamp across the primary winding. To reduce EMI, minimize the loop from the clamp components to the transformer and IC.

Y Capacitor
The Y capacitor should be connected between the primary bulk capacitor negative terminal and to either terminal of the transformer secondary winding. Connection to the primary bulk positive terminal is not recommended due to the presence of the blocking diode.

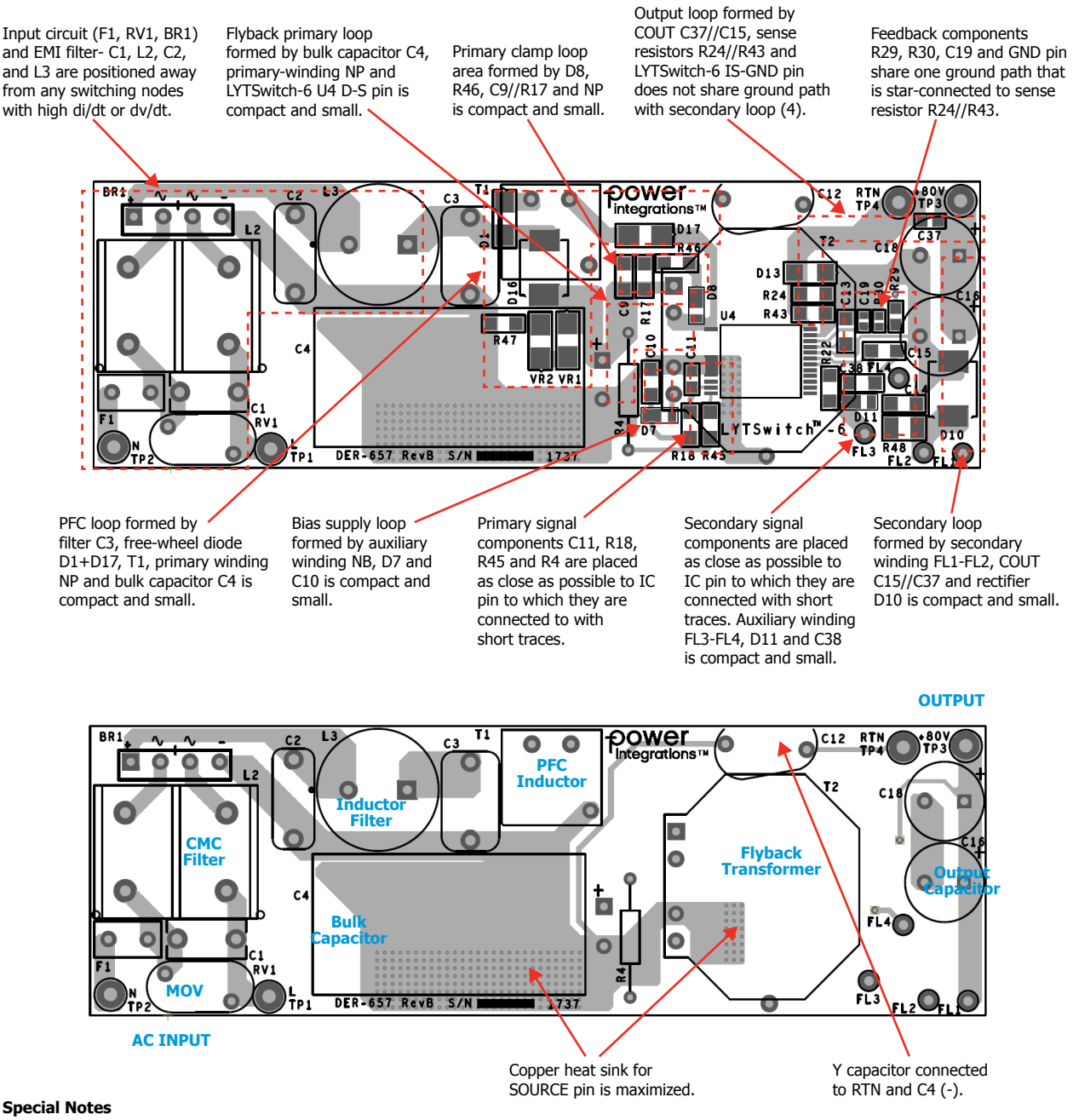
Output Rectifier Diode
For best performance, the area of the loop connecting the secondary winding, the output rectifier diode, and the output filter capacitor should be minimized. In addition, sufficient copper area should be provided at the terminals of the rectifier diode for effective heat sinking.

ESD Immunity
ESD immunity is not typically required in LED driver applications. The following recommendation, however, is for cases that have an ESD immunity requirement.

Sufficient clearance should be maintained (>8 mm) between the primary-side and secondary-side circuits to ensure compliance with ESD or hi-pot test requirements. A spark gap is best placed between output return and/or positive terminals and one of the AC inputs after the fuse. In this configuration a 6.4 mm (5.5 mm is acceptable – dependent on customer requirement) spark gap is more than sufficient to meet the creepage and clearance requirements of applicable safety standards. This can be less than the primary to secondary spacing because the voltage across spark gap does not exceed the peak of the AC input.

Drain Node
The drain switching node is the dominant noise generator. As such the components connected to the drain node should be placed close to the IC and away from sensitive feedback circuits. The clamp circuit components should be located away from the PRIMARY BYPASS pin. Trace width and length for this circuit should be minimized.

PCB Layout Example



Special Notes

- All loops are separated; no loop is inside a loop. This will avoid ground impedance noise coupling.
- Maintain trace surface area and length of high dv/dt nodes such as DRAIN, as small and short as possible to minimized RFI generation.
- No signal trace (quiet trace) such as Y capacitor and feedback return can be routed near or across noisy nodes (high dv/dt or di/dt) such as DRAIN, underneath transformer belly, switching side of any winding, or output rectifier diode to reduce capacitively magnetically coupled noise.
- No signal trace should share path with traces having an AC switching current such as output capacitor. Connection must be star-connected to the capacitor pad in order to avoid ground impedance coupled noise.

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Figure 31. TOP and BOTTOM Sides – Ideal Layout Example Showing Tight Loop Areas for Circuit with High dv/dt or di/dt, Component Placement and Spark-Gap Location in Reference to Figures 19 and 20.

Application Examples

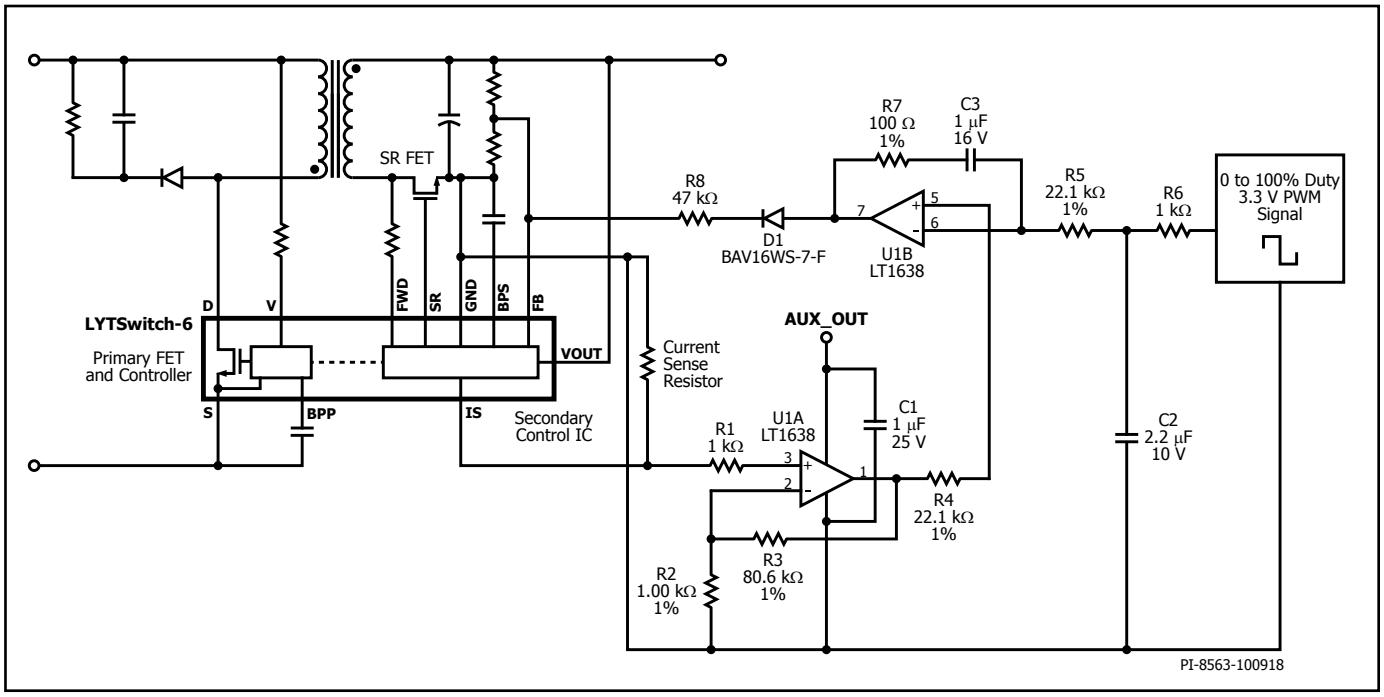

Figure 32. PWM Circuit.

PWM Dimming Circuit

Dimming is preferred by sensing the output current, amplifying the signal, comparing it with a variable reference and injecting a switcher current into the FEEDBACK (FB) pin. The circuit is limited to constant current operation such as when driving an LED load.

Output current is sensed through the IS pin which has a threshold of 35.9 mV (V_{REF}). The signal is then passed through the non-inverting amplifier circuit R1, R2, R3, U1, and C1. The gain is set by R2 and R3. The maximum voltage of the non-inverting amplifier must be limited to 90% – 95% of the maximum PWM source voltage.

$$V_{REF} \times \left(\frac{R3}{R2} + 1\right) = Derating_{FACTOR} \times VDD$$

Where
V_{REF} = IS pin reference voltage (35.9 mV)
R3 = Feedback resistor Rf of the non-inverting op-amp
R2 = Input resistor R_I of the non-inverting op-amp
VDD = Maximum output voltage of the PWM source
$Derating_{FACTOR}$ = Value between 0.9 – 0.95 of VDD

Assume a value for R2 (1 kΩ) then solve for R3:

$$R3 = R2 \times \left(\frac{Derating_{FACTOR} \times VDD - V_{REF}}{V_{REF}}\right)$$

The output of the op-amp (pin 1) connects to the positive input (pin 5) through R4. The signal going to the negative input (pin 6) comes from a PWM source (e.g, a BLE module or MCU). Resistor R6 and C2 integrate the PWM signal to create DC bias and input it to the op-amp via R5. The output (pin 7) of the error amplifier is connected to the FEEDBACK pin via D1 and R8. Resistor R7 and C3 are required for loop stability.

At full-load start-up (constant current mode), the PWM output is set to 100% to prevent the dimming circuit from injecting current into the feedback loop. Dimming will start once the rectified PWM output goes below the ($Derating_{FACTOR}$ × VDD) reference, current is injected into the feedback loop.

The feedback voltage will go up as current is injected. This will normally bring the output voltage down. However, since the LED load is a constant voltage, voltage is fixed and the output current goes down instead.

The current injection loop has to be slow enough to avoid triggering overvoltage protection when a step load from 100% to 0% is applied. This is accomplished by increasing the value of R8.

A low-input offset operational amplifier is also recommended to reduce unit-to-unit variability. It is also important to place the dimming circuit close to the IS pin and FEEDBACK pin to prevent noise from disturbing the loop.

The op-amp supply, AUX_OUT, may be tied directly to the output rail or to an auxiliary bias supply. Ensure that it does not exceed the maximum voltage rating of the op-amp.

3-in-1 Dimming Circuit

The PWM circuit shown in Figure 32 supports PWM and analog dimming. If resistor dimming and 0 – 10 V dimming compatibility are also needed, then this can be accomplished by adding R9, R10, Q2, D2, and U2 (Figure 33) which form a constant-current source. This converts a variable resistance input into an appropriate variable DC signal.

MOSFET Q1, C4, and R11 are optional components that can be added to ensure a monotonic output current rise profile during AC start-up.

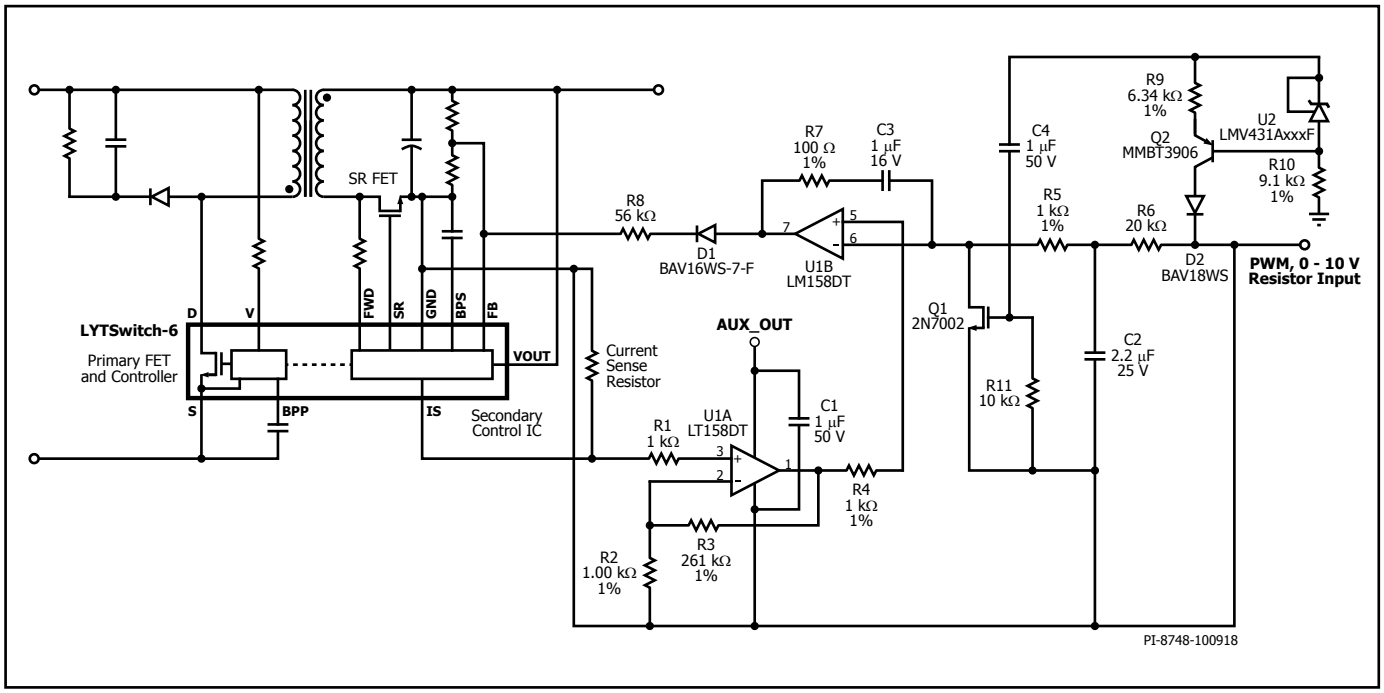

Figure 33. 3-in-1 Dimming Circuit.

Applications Design Example with SR FET

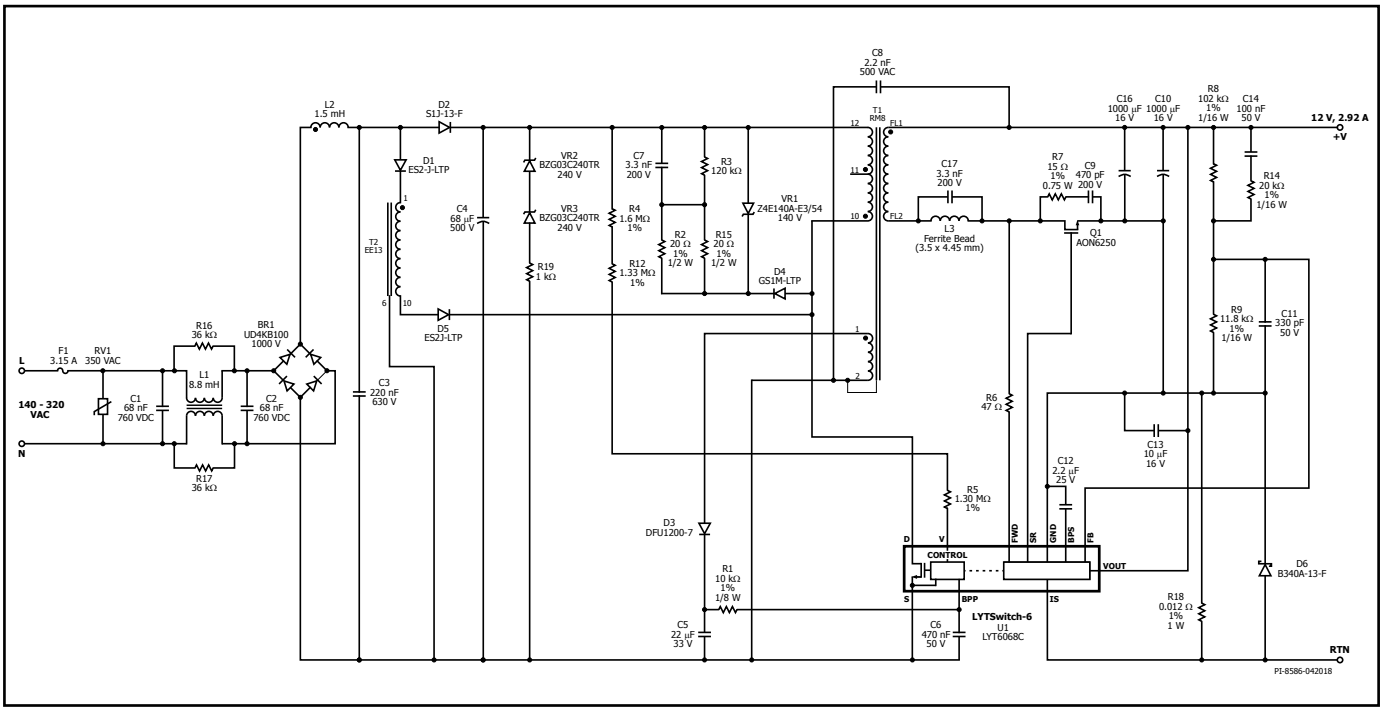

Figure 34. Schematic of DER-637, 35 W, 12 V, 2.92 A, 140 VAC – 320 VAC using LYSwitch-6 LYT6068C with Synchronous Rectification.

A High Efficiency, 35 W, 12 V Universal Power Supply LED Ballast with Synchronous Rectification

The circuit shown on Figure 34 is a 35 W isolated flyback power supply with a single-stage power factor correction circuit for LED lighting applications. It is designed to provide a constant voltage supply of 12 V with accurate voltage regulation up to 2.92 A output current. This is typically for applications where a post regulator is used for multi-LED string designs such as in RGB smart-lighting. For single-LED string applications, it provides a constant current with accurate regulation of 2.92 A from 12 V to 3 V output and prevents line induced ripple. The circuit is optimized to be highly efficient and provide accurate line and load regulation across an input voltage range of 140 to 320 VAC, with greater than 0.9 PF and achieves less than 20 % A-THD at 230 VAC.

Input Stage

Fuse F1 provides open-circuit protection which isolates the circuit from the input line in the event of catastrophic component failures. Varistor RV1 clamps any voltage spikes to a safe level to protecting the circuits connected after the fuse from damage due to overvoltage caused by a line transient or surge. Bridge diode BR1 rectifies the AC line voltage to provide a full-wave rectified DC voltage across the input filter capacitors C3 and C4. The circuit employs a 2-stage LC EMI filter comprises C1, L1, C2, L2, and C3 to suppress differential and common-mode noise generated from the PFC and flyback switching stages.

Primary Flyback Stage

The bulk capacitor C4 filters the line ripple voltage and provides energy storage to supply DC voltage to the flyback stage. One end of transformer (T1) primary winding is connected to the positive terminal of the bulk capacitor (C4) while the other side is connected to the DRAIN pin of the integrated 650 V power MOSFET of LYTSwitch-6 IC (U1). Capacitor C4 also filters differential current which reduces conducted EMI noise. A low cost RCD primary clamp comprised of D4, R2//R15 and R3//C7 limits the voltage spike caused by transformer leakage inductance which appears across the DRAIN and SOURCE pins of the internal power MOSFET in the LYTSwitch-6 IC. Clamp Zener VR1 is employed to clamp the drain voltage spike during start-up into full load at 320 VAC. The RCD primary clamp also reduces radiated and conducted EMI. The voltage across the bulk capacitor (C4) is sensed and converted into current through INPUT OVERVOLTAGE pin resistor (R4 and R12) and provides detection of a line overvoltage as well as the brown-in voltage. The overvoltage threshold (I_{OV+}) determines the input overvoltage threshold, while undervoltage brown-in threshold (I_{UV+}) determines the turn-on voltage.

The LYTSwitch-6 IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS pin capacitor (C6) when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer T1. The value of the PRIMARY BYPASS pin capacitor C6 used is 470 nF for standard current limit. Output of the auxiliary (or bias) winding is rectified using diode D3 and filtered using capacitor C5. Resistor R1 limits the current supplied to the PRIMARY BYPASS pin.

Power Factor Correction Stage

The power factor circuit comprises of inductor (T2) in series with blocking diodes (D1 and D5) which are connected to the DRAIN pin of the LYTSwitch-6 IC. High power factor correction is achieved using a Switched Valley-Fill Single Stage PFC (SVFS^{2}PFC) circuit operating in discontinuous conduction mode (DCM). The DCM switched current from inductor T2 shapes the input current into a quasi-sinusoid when the rectified voltage on C3 is less than the DC voltage on C4. This gives high power factor.

During MOSFET on-time, energy is stored in the PFC inductor (T2) and flyback transformer (T1). During MOSFET off-time, the energy

from both the PFC and flyback inductors is transferred to the secondary-side through the flyback transformer T1.

Diode D2 isolates C3 rectified AC input from C4, and also provides a current path for the charging of the bulk capacitor C4 (especially at low-line) which improves efficiency. Free-wheel diodes D1 and D5 provide a path for the energy stored in the PFC inductor to be transferred to the secondary-side during MOSFET turn-off time. Diode D1 and D5 are connected in series to withstand the voltage resonance ring from the PFC inductor when the MOSFET turns off.

During no-load or light load conditions (i.e. <10% load) the energy stored in the PFC inductor (T2) may be more than what the secondary load requires, the excess energy from the PFC inductor is recycled to the bulk capacitor C4 which boosts the voltage level. Zener-resistor clamp, VR2 and VR3 in series with R19 connected across the bulk capacitor C4 are employed to limit the voltage from rising above its safe levels. The Zener clamp voltage should be ≤500 V maximum voltage rating of bulk capacitor C4. In the event of a line voltage surge or transient, an overvoltage induced shutdown of the IC will occur.

Secondary Stage

The secondary-side control of the LYTSwitch-6 IC provides constant output voltage and constant output current. The secondary of the transformer is rectified by SR FET Q1 and filtered by the output capacitors C10 and C16. Adding a RC snubber (R7 and C9) across the SR FET reduces voltage stress across it.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage via the FORWARD pin or the output voltage via the OUTPUT VOLTAGE pin. Capacitor C13 is connected to the SECONDARY BYPASS pin of LYTSwitch-6 IC (U1) and provides decoupling for the internal circuitry.

During constant voltage operation, the output voltage regulation is achieved through sensing the output voltage via network divider resistors R8 and R9. The voltage across R9 is monitored at the FEEDBACK pin and compared to an internal reference voltage of 1.265 V to maintain accurate regulation. Bypass capacitor C11 is placed across FEEDBACK and SECONDARY GROUND pins to filter out high frequency noise that could couple to the feedback signal and cause unwanted behavior such as pulse grouping.

During constant current operation, the maximum output current is set by the sense resistor R18; to maintain constant current regulation the voltage across the sense resistor is compared to the ISENSE pins internal reference threshold of 35.9 mV. Diode D6 in parallel with the current sense resistor R18 clamps the voltage across the ISENSE and SECONDARY GROUND pins and protects from high current surge from the output capacitor during output short-circuit condition.

Applications Design Example with Auxiliary Winding and 3-in-1 DALI Dimming

Figure 35 shows the schematic of DER-740. See DER-740 for more details.

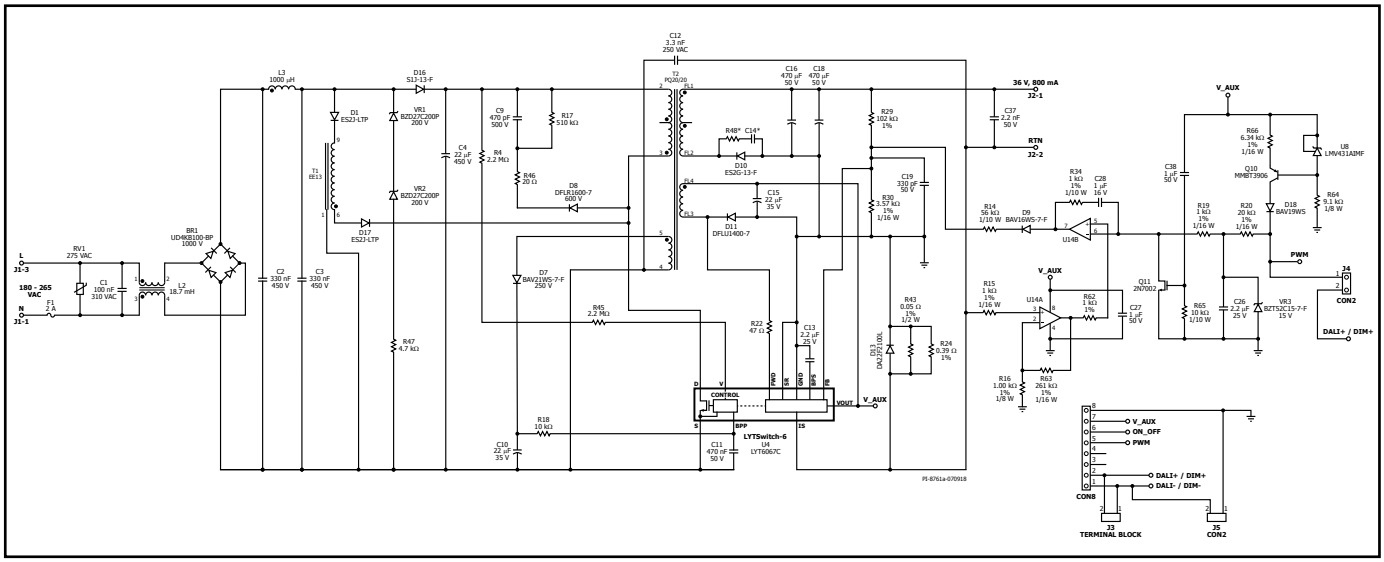

Figure 35. Schematic of DER-740.

Appendix – LYTSwitch-6 with SVFS²PFC Circuit Analysis

Overview

SVFS²PFC stands for Switched Valley-Fill, Single-Stage Power Factor Correction. The circuit is formed by placing a small capacitor C_{FILTER}, blocking diodes D_{PFC} and D_{BLOCK}, and PFC inductor L_{PFC} in front of a LYTSwitch-6 flyback circuit.

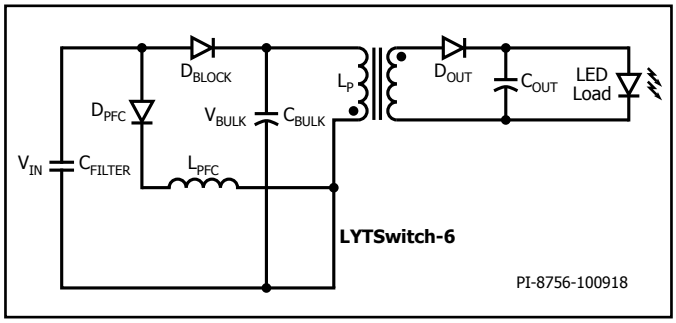

Figure 36. Simplified SVFS²PFC Schematic.

Aside from achieving >0.9 power factor, the main advantage of this circuit is the elimination of low-frequency output current ripple (Figure 37).

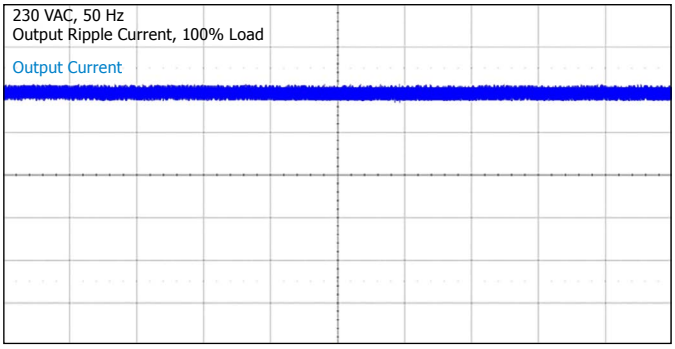

Figure 37. Output Current Ripple Profile using LYTSwitch-6 + SVFS²PFC.

SVFS²PFC Circuit Analysis

Assumptions:

- The flyback operates in DCM or CCM.
- The PFC inductor is in DCM. This mode is required to achieve good power factor.
- The rectified input voltage, V_{IN}, is near zero crossing.
- The bulk voltage capacitor is already pre-charged.

t0 to t1 – Primary FET Turns ON

PFC Current I_{PFC}

When the FET turns on, the PFC diode D_{PFC} will be forward-biased. Current will flow from the input to the PFC inductor. The PFC current will ramp-up as defined in this equation:

$$\frac{di_{PFC}}{dt_{(t0-t1)}} = \frac{V_{IN}}{L_{PFC}}$$

In DCM, the peak PFC current is given by:

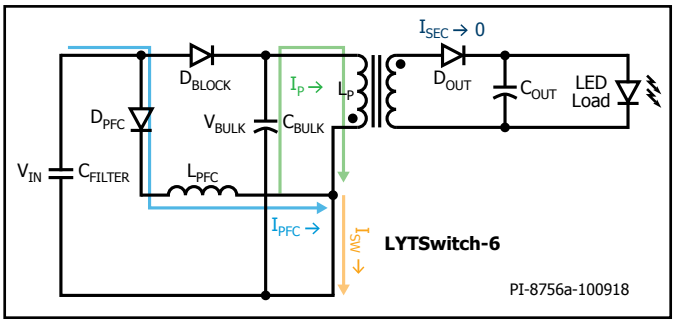

Figure 38. Current Flow from t0 to t1.

$$I_{PFC(PEAK),}\, t_0 - t_1 = \frac{V_{IN}}{L_{PFC}} \times t_{ON}$$

Primary Winding Current I_p

The primary transformer current slope is given by:

$$\frac{di_P}{dt_{(t0-t1)}} = \frac{V_{BULK}}{L_P}$$

The peak primary winding current IP is

$$I_{P(PEAK),}\, t_0 - t_1 = \frac{V_{BULK}}{L_P} \times t_{ON}$$

LYTSwitch-6 Switch Current I_{SW}

The switch current I_{SW} is the sum of current from the PFC inductor I_{PFC}, and the current from the transformer winding I_P.

$$I_{SW(t0-t1)} = I_{PFC} + I_P$$

The contribution of the PFC current is smaller than that of the flyback because the rectified input V_{IN} is very low at this point.

As V_{IN} increases, the PFC current will increase while the flyback current will decrease.

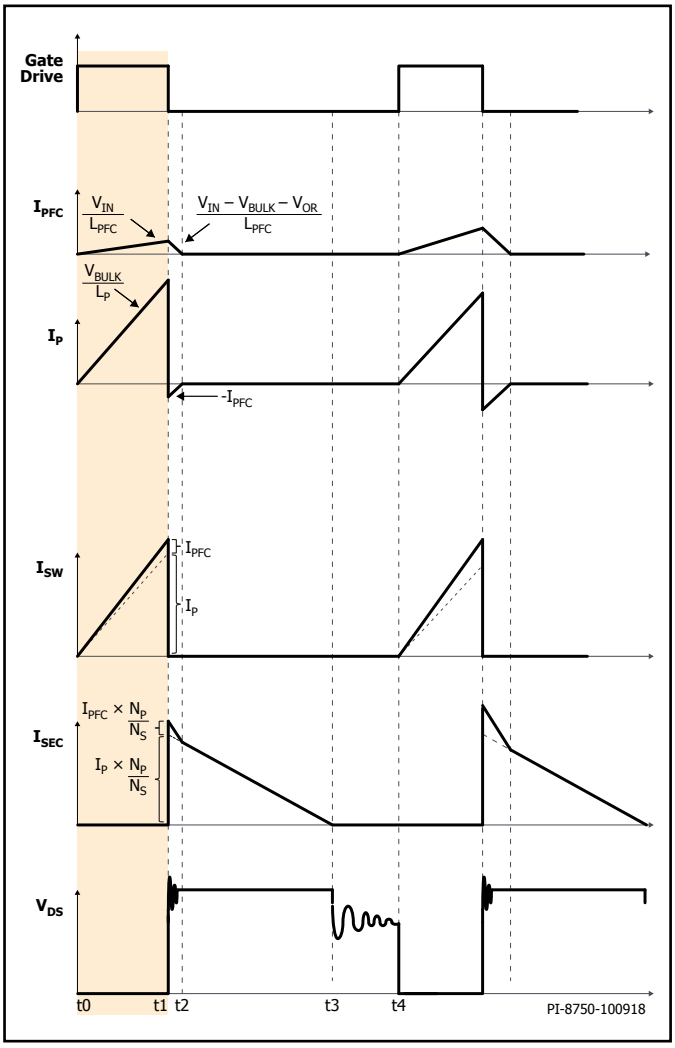

Figure 39. SVFS²PFC Timing Diagram, t0 to t1.

t1 to t2 – Primary FET Turns OFF

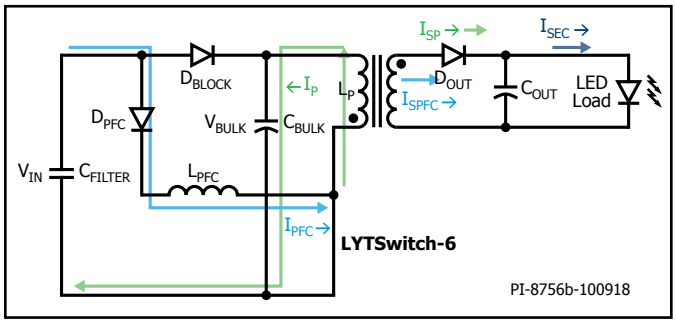

Figure 40. Current Flow from t1 to t2.

PFC Current I_{PFC}

When the FET turns off, the energy stored in the PFC is transferred to the secondary through the flyback transformer. At the same time, the current will flow through the transformer winding onto bulk capacitor.

The slope of the PFC current going to the primary winding is defined by

$$\frac{di_{PFC}}{dt_{(t1-t2)}} = \frac{V_{IN} - V_{BULK} - V_{OR}}{L_{PFC}}$$

Referred to the secondary, I_{SPFC} is

$$I_{SPFC(T1-T2)} = \frac{N_P}{N_S} \times I_{PFC}$$

Primary Winding Current I_p

Unlike flyback, current will flow back from the flyback transformer winding to the bulk capacitor. The current is negative since it is going in the opposite direction and is equal to the PFC current.

Secondary Diode Current I_{SEC}

The secondary diode will be forward-biased and will supply the current to the LED load. The diode current contains current from both the stored energy in the flyback transformer and energy from the PFC inductor. If the rectified input voltage is low, the secondary diode current mainly comes from the flyback transformer. As the rectified input voltage goes up, the contribution of the PFC current will go up while the contribution of the flyback transformer will go down.

$$I_{SEC(t1-t2)} = \frac{N_P}{N_S} \times (I_{PFC} + I_P)$$

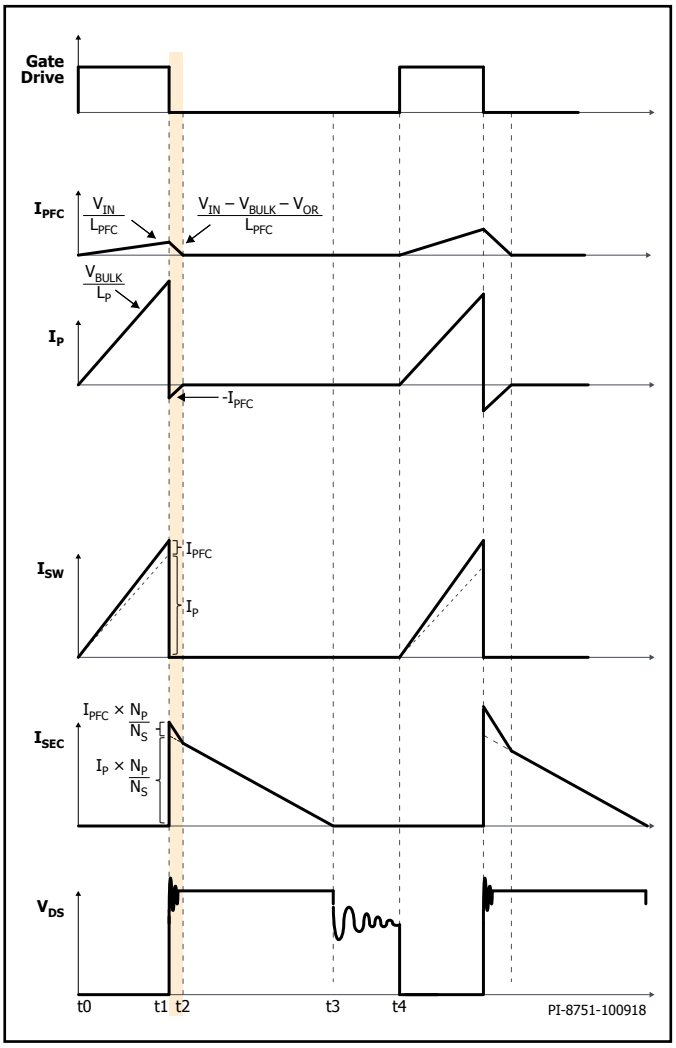

Figure 41. SVFS²PFC Timing Diagram, t1 to t2.

t2 to t3 – PFC Energy Completely Discharged

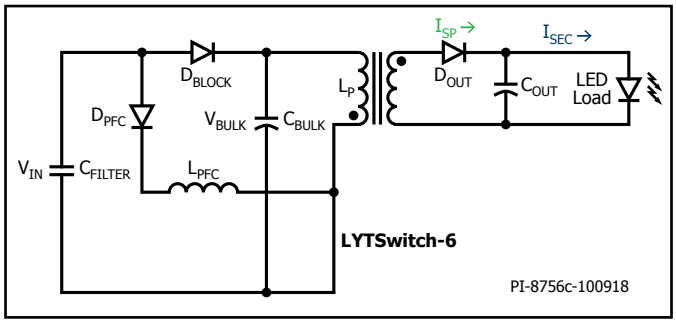

Figure 42. Current Flow from t2 to t3.

PFC Current I_{PFC}
The PFC inductor is designed to work in DCM. At time = t2, the stored energy on the PFC inductor has been depleted.

Primary Winding Current I_P
No more current will flow through the primary winding.

Secondary Diode Current I_{SEC}
The diode current contains current from the stored energy in the flyback transformer only.

$$I_{SEC(t2-t3)} = \frac{N_P}{N_S} \times I_P$$

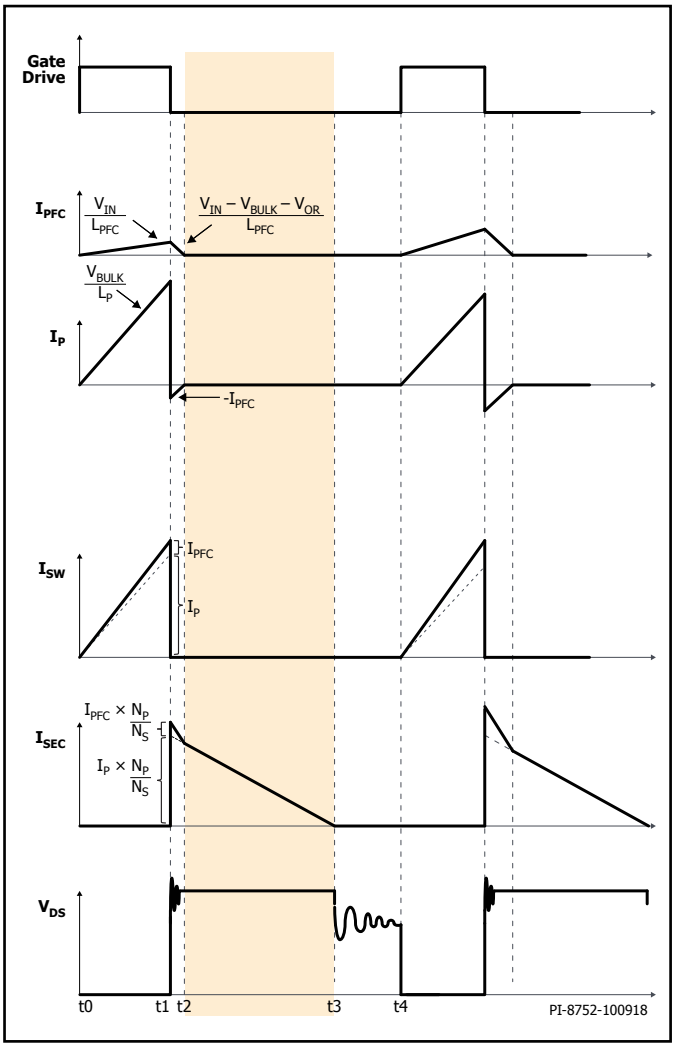

Figure 43. SVFS²PFC Timing Diagram, t2 to t3.

t3 to t4 – PFC Energy Completely Discharged

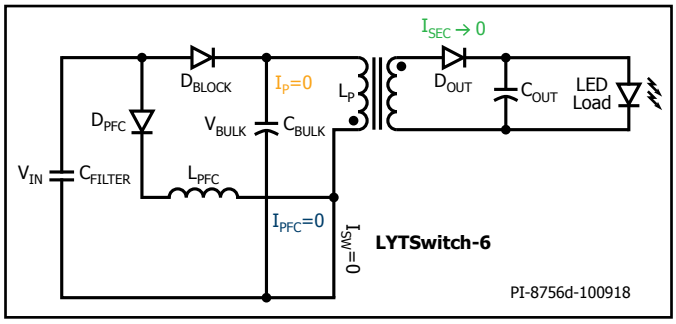

Figure 44. No Current Flow from t3 to t4.

The time from t3 to t4 only occurs if the device is operating in discontinuous conduction mode (DCM).

Changes in the Next Switching Cycle

In the next switching cycle, the rectified input voltage V_{IN} is higher. Looking at the equation for the PFC inductor, the peak PFC current will also be higher, while the primary winding current will be lower.

Consolidated Waveforms in One Line Cycle

In summary,

- The PFC current IPFC follows the shape of the input line.
- The primary winding current is maximum at the zero-crossing and lowest at 90º phase angle.
- The Drain current is lowest at the zero-crossing and increases with line.
- The switching frequency is lowest at the zero-crossing and increases with line.

How PF is Achieved?

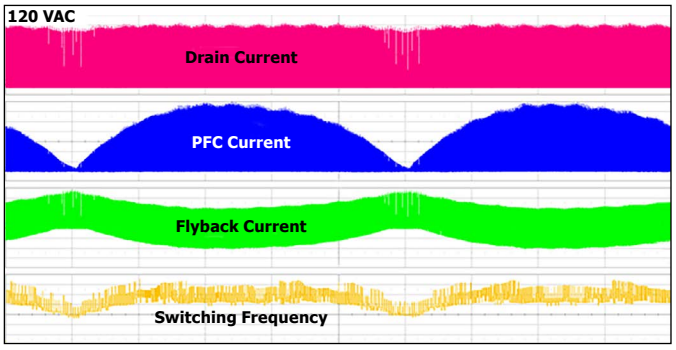

Figure 45. Current Waveforms, 1 Line Cycle.

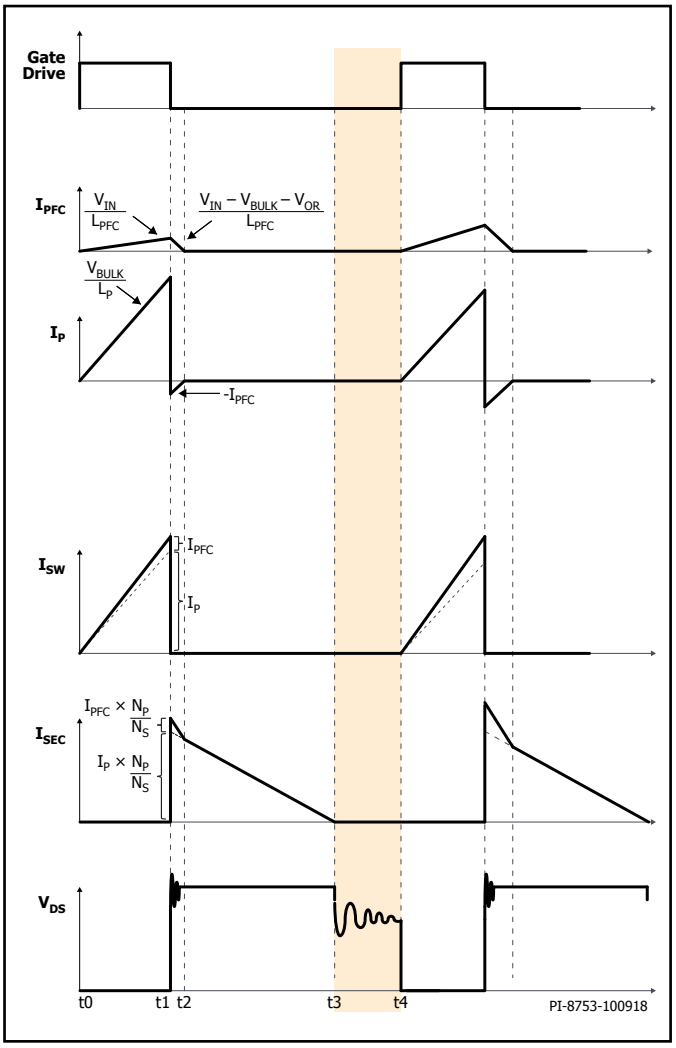

Figure 46. SVFS²PFC Timing Diagram, t3 to t4.

Looking at Figure 47, the input current is the sum of the PFC current I_{PFC} and I_{DBLOCK}, which is the current whenever the bulk capacitor draws current from the input. This relationship forms the basis of the term switched-valley-fill; i.e. the PFC circuit fills the "valley" whenever the bulk capacitor is not drawing current from the input.

Figure 48 shows the typical input current waveform on a non-PF flyback converter. Here, the bulk capacitor supplies the power to the circuit. The only time the converter draws current from the input is when the bulk voltage drops below the input voltage. Typical conduction period is 3 ms.

With SVFS²PFC circuit, the PFC circuit creates a pseudo-sinusoidal input current that dramatically increases the power factor (Figure 49).

As a bonus, the PF and THD at higher input line are even better (Figure 50). This is because the PFC circuit also refills the energy in the bulk capacitor every switching cycle. At high-line, if the energy that the PFC circuit provides the bulk capacitor is greater than the energy that the converter draws, then this results to the boosting of the bulk voltage. Some designs can boost the bulk voltage such that it is always higher than the input (Figure 51). This means that the input current is completely dependent on the PFC current which follows the input voltage, resulting in higher power factor.

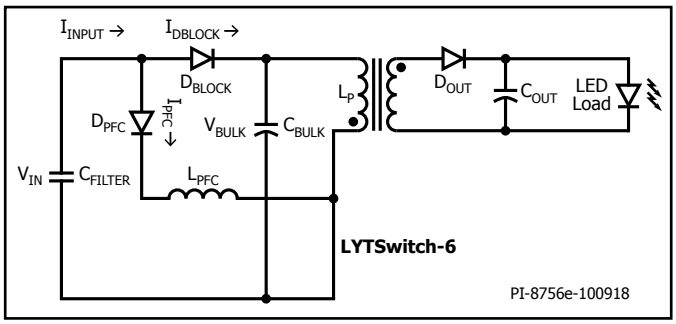

Figure 47. Input Current Flow, SVFS²PFC.

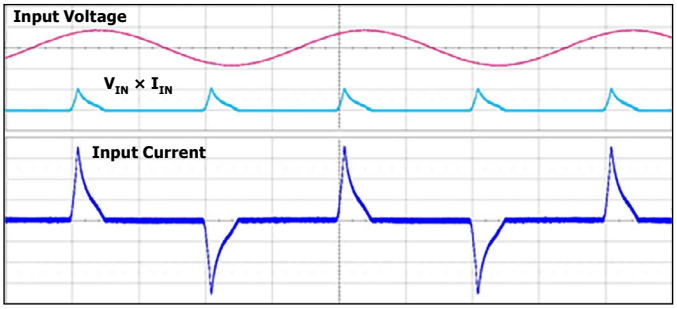

Figure 48. Input Current Waveform, Typical Non-PF Flyback, 120 VAC.

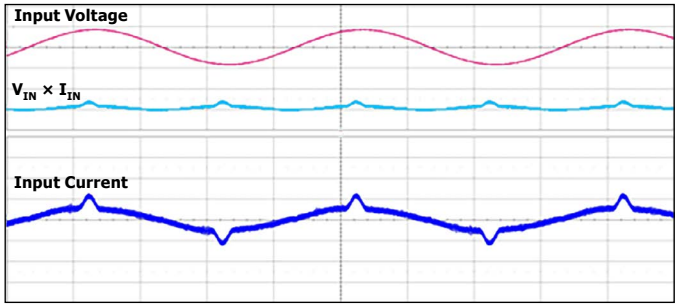

Figure 49. Input Current Waveform, SVFS²PFC + LYTSwitch-6 Flyback, 120 VAC

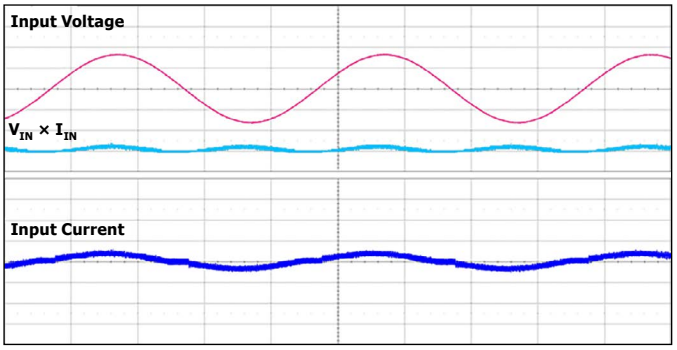

Figure 50. Input Current Waveform, SVFS²PFC + LYTSwitch-6 Flyback, 230 VAC.

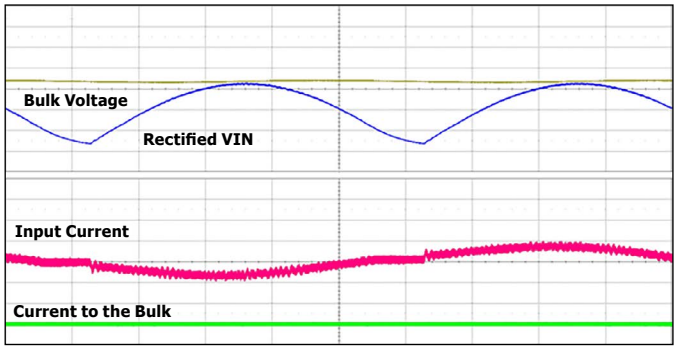

Figure 51. Bulk Voltage Waveform, SVFS²PFC + LYTSwitch-6 Flyback, 230 VAC.

Revision	Notes	Date
A	Initial release.	10/18
B	Updated Figure 2 on page 2.	01/19

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