LinkSwitch-XT2SR Family

High-Efficiency Off-line CV Flyback Switcher IC with Integrated 725 V / 900 V Primary MOSFET, Low No-Load, and Synchronous Rectification

Product Highlights

Ideal for Non-Isolated Applications

- Low component count switcher solution with SR driver and integrated 3.3 V LDO (uVCC)
- High-efficiency across load range
- Accurate CV independent of transformer design or external components
- Default 5 V output with no external feedback components
- Adjustable VOUT using optional FEEDBACK pin
- Simple two winding transformer
- Compact package reduces PCB area

EcoSmart™ – Energy-Efficient

- Less than 5 mW no-load at 230 VAC
- Enables designs that easily meet global energy efficiency regulations
- Achieves up to 90% full load efficiency with 5 V output

Advanced Protection / Safety Features

- Hysteretic thermal shutdown (OTP)
- Output OV protection with VOUT pin
- Extended creepage between DRAIN pin and all other pins increases field reliability
- 725 V MOSFET rating series for excellent surge withstand
  - 900 V switch rating for industrial applications and extra safety margin
- Extremely low component count enhances reliability
- Allows use of single-sided PCB and full SMD manufacturability

Green Package

- Halogen free and RoHS compliant

Applications

- Single and multi-output power supplies in appliances, home and business automation, and industrial systems

Description

The LinkSwitch-XT2SR family dramatically increases the efficiency of auxiliary power supplies used in appliances, consumer products and industrial applications. Ideal for non-isolated designs with a high current, 5 V output, this advanced flyback controller can achieve >90% full load efficiency. High efficiency is maintained over to load range, with >85% efficiency at 100 mW load. No-load consumption is <5 mW. The default 5 V main output can be adjusted via optional external feedback resistors.

Power for start-up and normal operation is supplied from the DRAIN and VOUT pins, eliminating the need for a bias winding and associated circuitry.

The SO-16 package and a low number of external components make the LinkSwitch-XT2SR ICs ideal for compact designs.

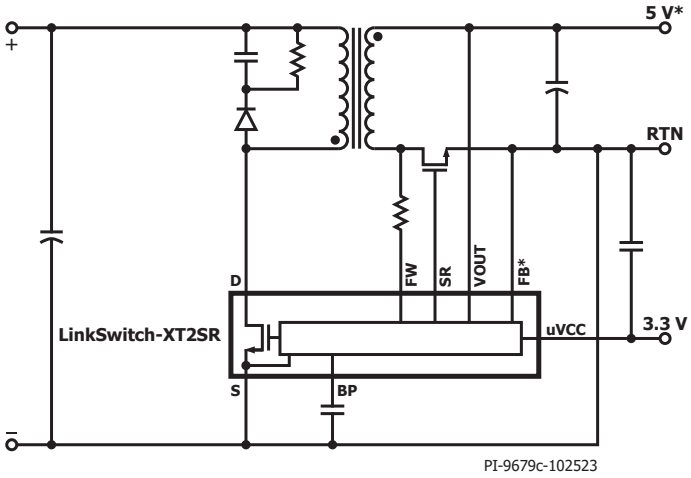


Figure 1. Typical Application Schematic with LinkSwitch-XT2SR IC.
*Adjustable with optional external feedback resistors (see Figure 8).

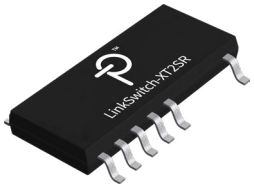


Figure 2. Compact SO-16B (D Package).

Maximum Output Power Table

Product	Open Frame[1,2]	
725 V MOSFET	230 VAC	85-265 VAC
LNK3771D	7 W	6 W
LNK3772D	12 W	10 W
LNK3773D	15 W	12 W
900 V Switch	230 VAC	85-484 VAC
LNK3792D	12 W	10 W

Table 1. Output Power Table.

Notes:
1. Minimum peak power capability.
2. Maximum output power is dependent on the design. Limit package temperature to <125 ºC.

Pin Functional Description

FEEDBACK (FB) Pin (Pin 1)
(Optional pin) Connection to an external resistor divider network to set the output voltage. Shorted to ground on application board when using internal resistor divider network for default 5 V.

OUTPUT VOLTAGE (VOUT) Pin (Pin 2)
Connected directly to the output voltage providing current for the controller.

SR (SR) Pin (Pin 3)
Gate driver for external SR FET. Note that the SR pin should be used to drive SR FET, and cannot be shorted to ground or left floating.

FORWARD (FW) Pin (Pin 4)
Connection point to the switching node of the transformer output winding to provide sense for SR drive control.

SOURCE (S) Pin (Pin 5)
SOURCE pin that must be connected to the ground.

DRAIN (D) Pin (Pin 8)
Power switch drain connection.

SOURCE (S) Pin (Pins 9-14)
Grouped together to provide a better thermal path.

EXTERNAL SUPPLY (uVCC) Pin (Pin 15)
3.3 V supply for an external controller.

POWER BYPASS (BP) Pin (Pin 16)
Connection point for an external bypass capacitor for the IC supply.

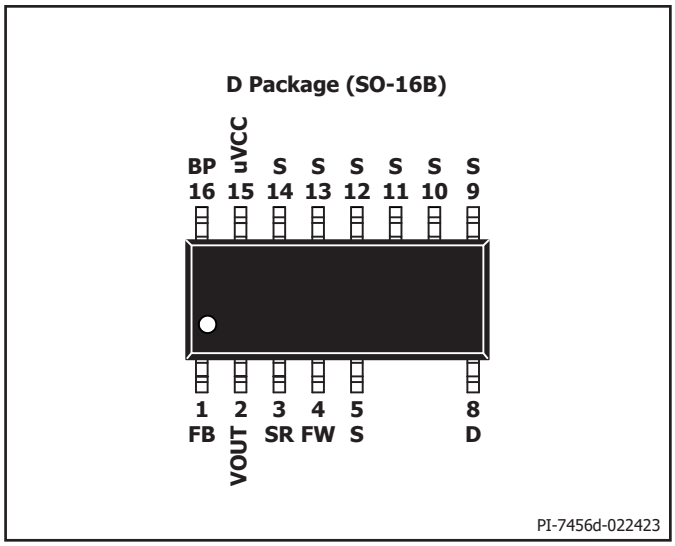


Figure 3. Pin Configuration.

Application Example

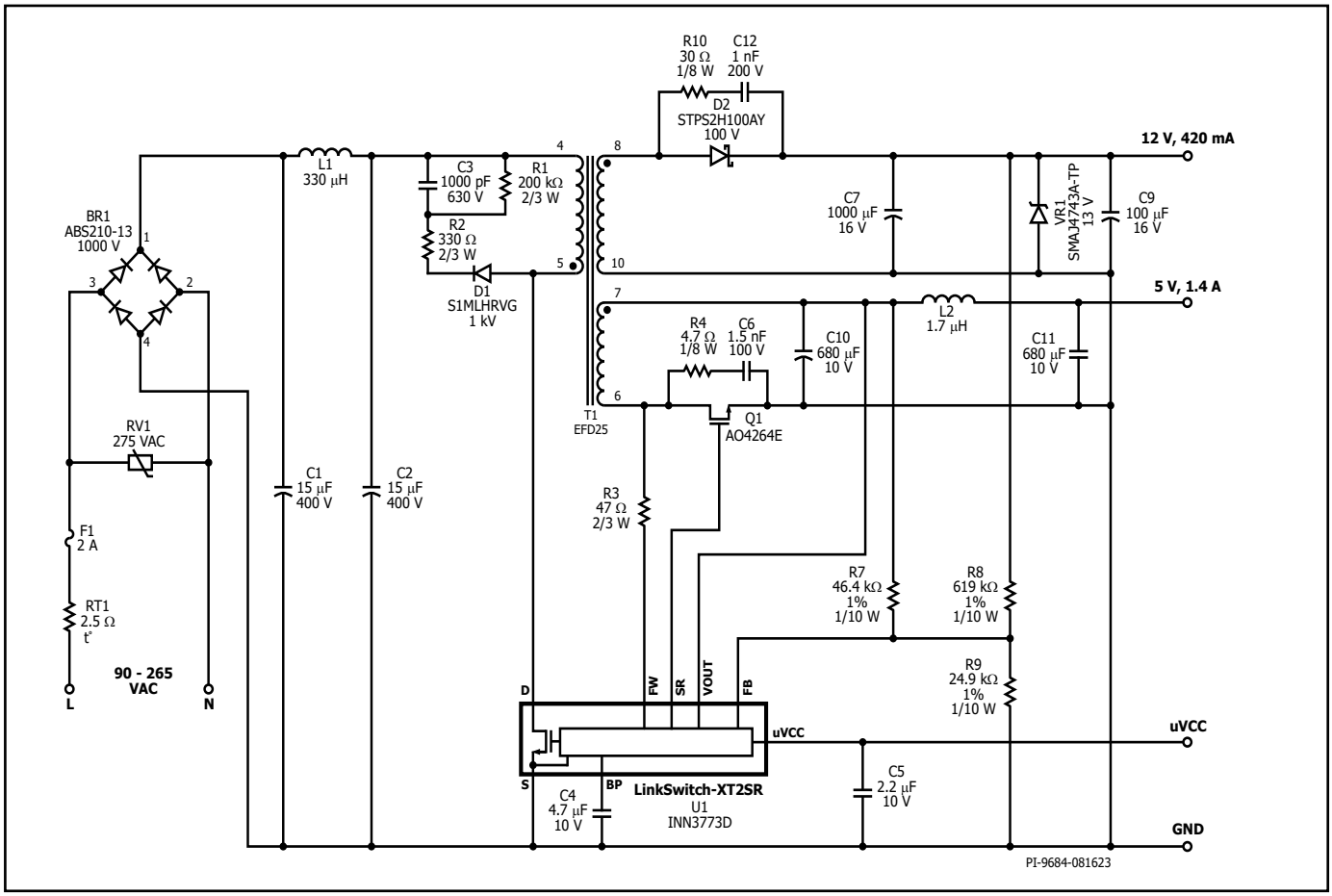


Figure 4. Schematic for Non-Isolated Dual Output 5 V, 1.4 A and 12 V, 0.42 A (12 W) Design.

A 5 V, 1.4 A and 12 V, 0.42 A (12 W) Design

The schematic shown in Figure 4 is a typical implementation of a non-isolated dual output, 5 V, 1.4 A and 12 V, 0.42 A power supply for appliance using the LNK3773D IC. Using the optional external feedback pin for the dual output PSU results in a highly efficient design that meets typical cross regulation requirements without the need for a post regulator. This circuit makes the use of synchronous rectifier section on the 5 V output to improve efficiency.

The EcoSmart features built into the LinkSwitch-XT2SR family allow this design to easily meet all current and proposed energy efficiency standards, including the mandatory California Energy Commission (CEC) requirement for average operating efficiency. It is also possible to achieve zero input power for no load operation with less than 5 mW input power at 230 VAC input (per IEC62301:2011).

Fuse F1 isolates the circuit and provides protection against excess input current resulting from catastrophic failure of any of the components in the power supply. The Bridge rectifier BR1 rectifies the AC line voltage and capacitors C1 and C2 filter the rectified AC input with inductor L1, which forms a pi-filter to attenuate differential mode EMI. Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply. One side of the transformer primary winding is connected to the rectified DC bus, the other is connected to the integrated 725 V power MOSFET inside the LinkSwitch-XT2SR IC (U1).

A cost efficient R2CD clamp circuit formed by D1, R1, R2, and C3 limits the peak drain voltage at the instant of turn-off of the switch inside U1. The clamp circuit helps to dissipate the energy stored in the leakage inductance of transformer T1 and output traces.

The LinkSwitch-XT2SR IC is self-starting, using an internal high-voltage current source to charge the BP pin capacitor, C4 when AC is first applied. During normal operation the BP regulator is powered from VOUT. The minimum drain voltage at startup before the IC starts switching is 50 VDC, and VOUT will be used to charge BP when VOUT voltage reaches 0.2 V higher than the BP pin voltage.

The controller of the LinkSwitch-XT2SR IC provides output voltage sensing and drives to a switch providing synchronous rectification. The 5 V output of the transformer is rectified by SR FET Q1 and filtered by C10, L2, and C11. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RC snubber, R4 and C6.

The 12 V output from the transformer is rectified by Schottky diode D2 and filtered by C7 and C9. High frequency ringing during switching transients are reduced via a RC snubber, R10 and C12.

Synchronous rectification (SR) is provided by switch Q1. Switch Q1 is turned on by the controller inside IC U1, based on the winding voltage sensed via resistor R3 and current fed into FORWARD pin of the IC.

In continuous conduction mode operation, the SR FET is turned off just prior to the controller initiating a new switching cycle. In discontinuous mode the SR FET is turned off when the voltage drop across the MOSFET falls below a threshold ($V_{SR(TH)}$). The controller ensures that the primary switching MOSFET and the synchronous rectification MOSFET are never on simultaneously.

Resistor R7, R8 and R9 form an external voltage divider network that senses the output voltage from both outputs for better cross-regulation. Zener diode VR1 improves the cross regulation when only the 5 V output is loaded, which results in the 12 V output operating at the higher end of its voltage range. The LinkSwitch-XT2SR IC has an internal reference of 2.0 V, and the unit enters auto-restart when VOUT pin voltage goes higher than 6 V.

There is a 3.3 V uVCC output with C5 decoupling capacitor, see current capability Figure 21.

Key Application Considerations

Output Power Table

The data sheet output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following conditions:

1. The minimum DC input voltage is 90 VDC or higher for 85 VAC input, 220 VDC or higher for 230 VAC input or 115 VAC with a voltage-doubler. Input capacitor voltage should be sized to meet these criteria for AC input designs.
2. Efficiency assumption is >85 %.
3. Transformer primary inductance tolerance of ±10%.
4. Reflected output voltage (VOR) is set to maintain K_P = 0.9 at minimum input voltage for universal line and K_P = 1 for high input line designs.
5. Maximum conduction losses for open frame designs = 1.0 W.
6. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink to keep the SOURCE pin temperature at or below 125 °C.
7. Ambient temperature of 40 °C for open frame designs.
8. Below a value of 1, K_P is the ratio of ripple to peak primary current. To prevent reduced power delivery, due to premature termination of switching cycles, a transient K_P limit of ≥0.25 is recommended. This prevents the initial current limit (I_{INT}) from being exceeded at Switch turn-on.

Reducing No-Load and Standby Consumption

The LinkSwitch-XT2SR IC starts in self-powered mode, drawing energy from the BYPASS pin capacitor charged through an internal current source. The required BP supply current for the device is low. It is easier to achieve zero input power for no load operation with LinkSwitch-XT2SR. Optimization of external components such as the input capacitor, primary snubber, and power transformer will further reduce no load input power. For dual output application, the standby input power with 30 mA load on the 5 V output will be less than 200 mW.

Selection of Components

Components for LinkSwitch-XT2SR Primary-Side Circuit

BP Capacitor

A capacitor connected from the BYPASS pin of the LinkSwitch-XT2SR IC to Source provides decoupling for both primary and secondary controller. A 4.7 µF capacitor needs to be used. Though electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use on double sided boards as they enable placement of capacitors close to the IC. Their small size also makes it ideal for compact power supplies. At least 10 V, 0805 or larger size rated X5R or X7R dielectric capacitors are recommended to ensure that minimum capacitance requirements are met. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 5 V. Do not use Y5U or Z5U / 0603 rated MLCC due to this type of SMD ceramic capacitor has very poor voltage and temperature coefficient characteristics.

Primary-Side Snubber Clamp

A snubber circuit should be used on the primary-side as shown in Figure 4. This prevents excess voltage spikes at the drain of the Switch at the instant of turn-off of the Switch during each switching cycle though conventional R2CD clamps can be used. RCDZ clamps offer the highest efficiency. The circuit example shown in Figure 4 uses an R2CD clamp with a resistor in series with the clamp diode. This resistor dampens the ringing at the drain and also limits the reverse current through the clamp diode during reverse recovery. Standard recovery glass passivated diodes with low junction capacitance are recommended as these enable partial energy recovery from the clamp thereby improving efficiency.

Audible Noise

The cycle skipping mode of operation used in LinkSwitch-XT2SR ICs can generate audio frequency components in the transformer. To limit this audible noise generation, the transformer should be designed such that the peak core flux density is below 3000 gauss (300 mT). Following this guideline and using the standard transformer production technique of dip varnishing practically eliminates audible noise. Vacuum impregnation of the transformer should not be used due to the high primary capacitance and increased losses that result. Higher flux densities are possible, however careful evaluation of the audible noise performance should be made using production transformer samples before approving the design.

Ceramic capacitors that use dielectrics, such as Z5U, when used in clamp circuits may also generate audio noise. If this is the case, try replacing them with a capacitor having a different dielectric or construction, for example a film type.

Components for LinkSwitch-XT2SR Secondary-Side Circuit

FORWARD Pin Resistor

A 47 ohms, 5% resistor is recommended. A higher or lower resistor value should not be used as it can affect device operation such as the timing of the synchronous rectifier drive. Figure 5 and Figure 6 below show examples of unacceptable and acceptable FORWARD pin voltage waveforms.

VD is forward voltage drop across the SR.

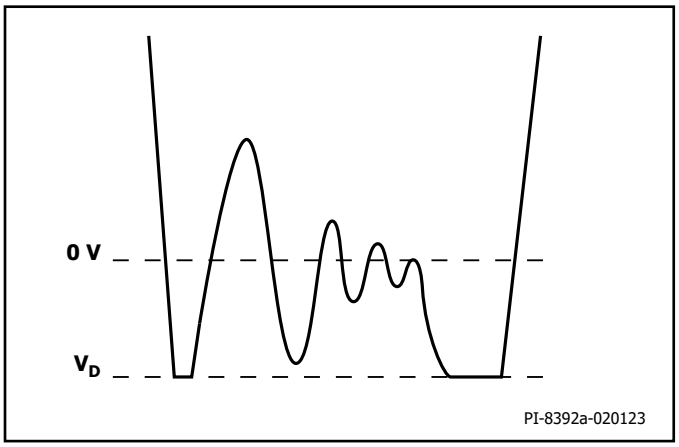


Figure 5. Unacceptable FORWARD Pin Waveform.

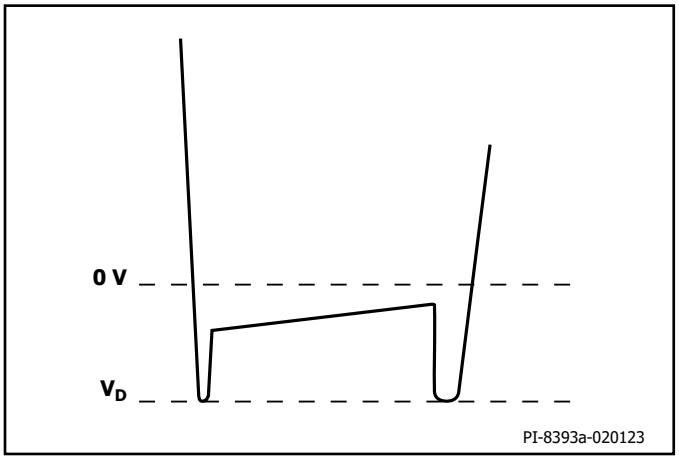


Figure 6. Acceptable FORWARD Pin Waveform.

SR Switch Operation and Selection

Although a simple diode rectifier and filter works for the output, use of an SR FET enables the significant improvement in operating efficiency often necessary to meet the European CoC and the U.S. DoE energy efficiency requirements. The controller turns on the SR FET once the flyback cycle begins. The SR FET gate should be tied directly to the SYNCHRONOUS RECTIFIER DRIVE pin of the LinkSwitch-XT2SR IC (no additional resistors should be connected in the gate circuit of the SR FET). A FET with 13.5 mΩ $R_{DS(ON)}$ is appropriate for a 5 V, 1.4 A output, and a Schottky diode is suitable for designs rated with a 12 V, 0.42 A output. The SR FET driver uses the BYPASS pin for its supply rail, and this voltage is typically 4.4 V. A FET with a gate high threshold voltage is therefore not suitable; FETs with a gate threshold voltage of 1.5 V to 2.5 V are ideal. There is a slight delay between the commencement of the flyback cycle and the turn-on of the SR FET. During this time, the body diode of the SR FET conducts. Once the LinkSwitch-XT2SR IC detects end of the flyback cycle, voltage across SR FET $R_{DS(ON)}$ reaches 0 V, any remaining portion of the flyback cycle is completed with the current commutating to the body diode of the SR FET.

The voltage rating of the Schottky diode and the SR FET should be at least 1.4 times the expected peak inverse voltage (PIV) based on the turns ratio used for the transformer. 60 V rated FETs and diodes are suitable for most 5 V designs, and 100 V rated Schottky diodes are suitable for 12 V designs.

The interaction between the leakage reactance of the output windings and the SR FET capacitance (C_{OSS}) leads to ringing on the voltage waveform at the instance of voltage reversal at the winding due to primary switch turn-on. This ringing can be suppressed using an RC snubber connected across the SR FET. A snubber resistor in the range of 10 Ω to 47 Ω may be used (higher resistance values lead to noticeable drop in efficiency). A capacitance value of 1 nF to 2.2 nF is adequate for most designs.

For single output design, SR FET is a default rectifier for LinkSwitch-XT2SR, Schottky diode is not allowed. But for dual output design, the SR FET should be used for the rectifier of the higher load output to maximize efficiency. A Schottky diode needs to be used for the rectifier of the lower load output to prevent any negative current flowing. After output rectifiers are selected, V_{OUT} and FWD pins should be connected to the SR FET winding as shown in the following diagram.

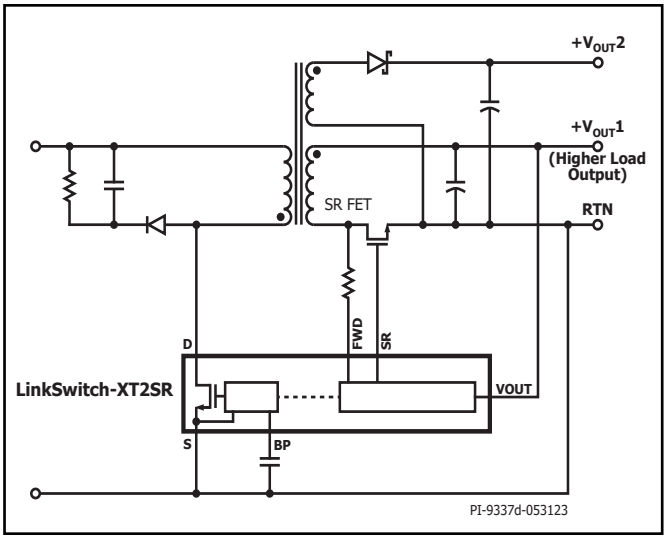


Figure 7. Recommended Dual Output Circuit using LinkSwitch-XT2SR.

Output Capacitor

Low ESR aluminum electrolytic capacitors are suitable for use with most high frequency flyback switching power supplies, though the use of aluminum-polymer solid capacitors have gained considerable popularity due to their compact size, stable temperature characteristics, extremely low ESR and high RMS ripple current rating.

Typically, 300 µF to 500 µF of Low ESR aluminum electrolytic capacitance per ampere of output current is adequate. The other factor that influences choice of the capacitance is the output ripple. Ensure that capacitors with a voltage rating higher than the highest output voltage plus sufficient margin be used.

Built in Output Voltage Feedback Circuit
The FB pin voltage is 2.0 V, and FB pin should be shorted to ground when using internal built in divider used for single output voltage.

For external feedback, resistors RH and RL can be selected as follows:

$$V_{OUT} = \frac{V_{FB} \times (R_H + R_L)}{R_L}, \text{ where } V_{FB} = 2.0\ V$$

Let R_H = 130 kΩ, R_L = 64.9 kΩ, then V_{OUT} = 6 V.

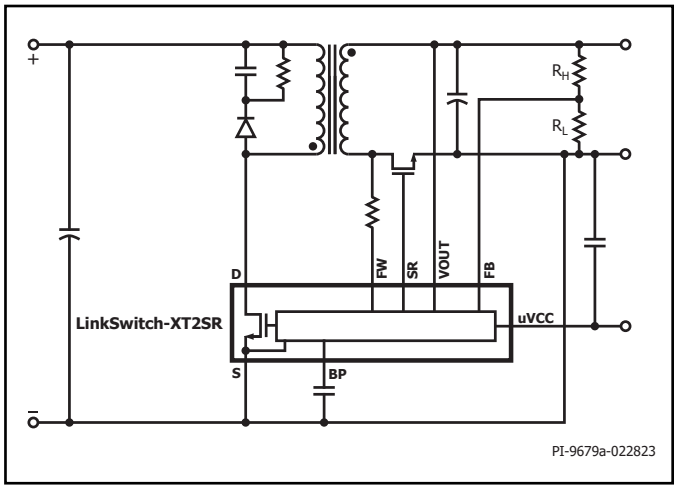


Figure 8. Typical Application with LinkSwitch-XT2SR with External Feedback Resistors for Non 5 V Design.

Recommendations for Circuit Board Layout

See Figure 9 for a recommended circuit board layout for a LinkSwitch-XT2SR based power supply.

Single-Point Grounding
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitors
The BYPASS pin capacitor must be located adjacent to the BYPASS-SOURCE pins respectively and connections to this capacitor should be routed with short traces.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and IC should be kept as small as possible.

Primary Clamp Circuit
A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener diode (~200 V) and diode clamp across the primary winding. To reduce EMI, minimize the loop from the clamp components to the transformer and IC.

Thermal Considerations
The SOURCE pin is internally connected to the IC lead frame and provides the main path to remove heat from the device. Therefore, the SOURCE pin should be connected to a copper area underneath the IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, it can be maximized for good heat sinking without compromising EMI performance. Similarly for the output SR Switch, maximize the PCB area connected to the pins on the package through which heat is dissipated from the SR Switch.

Sufficient copper area should be provided on the board to keep the IC temperature safely below the absolute maximum limits. It is recommended that the copper area provided for the copper plane on which the SOURCE pin of the IC is soldered is sufficiently large to keep the IC temperature below 110 °C when operating the power supply at full rated load and at the lowest rated input AC supply voltage.

Output SR Switch
For best performance, the area of the loop connecting the secondary winding, the output SR Switch and the output filter capacitor, should be minimized.

Drain Node
The drain switching node is the dominant noise generator. As such the components connected the drain node should be placed close to the IC and away from sensitive feedback circuits. The clamp circuit components should be located physically away from the PRIMARY BYPASS pin and trace lengths minimized. The loop area of the loop comprising of the input rectifier filter capacitor, the primary winding and the IC primary-side Switch should be kept as small as possible.

Layout Example Layout

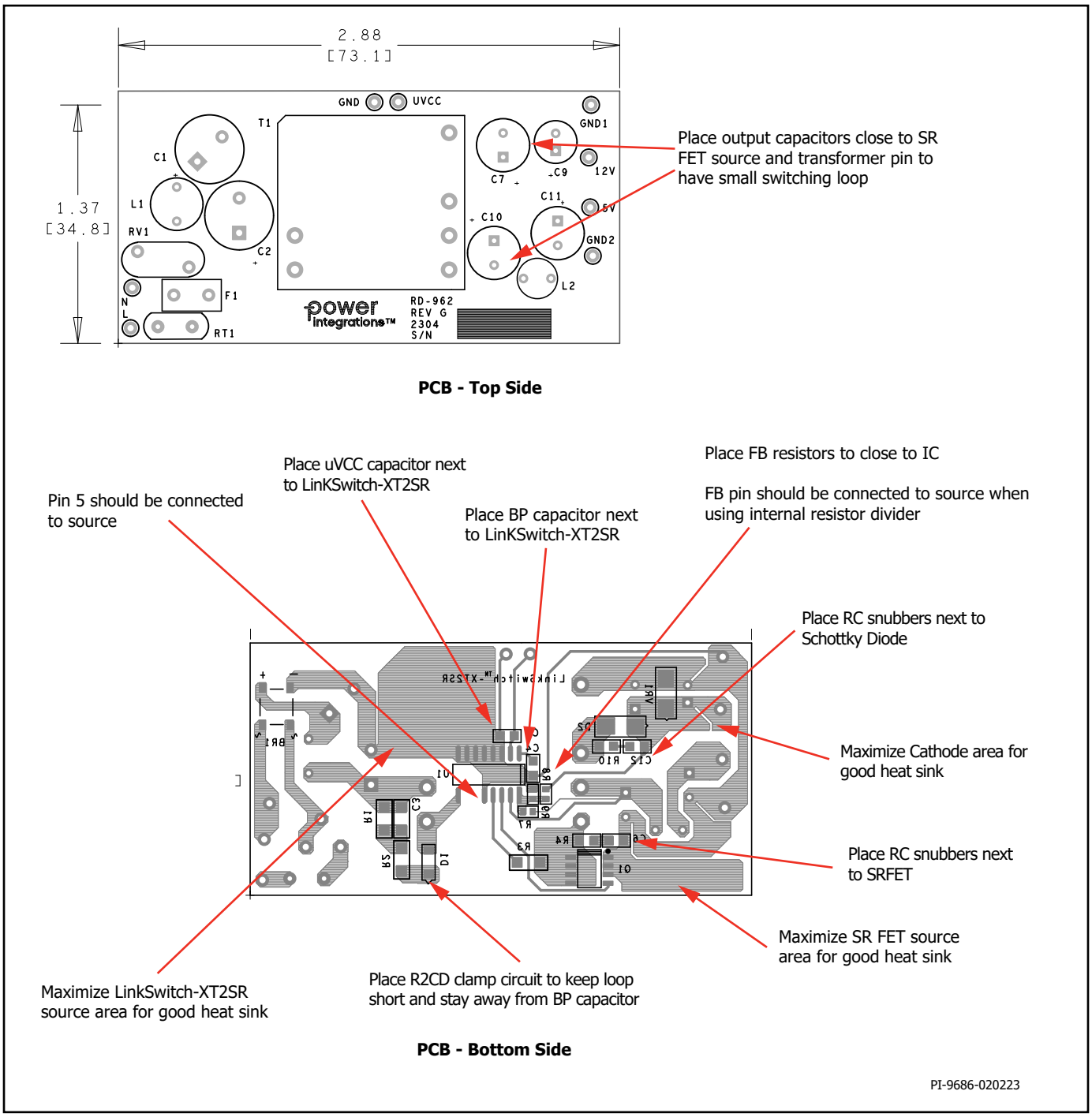


Figure 9. Layout Example.

Recommendations for EMI Reduction

1. Appropriate component placement and small loop areas of the primary and secondary power circuits help minimize radiated and conducted EMI. Care should be taken to achieve a compact loop area.
2. A small capacitor in parallel to the clamp diode on the primary-side can help reduce radiated EMI.
3. Adjusting SR switch RC snubber component values can help reduce high frequency radiated and conducted EMI.
4. A pi-filter comprising differential inductors and capacitors can be used in the input rectifier circuit to reduce low frequency differential EMI.

Recommendations for Transformer Design

Transformer design must ensure that the power supply delivers the rated power at the lowest input voltage. The lowest voltage on the rectified DC bus depends on the capacitance of the filter capacitor used. At least 2 μF/W is recommended to always keep the DC bus voltage above 70 V, though 3 μF/W provides sufficient margin. The ripple on the DC bus should be measured to confirm the design calculations for transformer primary-winding inductance selection.

Reflected Output Voltage, V_{OR} (V)

This parameter describes the effect on the primary Switch drain voltage of the secondary-winding voltage during diode/SR conduction which is reflected back to the primary through the turns ratio of the transformer. To ensure flattest efficiency over line/load, set reflected output voltage (V_{OR}) to maintain K_P = 0.9 at minimum input voltage for universal input and K_P = 1 for high-line-only conditions.

Consider the Following for Design Optimization

1. Higher V_{OR} allows increased power delivery at VMIN, which minimizes the value of the input capacitor and maximizes power delivery from a given LinkSwitch-XT2SR device.
2. Higher V_{OR} reduces the voltage stress on the output diodes and SR Switches.
3. Higher V_{OR} increases leakage inductance which reduces power supply efficiency.
4. Higher V_{OR} increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

Quick Design Checklist

As with any power supply, the operation of all LinkSwitch-XT2SR designs should be verified on the bench to make sure that specifications of components are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum Drain Voltage – Verify that VDS of LinkSwitch-XT2SR and SR FET do not exceed 90% of breakdown voltages at the highest input voltage and peak (overload) output power in normal operation and during start-up.
2. Maximum Drain Current – At maximum ambient temperature, maximum input voltage, and peak output (overload) power, verify drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start up.
3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that temperature specification limits for LinkSwitch-XT2SR IC, transformer, output SR FET, and output capacitors are not exceeded. Enough thermal margin should be allowed for part to part variation of the $R_{DS(ON)}$ of the LinkSwitch-XT2SR IC as specified in the data sheet. Under low line and maximum output power, a maximum LinkSwitch-XT2SR SOURCE pin temperature of 100 °C is recommended to allow for these variations.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations website: www.power.com

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage		725 V / 900 V
DRAIN Pin Peak Current:	LNK3771D	1.09 A
	LNK3772D	1.70 A
	LNK3773D	2.38 A
	LNK3792D	2.20 A
BP Pin Voltage		-0.3 V to 6 V
BP Pin Current		100 mA
FWD Pin Voltage		-1.5 to 150 V
SR Pin Voltage		-0.3 V to 6 V
VOUT Pin Voltage		-0.3 V to 18 V
Storage Temperature		-65 to 150 °C
Operating Junction Temperature[3]		-40 to 150 °C
Ambient Temperature		-40 to 105 °C
Lead Temperature[4]		260 °C

Notes:
1. All voltages referenced to SOURCE and Secondary GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of
3. Normally limited by internal circuitry.
4. 1/16” from case for 5 seconds.

Thermal Resistance

(θ_{JA})	63 °C/W[2]
(θ_{JA})	54 °C/W[3]
(θ_{JC})[1]	18 °C/W

Notes:
1. Measured on the SOURCE pin close to plastic interface.
2. Soldered to 0.36 sq. inch (232 mm^2), 2 oz. (610 g/m^2) copper clad, with no external heat sink attached.
3. Soldered to 1 sq. inch (645 mm^2), 2 oz. (610 g/m^2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
BP Pin Voltage	V_{BP}	T_J = 25 °C		4.3	4.46	4.6	V
BP Pin Voltage Hysteresis	$V_{BP(H)}$	T_J = 25 °C			0.3		V
BP Shunt Voltage	V_{SHUNT}	I_{BP} = 2 mA T_J = 25 °C		4.53	4.65	4.82	V
BP Power-Up Reset Threshold Voltage	$V_{BP(UV)}$	T_J = 25 °C		4.08	4.15	4.23	V
FEEDBACK Pin Voltage	V_{FB}	T_J = 25 °C See Note A		1.97	2	2.03	V
Circuit Protection							
Standard Current Limit	I_{LIMIT}	di/dt = 78 mA/µs T_J = 25 °C	LNK3771D	253	273	292	mA
		di/dt = 127 mA/µs T_J = 25 °C	LNK3772D	413	444	475	
		di/dt = 147 mA/µs T_J = 25 °C	LNK3773D	478	514	550	
		di/dt = 127 mA/µs T_J = 25 °C	LNK3792D	413	444	475	
Auto-Restart On-Time	t_{AR}	T_J = 25 °C			50		ms
Auto-Restart Off-Time	$t_{AR(OFF)}$	T_J = 25 °C	First Off Period		150		ms
			Subsequent Periods		1500		
uVCC Supply Current	uVCC	V_{OUT} ≥ 5 V, IuVCC ≤ 20 mA, T_J = 25 °C		3.2	3.3	3.4	V

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	LNK3771D $I_D = I_{LIMIT}$	T_J = 25 °C		8.8	10.12	Ω
			T_J = 100 °C		13.5	15.60	
		LNK3772D $I_D = I_{LIMIT}$	T_J = 25 °C		5.61	6.45	
			T_J = 100 °C		8.5	9.97	
		LNK3773D $I_D = I_{LIMIT}$	T_J = 25 °C		4.06	4.67	
			T_J = 100 °C		5.95	6.85	
		LNK3792D $I_D = I_{LIMIT}$	T_J = 25 °C		5.2	5.98	
			T_J = 100 °C		8.26	9.5	
OFF-State Drain Leakage Current	I_{DSS1}	$V_{BP} = V_{BP} + 0.1$ V V_{DS} = 80% Peak Drain Voltage T_J = 125 °C				200	µA
	I_{DSS2}	$V_{BP} = V_{BP} + 0.1$ V V_{DS} = 325 V T_J = 25 °C			15		µA
Breakdown Voltage	BV_{DSS}	$V_{BP} = V_{BP} + 0.1$ V T_J = 25 °C	LNK377xD	725			V
			LNK3792D	900			
Drain Supply Voltage				25			V
Thermal Shutdown	T_{SD}	See Note C		132	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note C			70		°C
Output Voltage	V_{OUT}	End of Board at No-Load T_J = 25 °C, See Note D		4.90	5.00	5.10	V
VOUT Pin Overvoltage Threshold	$V_{OUT(OVP)}$				1.2 × V_{OUT}		V
VOUT Pin Auto-Restart Timer	$t_{VOUT(AR)}$	T_J = 25 °C			50		ms
Maximum Switching Frequency	f_{SREQ}	T_J = 25 °C		60	66	72	kHz

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Synchronous Rectifier @ T_J = 25 °C							
FW Pin Voltage for SR Turn-On	V_D			75	100	125	mV
FW Pin Voltage for SR Turn-Off	$V_{SR(TH)}$	T_J = 25 °C		6.1	7.7	8.7	mV
Rise Time	t_R	T_J = 25 °C C_{LOAD} = 4.7 nF	10-90%	160	210	270	ns
Fall Time	t_F	T_J = 25 °C C_{LOAD} = 4.7 nF	90-10%	90	105	120	ns
Output Pull-Up Resistance	R_{PU}	T_J = 25 °C V_{BPS} = 4.4 V I_{SR} = 2 mA		12.30	13.50	15.50	Ω
Output Pull-Down Resistance	R_{PD}	T_J = 25 °C V_{BSP} = 4.4 V I_{SR} = 2 mA		5.6	6.5	7.3	Ω

NOTES:
A. Used with external feedback.
B. Peak current can reach 60 mA for <4 ms.
C. This parameter is derived by characterization.
D. Using internal feedback.

Typical Performance Characteristics

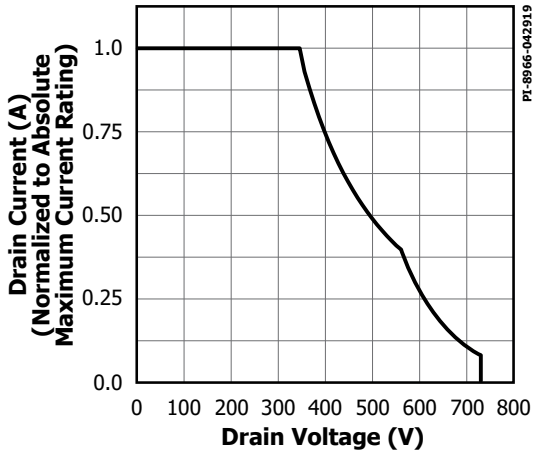


Figure 10. Maximum Allowable Drain Current vs. Drain Voltage (LNK3771 / 3772 / 3773).

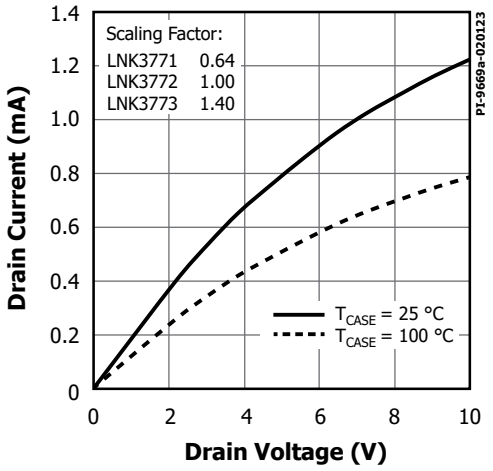


Figure 11. Output Characteristics.

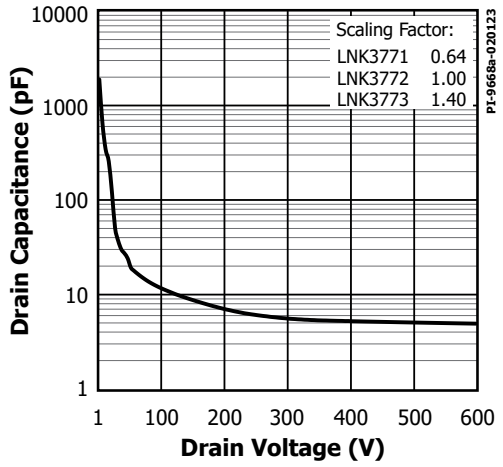


Figure 12. C_{OSS} vs. Drain Voltage.

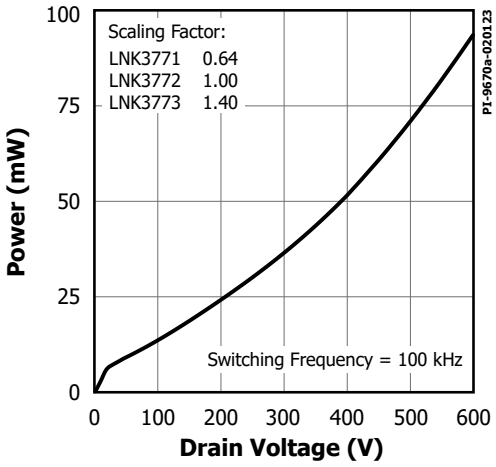


Figure 13. Drain Capacitance Power.

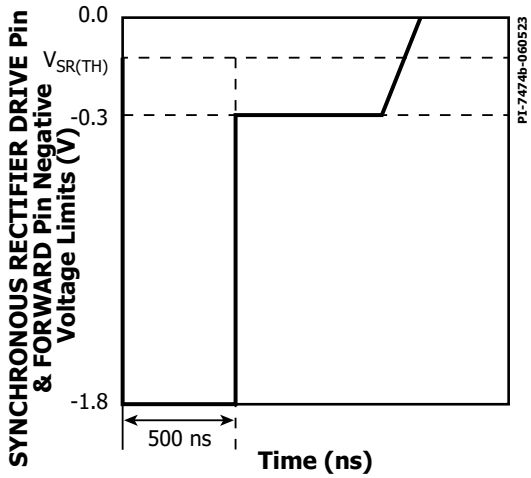


Figure 14. SYNCHRONOUS RECTIFIER DRIVE Pin and FORWARD Pin Negative Voltage Limits.

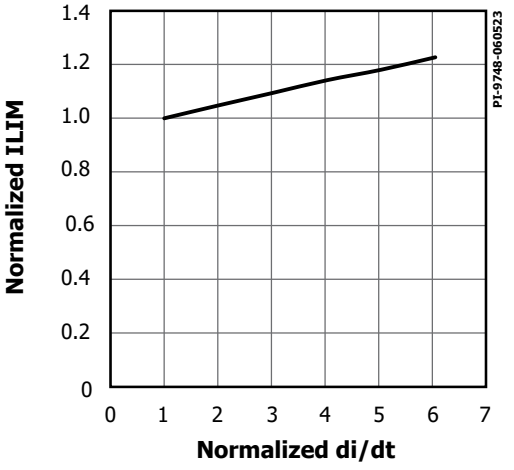


Figure 15. Standard Current Limit vs. di/dt.

Typical Performance Characteristics

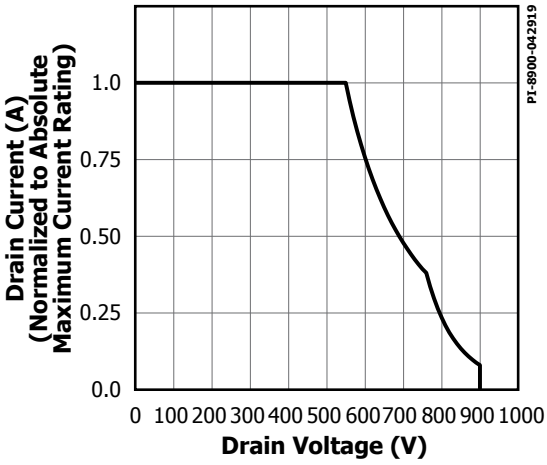


Figure 16. Maximum Allowable Drain Current vs. Drain Voltage (LNK3792).

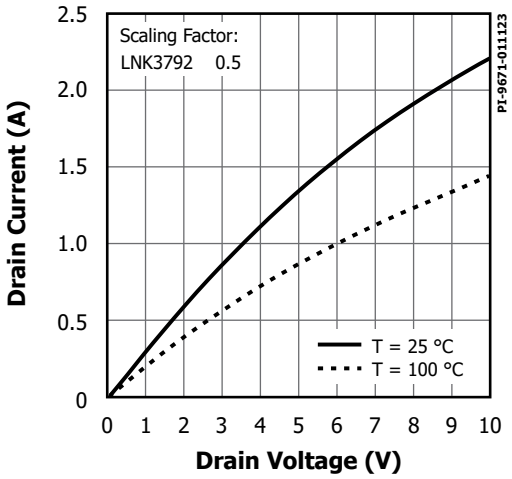


Figure 17. Output Characteristics.

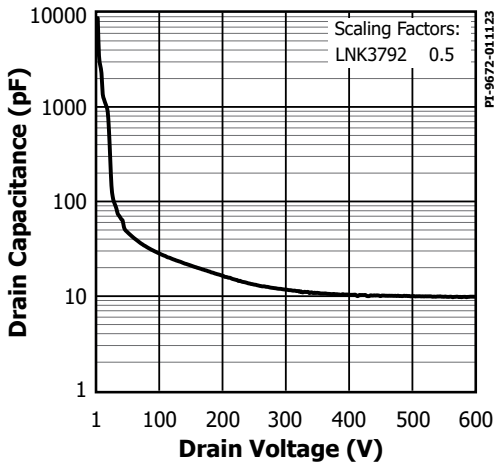


Figure 18. C_{OSS} vs. Drain Voltage.

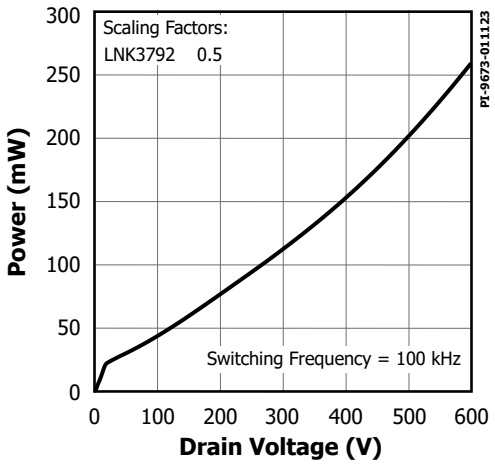


Figure 19. Drain Capacitance Power.

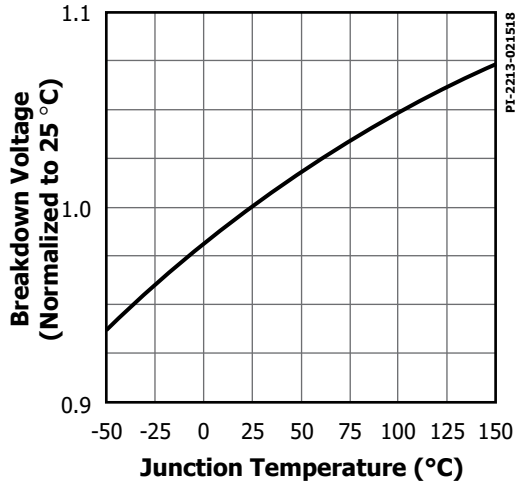


Figure 20. Breakdown vs. Temperature.

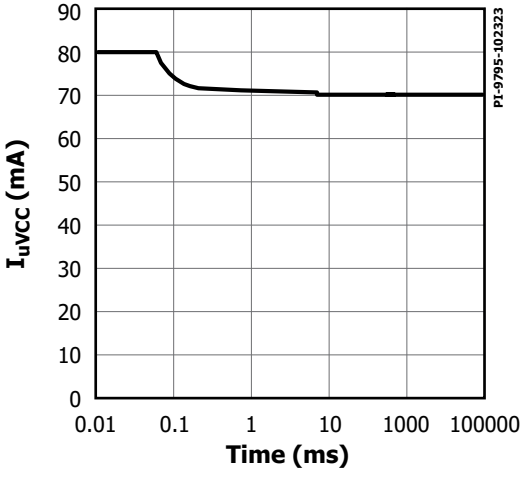
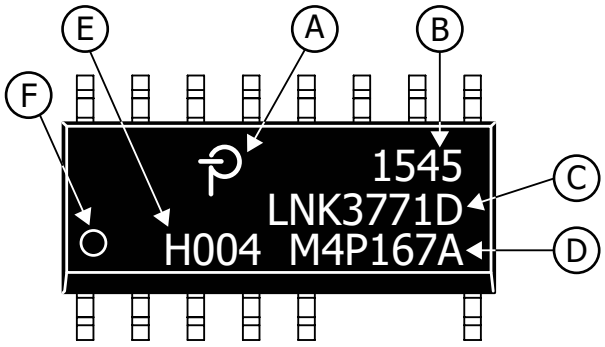


Figure 21. I_{uVCC} vs. Time.

PACKAGE MARKING

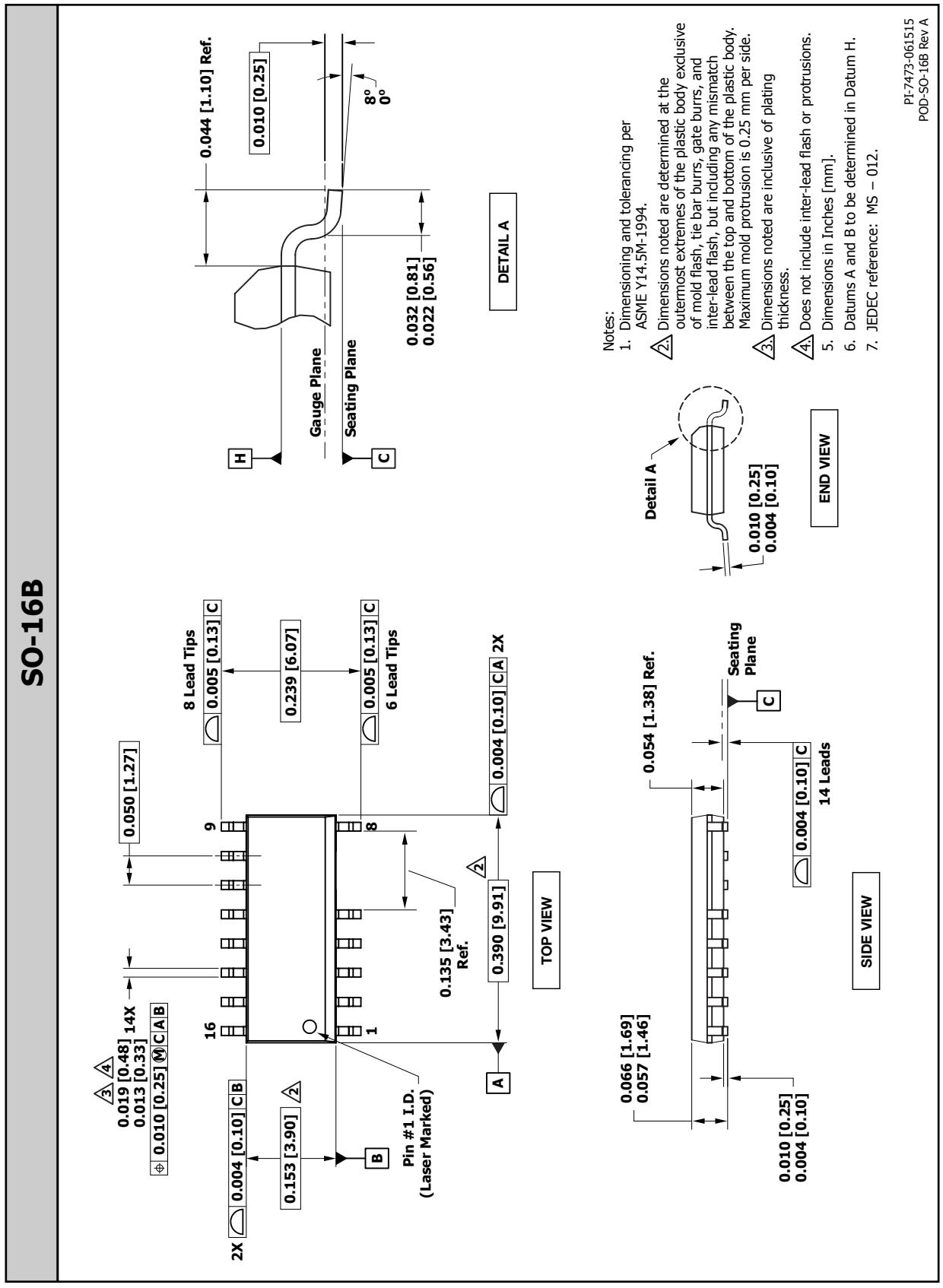
SO-16B



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of the year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Features Code
F. Pin 1 Indicator

PI-9584-081423

SO-16B



Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and inter-lead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.25 mm per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Dimensions in Inches [mm].
6. Datums A and B to be determined in Datum H.
7. JEDEC reference: MS – 012.

PI-7473-061515
POD-SO-16B Rev A

Feature Code Table[1,2]

Feature Code	Feedback
H003	5 V Internal
H004	External Resistors

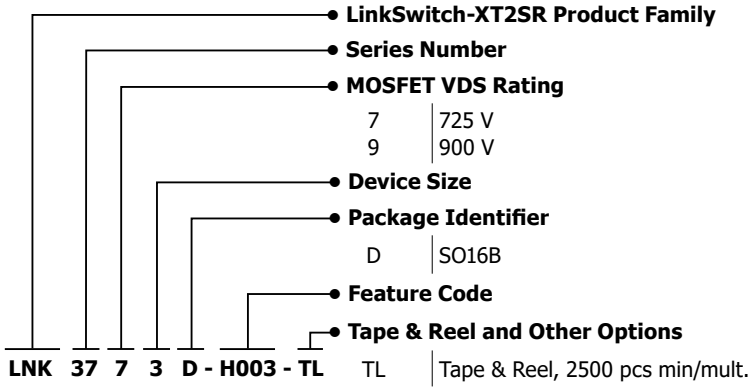
MSL Table

Part Number	MSL Rating
LNK3771D	3
LNK3772D	3
LNK3773D	3
LNK3792D	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2000 V on all pins
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±500 V on all pins

Part Ordering Information



Revision	Notes	Date
A	Preliminary release.	09/22
B	Introduction release.	03/23
C	Production release.	05/23
D	Updated Table 1 900 V Switch power to 85 – 484 VAC, and Figure 4 VAC input power. Added new Figures 7, 15 and 21.	10/23

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