Design Example Report

Title	**24 W Multi-Output Flyback Converter with One CV and Four CC Outputs Using InnoMux™2-BL IMX2065C and the LED Backlight Controller IC IML204DG**
Specification	90 VAC – 265 VAC Input; 5 V / 1.2 A, 25 V / 400 mA – 56 V / 320 mA (18 W LED Outputs)
Application	PC Monitor PSU
Author	Applications Engineering Department
Document Number	DER-715
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Summary and Features

Unique single-stage conversion, multiple-output flyback architecture enabling:

- High efficiency across the universal line range
- High regulation accuracy - independently regulated 5 V / 1.2 A CV output
- Four CC (LED) output with wide string voltage range from 25 V to 56 V
- All Four CC output currents are matched to within 3% matching error
- Configurable for
  - Analog dimming mode
  - Straight PWM dimming mode
  - Filtered PWM dimming mode
- Safety features
  - Output overvoltage protection (OVP), eliminating the need for a fault protection optocoupler
  - Output power limit set independently for each output
  - Accurate thermal protection with hysteretic shutdown
  - Input voltage monitor with accurate brown-in/brown-out and overvoltage protection
- Audible noise is 24 dBA in operation mode, and 22 dBA in standby mode

InnoMux2-BL is the industry's first single chip AC/DC solution with integrated multiple feedbacks, ensuring isolation and safety ratings. Additionally, the pulse-sharing feature significantly reduces audible noise, making it suitable for use in quiet appliance applications.

The control chip incorporates isolated feedback and communication channels, combining all the benefits of secondary-side control with the simplicity of primary-side regulation.

The new architecture achieves accurate cross-regulation across multiple outputs and high overall efficiency, simplifying the entire system by eliminating the need for post-regulation. The single-stage converter significantly reduces board size and part count compared to the equivalent conventional converter based on a two-stage conversion stage topology.

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a Switch Mode Power Supply (SMPS) intended for monitor applications. The SMPS utilizes the Power Integration's InnoMux2-BL controller. The controller implements a multiplexing power control algorithm, where the energy stored in the primary winding of the transformer during any primary conduction interval is subsequently delivered to only one of the converter's main outputs (CV1 or LED). More specifically, this is achieved by controlling the state of the selection MOSFET (Figure 3) during the flyback interval of each switching cycle. Utilizing a single magnetic component (transformer TX1), the controller directs the energy flow as needed to all outputs based on respective loading requirements, thus keeping each output accurately controlled. If the energy pulse needs to be delivered to the CV1 output, selection FET is turned ON prior to the end of the primary conduction interval. Otherwise, if selection FET is OFF, the energy is delivered to the LED output via the rectification diode D1.

The SMPS has one Constant Voltage (CV) outputs, 5 V / 1.2 A and a 4-string Constant Current (CC) output, capable of delivering maximum of 0.4 A current into an LED stack with voltage from 25 V to 56 V. The maximum output power of the LED strings is 18 W, i.e., the maximum LED current through 56 V LED stack should be limited to 320 mA. The current through the LED stack is controlled from zero to maximum by the PWM dimming signal (DIM1). The currents through 4 LED strings are accurately matched, and the matching error is up to 3%. The Power Supply Unit (PSU) can deliver a total maximum output power of 24 W, with universal mains input (from 90 VAC to 265 VAC).

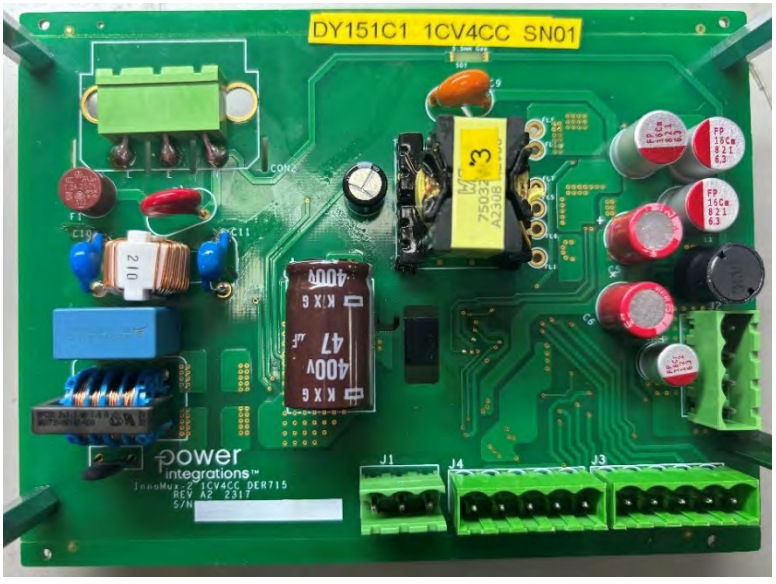


Figure 1 – PCB, Top View.

Figure 2 – PCB, Bottom View.

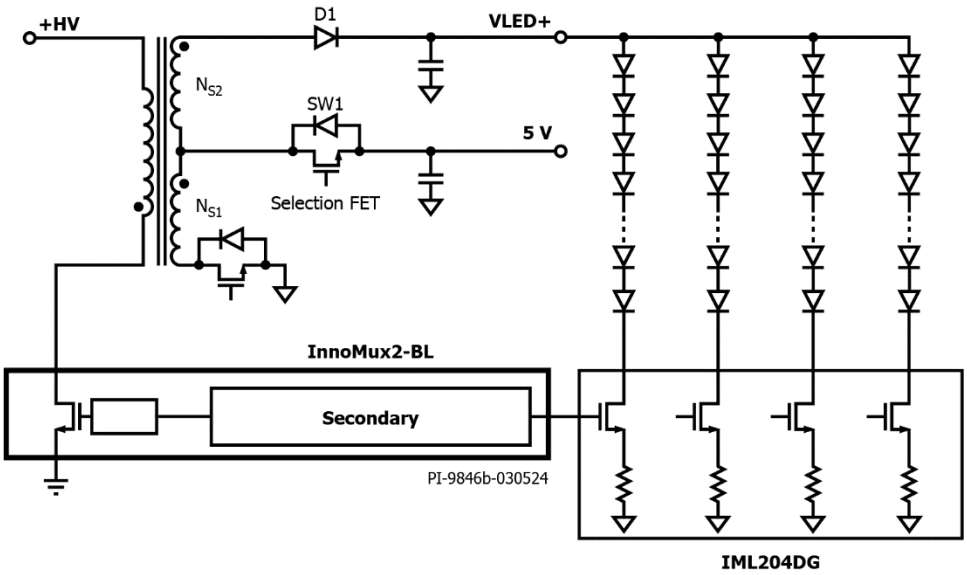


Figure 3 – DER-715 High Level Schematic.

The VCV1 and VLED (FB) pins continuously sense the output voltages. If the voltage of any of the outputs drops below regulation level, InnoMux2-BL secondary-side sends a request for pulse to the primary-side controller. This type of pulse-by-pulse regulation results in quick response and excellent cross-regulation. This SMPS utilizes a single-winding architecture on the secondary-side to simplify transformer design. For the described multiplexing algorithm to work correctly, it is essential that the reflected voltage of each winding must be higher than that of the preceding lower output voltage winding to effectively steer the power:

$$\frac{V_{CV1}}{N_{S1}} < \frac{V_{LED}}{N_{S1} + N_{S2}}$$

Transformer with stacked or independent secondaries may be used as appropriate. The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. The actual performance is illustrated in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	3 Wire Input.
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage 1	V_{OUT1}	4.75	5	5.25	V	±5%.
Output Ripple Voltage 1	$V_{RIPPLE1}$			100	mV	20 MHz Bandwidth.
Output Current 1	I_{OUT1}	0		1.2	A	
Output Voltage 2	V_{OUT2}	25	45	56	V	
Output Current 2	I_{OUT2}	0	0.32	0.4	A	20 MHz Bandwidth.
Output Power 2	P_{OUT2}	0		18	W	
Total Output Power						
Output Power	P_{OUT}		24		W	
Efficiency						
Full Load	η	88			%	Measured at 115 / 230 VAC, P_{OUT} 25 ºC.
No-Load Input Power				<0.3	W	Measured at 230 VAC 25 ºC, 5 V 30 mA.
Environmental Conducted EMI Safety	Meets CISPR22B / EN55022B Designed to meet IEC950, UL1950 Class II					
Ring Wave				±4	kV	12 Ω Common Mode.
Surge Differential Mode				±2	kV	2 Ω Differential Mode.
Surge Common Mode				±2	kV	12 Ω Common Mode.
ESD				±15 ±8	kV	Air Discharge. Contact Discharge.
Ambient Temperature	T_{AMB}		25		ºC	Free Convection, Sea Level.

3 Schematic

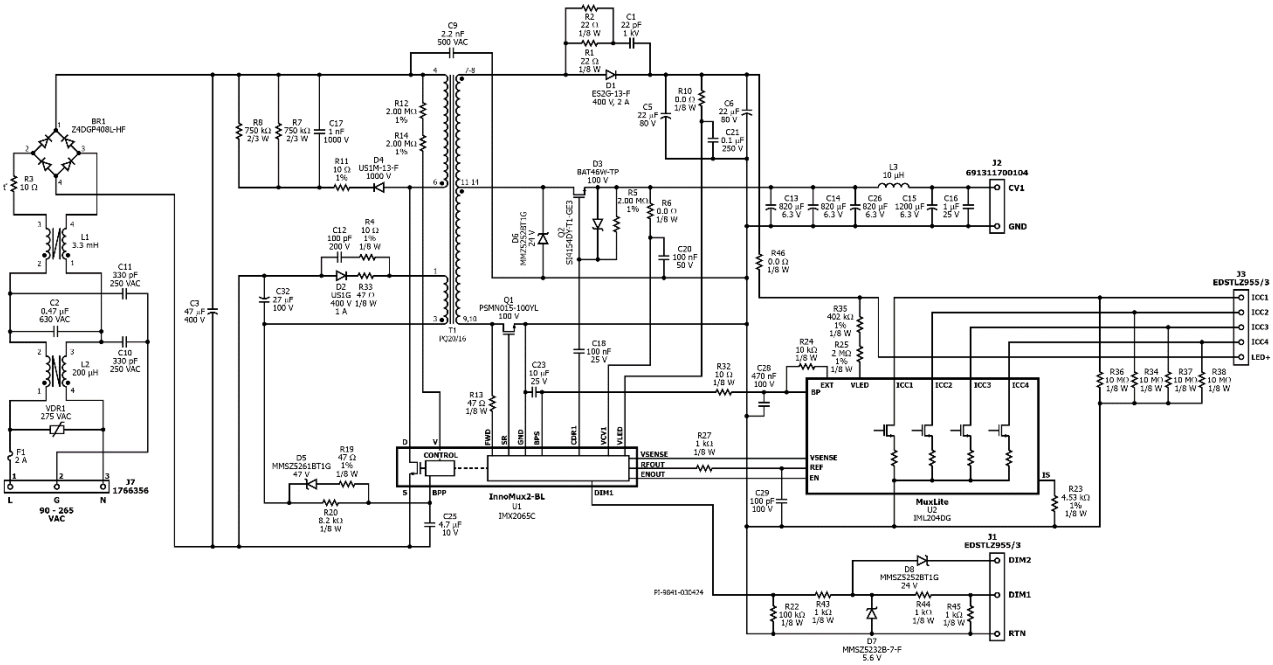


Figure 4 – Schematic.

4 Circuit Description

4.1 Input Rectifier and EMI Filter

A two-stage EMI filter is used: L1/C2 - for the lower frequency range and L2/C10/C11 for the high frequency range. Mainly common mode noise is suppressed by the input EMI filter, but some degree of differential noise attenuation is also achieved. These measures along with the Y capacitor C9, and the screen windings in the transformer keep the conducted emissions below the specification limits.

The bulk storage capacitor C3 provides DC voltage smoothing after the bridge rectifier BR1. Varistor VDR1 provides protection against differential voltage surges. Resistor R3 (NTC) limits the inrush current at power up. Fuse F1 protects the PSU from drawing excessive current from the mains.

4.2 Primary-Side

See latest data sheet for InnoMux2-BL operation details.

4.2.1 Primary Switch Arrangements

The transformer primary is connected between the input DC bus (TXPRI+) and the drain D of the integrated primary switch of InnoMux2-BL IC (U1 pin 24). Primary current is returned to the bulk capacitor (C3) via the source tab of U1 (pin 16). An RC type primary clamp (R11, R7, R8, C17, D4) is used to limit the peak drain voltage of the integrated primary switch, which is caused by transformer leakage inductance and output trace inductance.

4.2.2 Primary-Side Controller Power Source and OVP Protection

The primary-side controller is part of the InnoMux2-BL IC (U1). It is self-starting, using an internal high-voltage current source to charge the BPP capacitor C25, when AC voltage is first applied to the converter input. During normal operation (steady-state) the primary-side of the controller is powered from an auxiliary winding on the main transformer. The voltage across this winding is rectified and filtered using diode D2 and capacitors C24 and C32. Resistor R33 is inserted into the discharge circuit to limit the transient current to the auxiliary circuit. The primary auxiliary output is then connected to the BPP pin via a current limiting resistor R20.

4.2.3 Primary-Side OVP, Brown-In and Brown-Out Protection

A crude primary-side output overvoltage protection (OVP) is implemented by Zener diode D5 and the series resistor R19. In the event of an uncontrolled overvoltage at the output, the increased voltage at the bias winding causes the Zener diode D5 to break into conduction, increasing the current into the BPP pin. If this current exceeds a predetermined value I_{SD} = 7.5 mA, the OVP protection is triggered.

Resistor R12 and R14 provide line voltage sensing to facilitate controlled brown-in/out transients. The thresholds for these transients are set to approximately 75 VAC and 65

VAC respectively. At approximately 320 VAC, the current through these resistors exceeds the input over overvoltage threshold, which will result in the disabling of U1.

4.2.4 Primary Peak Current Limit

The value of capacitor C25 is used to set the maximum primary current to STANDARD or INCREASED level. In this case a 4.7 μF capacitor sets the primary-side controller peak current limit to its INCREASED level of 1.15 A.

4.3 Secondary-Side

See latest data sheet for InnoMux2-BL operation details.

The secondary-side of the InnoMux2-BL (U1) is powered from the 5 V BPS rail generated internally. Capacitor C23 is a local decoupling capacitor.

4.3.1 Primary to Secondary-Side Communication

The secondary-side of the InnoMux2-BL IC (U1) sends a request to the primary-side controller to initiate a switching cycle. This is done by sending a pulse via the internal FluxLink™, a galvanically isolated communication channel.

4.3.2 Powering InnoMux2-BL Secondary-Side

During start-up the InnoMux2-BL's secondary-side is powered by VLED+ via R10. There is a local decoupling capacitor C21 connected close to the VLED+ pin of U1. Resistor R10 and C21 are optional and provide additional ESD protection. An internal regulator lowers the VLED+ voltage to 5 V and supplies it to the BPS bus (U1 pin 6).

In steady-state, when the voltage on VCV1 (U1 pin 10) falls within the direct power mode range (4.65 V to 5.45 V), the internal BPS regulator is deactivated. In this state, the secondary circuit is directly powered from VCV1, effectively minimizing power dissipation in standby mode. Resistor R6 and C20 provide local decoupling and ESD protection.

4.3.3 Synchronous Rectifier (SR) MOSFET Control

The SR pin is used to drive the SR MOSFET (Q1) when the transformer is delivering energy to the secondary circuit. The gate voltage of the SR MOSFET is reduced before the end of secondary discharge, to maintain the SOURCE to DRAIN voltage across SR MOSFET. This functionality plays a crucial role in preventing premature turn-off of the SR MOSFET.

In DCM operation, SR MOSFET (Q1) is turned on for a short period of time right before the primary switch turns on. This action generates a reverse current in the CV1 secondary winding, which then causes a reverse current flow in the transformer on the primary side when the SR MOSFET is turned off. Subsequently, the reverse current discharges the voltage across the primary switch until the voltage is close to zero, allowing the primary switch to turn on at zero-voltage. This is called SR-ZVS, which substantially minimizes switching loss.

4.3.4 Selection MOSFET Drive

The gate drive amplitude for the selection MOSFET Q2 is approximately equal to the voltage on the BPS rail (5 V). Consequently, logic level MOSFETs must be used. When CDR1 is low, capacitor C18 is charged up to the level of V_{CV1} from CV1 output via diode D3. When the selection MOSFET Q2 needs to be gated on, CDR1 pin voltage is raised from GND to BPS, causing the gate voltage of the selection MOSFET to rise to $V_{CV1}+V_{BPS}$.

The secondary control circuit in InnoMux2-BL IC requires access to the idle ring waveform through the FWD pin to calculate its timing and facilitate valley switching. Such access is ensured by keeping Q2 on even after secondary conduction time is finished.

4.3.5 Output Control

Output rectification for the CV1 output is provided by the SR FET (Q1) and the CV1 selection FET (Q2). To ensure low output ripple voltage, a Π – type LC filter (C13, C14, C26, C15, C16 and L3) is employed. Low ESR capacitors C13, C14, C26 and C15 are used to minimize switching noise. Capacitor C26 and C44 are Al-electrolytic type. Additionally, a small multilayer ceramic (MLC) capacitor C16 is connected across the 5 V output terminals to provide a low-impedance bypass for any high-frequency noise.

Output rectification for the LED output is provided by LED diode (D1) and SR FET (Q1). Very low-ESR capacitors C4 and C6 provide energy storage and filtering at the LED output.

The RC snubber network R1, R2 and C1 serves to dampen high-frequency ringing across the rectifier diode D1. This ringing is a result of the transformer leakage inductance and the secondary's trace inductance oscillating with the diode capacitance.

Zener diode D6 is used as a voltage clamp for the transformer CV1 winding while the primary FET is on and Q1, Q2 are turned off, and D1 is reverse biased. In this condition, the secondary windings are floating with respect to GND. Without D6, the voltage on Q2 drain could be too high due to transformer winding capacitance.

When both the selection FET (Q2) and SR FET (Q1) are turned on, the transformer secondary windings are designed such that the voltage on the anode of D1 is below the lowest working LED string voltage. As a result, D1 remains reverse-biased, ensuring that all the transformer energy is directed to the CV1 output via selection FET Q2.

When the delection FET (Q2) is turned off, and the SR FET (Q1) is turned on, the voltage on the anode of D1 rises until it is forward-biased. In this condition, all the transformer energy is directed to the LED output.

The set point for the CV1 output is determined by the internal trim code settings, CV1 voltage is monitored via a feedback signal to the VCV1 pin of InnoMux2-BL IC.

LED+ output maximum voltage is set by the internal trim code. In this design it has been set to the default value of 60 V. Note that the actual LED+ voltage is not set by the trim code, and it varies depending on the LED stack voltage and the current source voltages (ICC1, ICC2, ICC3 and ICC4) on the LED driver IML204DG IC (U2).

The current through each LED string is controlled separately by the LED driver IML204DG IC (U2). The resistor on IS pin of U2 (R23) sets the LED string current.

$$I_{LED(MAX)} = \frac{1.5\ V}{R_s} \times 320$$

The matching accuracy of the LED strings is <3% when the LED string current is above 5 mA. Although the maximum VLED+ is set by the trim code on U1, a maximum VLED+ needs to be set for U2 for it to run LED open string fault detection. This maximum VLED+ voltage for U2 is set by the resistors on VLED pin of U2 (R25 and R35). In this design, the full-scale current is set to 106 mA for each LED string, and the maximum VLED+ for U2 is set to 56.5 V.

4.3.6 LED Current Control and Dimming

The application is configured for 1-wire filtered PWM dimming mode. The maximum total current through the 4 LED strings is 400 mA (4 x 100 mA). It is achieved at 94% duty cycle on DIM1.

Other dimming options are also available, such as PWM or analog dimming. For more details, please see the latest InnoMux2-BL data sheet on the website.

4.3.7 Output Power Limiting

A power limit can be applied to each output individually by setting the internal trim code in InnoMux2-BL IC (U1). Power is restricted by limiting the maximum average frequency an output can receive charging pulses. The frequency limit is set by the trim code bits PLIM1 and PLIM3. Specifically, PLIM1 bits set the frequency limit for output CV1, and PLIM3 bits set the frequency limit for LED output. If the frequency surpasses the predefined limit for a set time interval, the InnoMux2-BL controller will initiate an auto-restart. Power limit is a custom trim code, in this design, power limit is not implemented.

4.3.8 Standby Mode

If the DIM1 input is held at 0 V the PSU enters “Standby Mode”. The LED current is disabled and the internal LED driver circuit is powered down, reducing the controller’s own power consumption. While in Standby Mode, fully rated power is still available on the CV1 output. The +V_LED output is maintained at a level of at least 8 V - the minimum voltage that can power up the controller’s secondary-side. The DIM1 input is a logic level type. If it is pulled up to above 3.3 V (5 V_{MAX}), the LED current will be enabled.

4.3.9 Start-Up Sequence

Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7
Pri Switch V_{DS} [V]	V_{CV1} [V]	BPS [V]	V_{LED+} [V]	I_{LED} [mA]	I_{CV} [A]	SR_{GATE} [V]

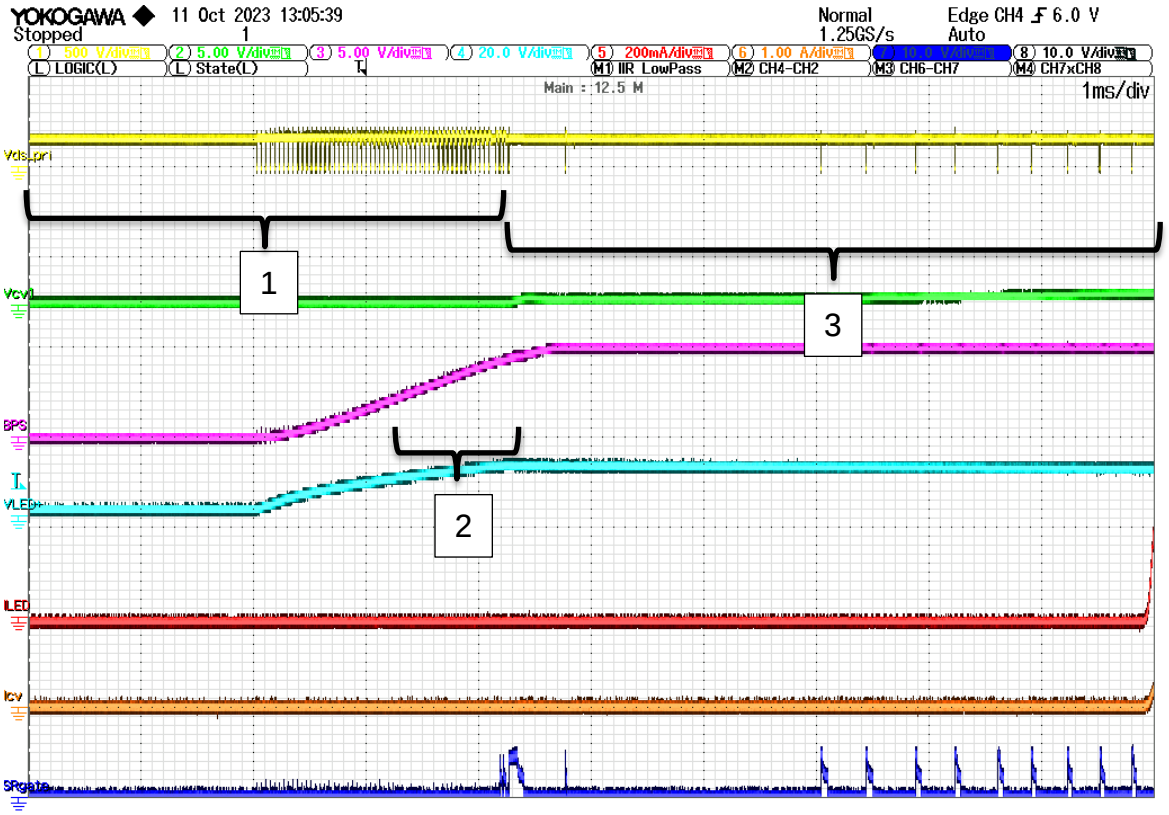


Figure 5 – First 10 ms of Start-up.

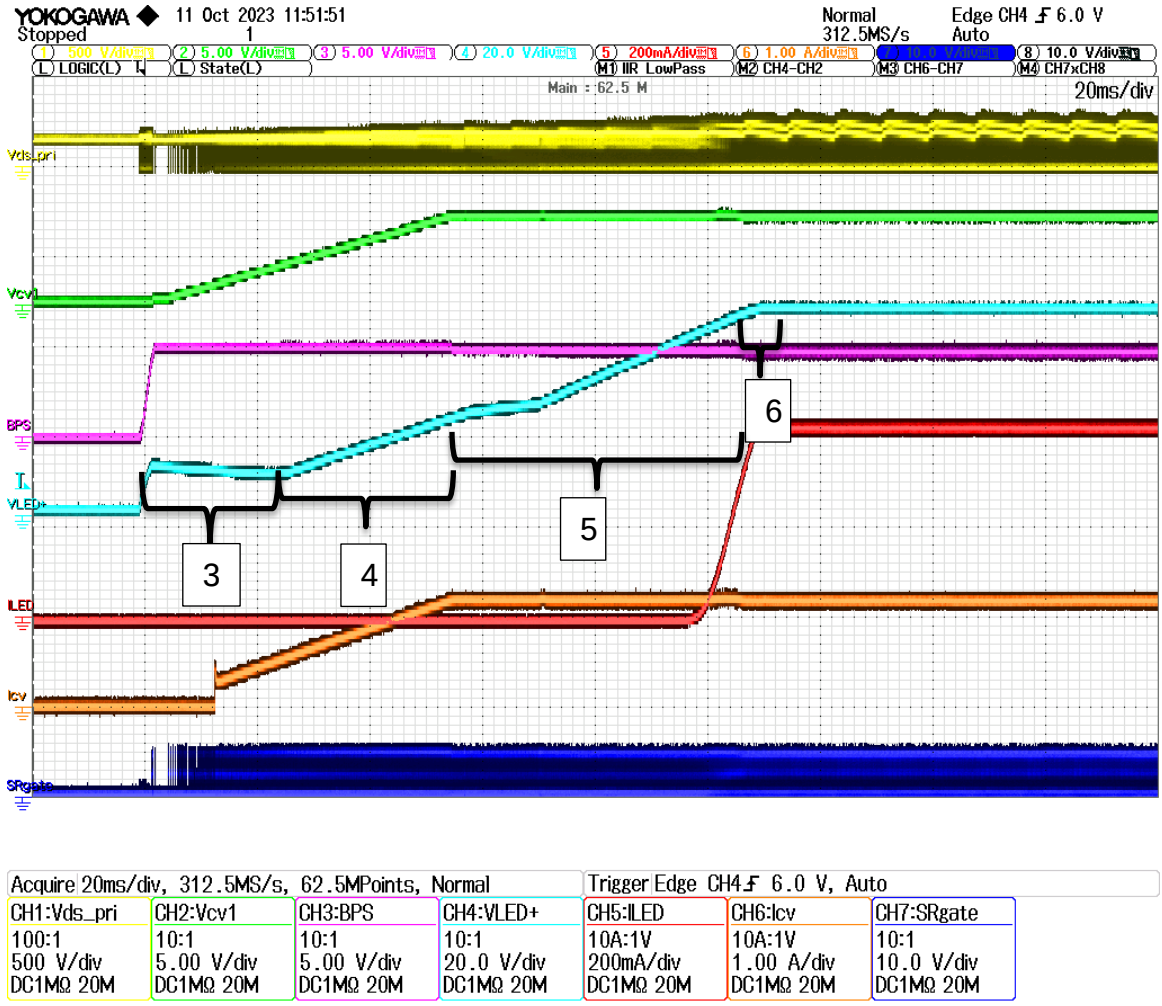


Figure 6 – Complete Start-Up Cycle.

1. Mains voltage is applied to the primary-side, after the primary wait and listen time, the primary assumes primary control. The controller starts operating with an open loop and switching at a fixed soft-start frequency of 25 kHz. During this period, the secondary is off, and V_{LED} begins to rise.

2. The controller secondary-side is powered up by the internal BPS regulator through either the FWD pin tap or once V_{LED} is high enough. The secondary reads the trim code, configured the internal feedback and handshakes as soon as possible. The switching of the secondary SR MOSFET (Q1) indicates that the primary and secondary handshake occurred and the secondary now has control.

   If the secondary-side does not wake up and respond, the primary-side will:
   a. time out and shut down, or
   b. the primary-side bias voltage will rise high enough to trigger a bias OVP shutdown.

3. Following the handshake, the fixed 25 kHz switching frequency is concluded. InnoMux2-BL IC (U1) transitions to switching based on the feedback and reference voltages on CV1 and VLED+. The CV1 voltage linearly increased, while the VLED+ voltage is held at the stay-alive voltage ($V_{STAYALIVE}$, ~8.0 V) to supply input to the internal BPS regulator.

4. CV1 and LED output voltages can be seen rising simultaneously. When the V_{CV1} is raised to the same reference percentage as the V_{LED}, the InnoMux2-BL IC (U1) starts ramping up V_{LED}. When V_{CV1} reaches its designed reference level, V_{LED} is as high as the voltage reflected from the turns ratio between CV1 winding and LED winding $V_{LED} = \frac{V_{CV1}}{N_{S1}} \times (N_{S1} + N_{S2})$.
   At some time during interval 4, the CV1 will reach a sufficient level to power the internal BPS regulator via the VCV1 pin (U1 pin 10). The internal BPS regulator is then bypassed, and the secondary circuit is directly powered from the CV1 output. This is the direct power mode, which substantially reduces standby power loss.

5. The controller keeps ramping V_{LED} up till it's high enough for current to go through the LED string and that all the LEDs can be lit up.

6. The LED current is enabled. Its level depends on the dimming configuration and the signal on the dimming input. The LED current is controlled by the internal LED drivers on the IML204DG controller (U2) ICC1 to ICC4 (U2 pins 1, 2, 15, 16). To reduce its own dissipation the InnoMux2-BL controller (U1) maintains V_{LED} at a level with some minimum headroom above the LED stack voltage. This keeps the voltage at the ICC pins to a minimum.

5 DER-715 Connection Diagram

The connection diagram on Figure 7 below shows a 1-wire filtered PWM dimming configuration. For other dimming configurations, please refer to the product data sheets.

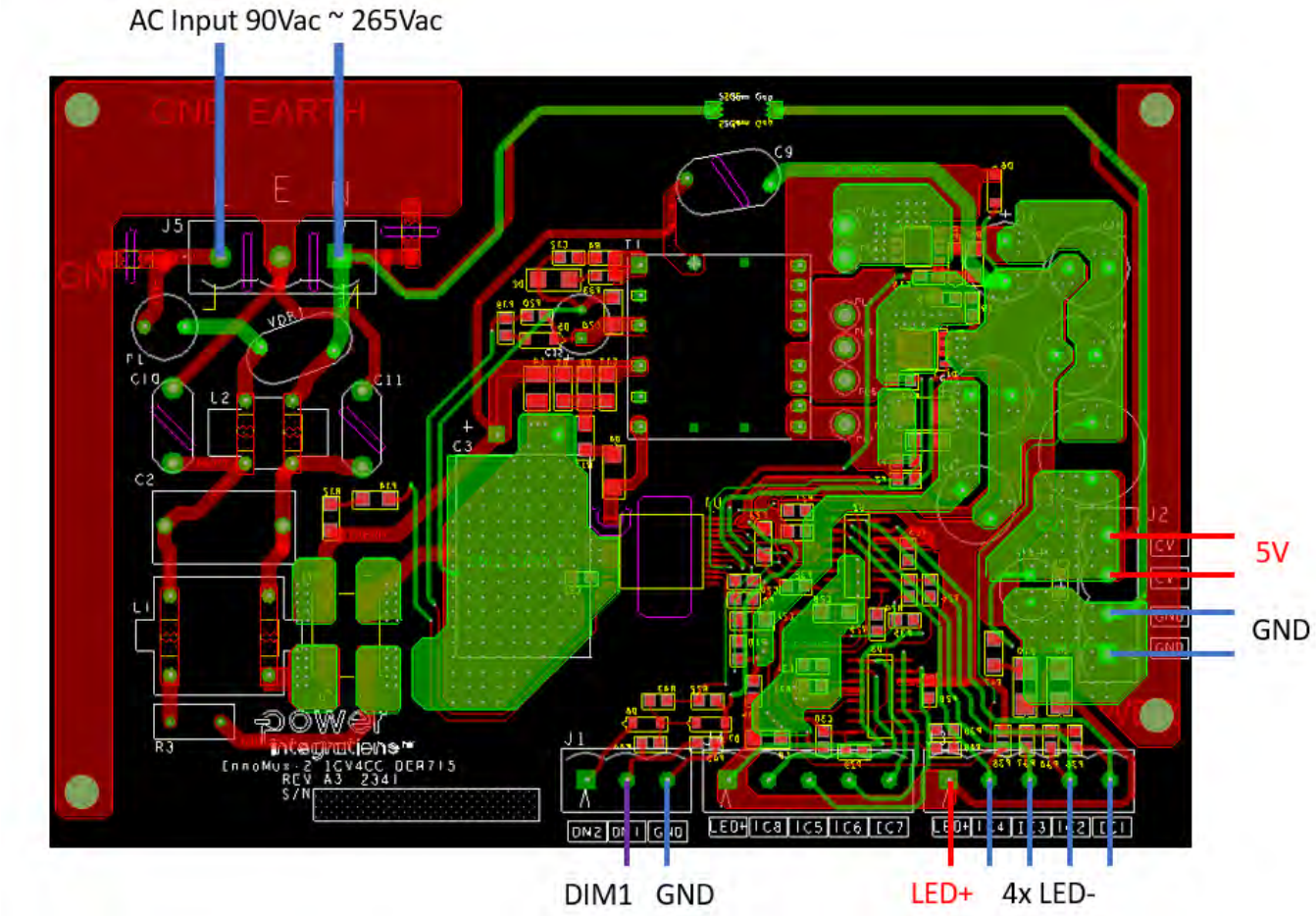


Figure 7 – Connection Diagram.

6 PCB Layout

The converter PCB layout is illustrated on Figure 8, Figure 9 and Figure 10 below. PCB copper thickness is 2 oz (2.8 mils / 70 μm).

(1) FWD pin: FWD signal has large dv/dt, which can be one of the major noise sources on the secondary circuit. FWD signal is critical for the controller so its PCB route should be kept away from the other signals. A 90° angle route is used here to ensure FWD signal is as far from the other signals as possible.
(2) Ground plane: The impedance from InnoMux2-BL controller's ground to SOURCE terminal of the SR MOSFET (Q1) should be minimized. Ground for both controllers U1 and U2 should be separated from the power return ground. Star-connection ground is used here, to prevent the large secondary discharge current from affecting the ground level of the InnoMux2-BL controller (U1) and LED backlight controller IML204DG IC (U2).
(3) Thermal: The primary switch in InnoMux2-BL IC (U1) is cooled through the SOURCE pin of the IC. It is crucial to minimize the thermal impedance between the SOURCE pin and the PCB cooling copper, as illustrated in Figure 8. To enhance cooling efficiency, a substantial copper area is employed.

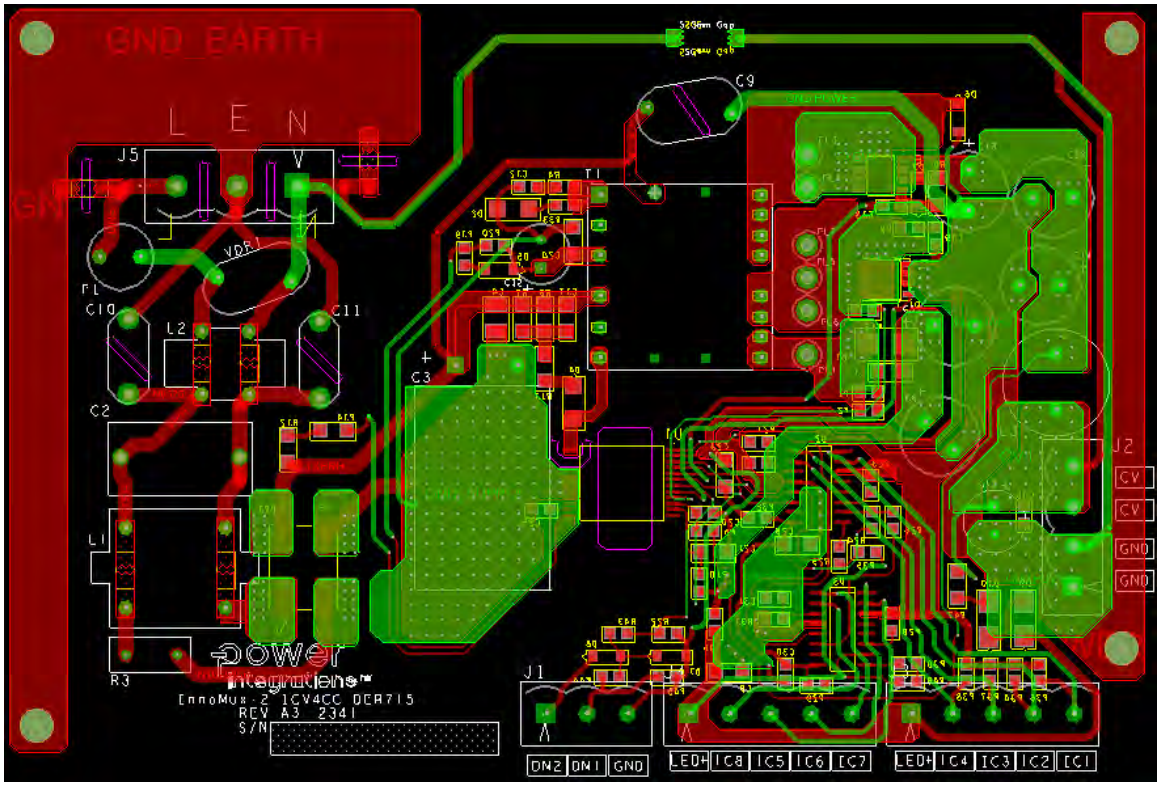


Figure 8 – Printed Circuit Layout.

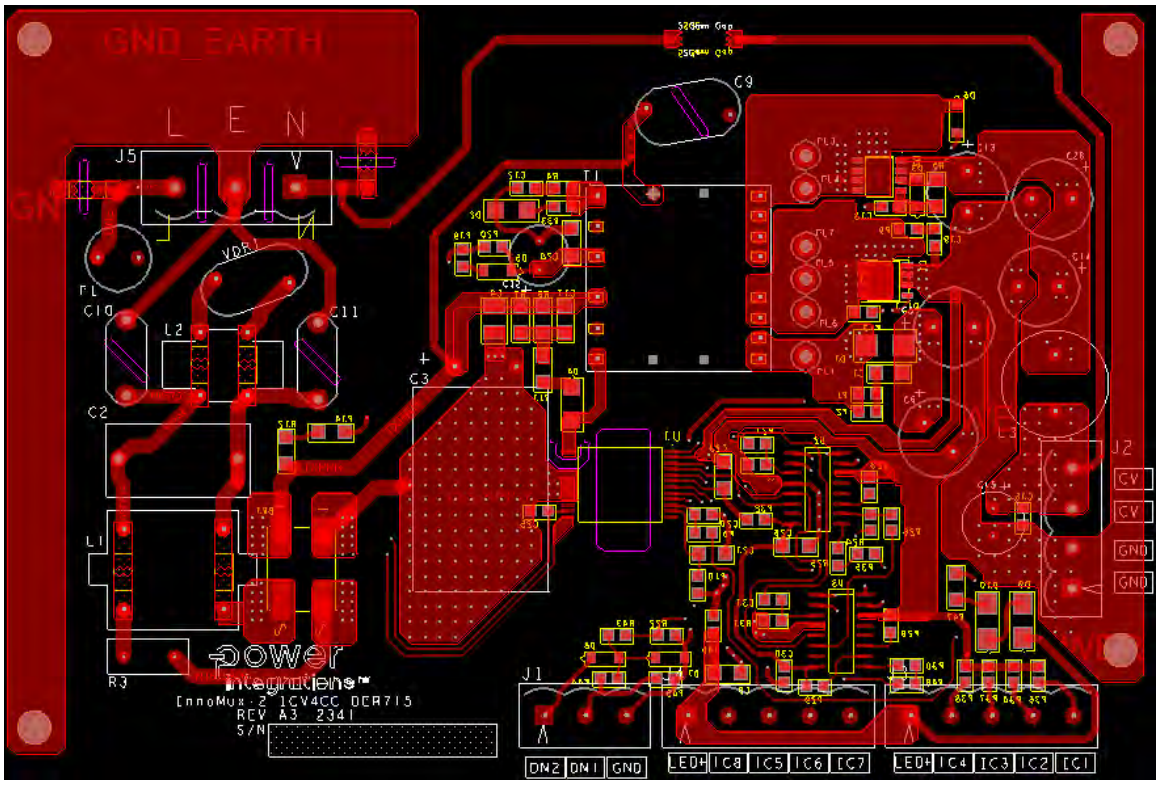


Figure 9 – Printed Circuit Layout, Bottom.

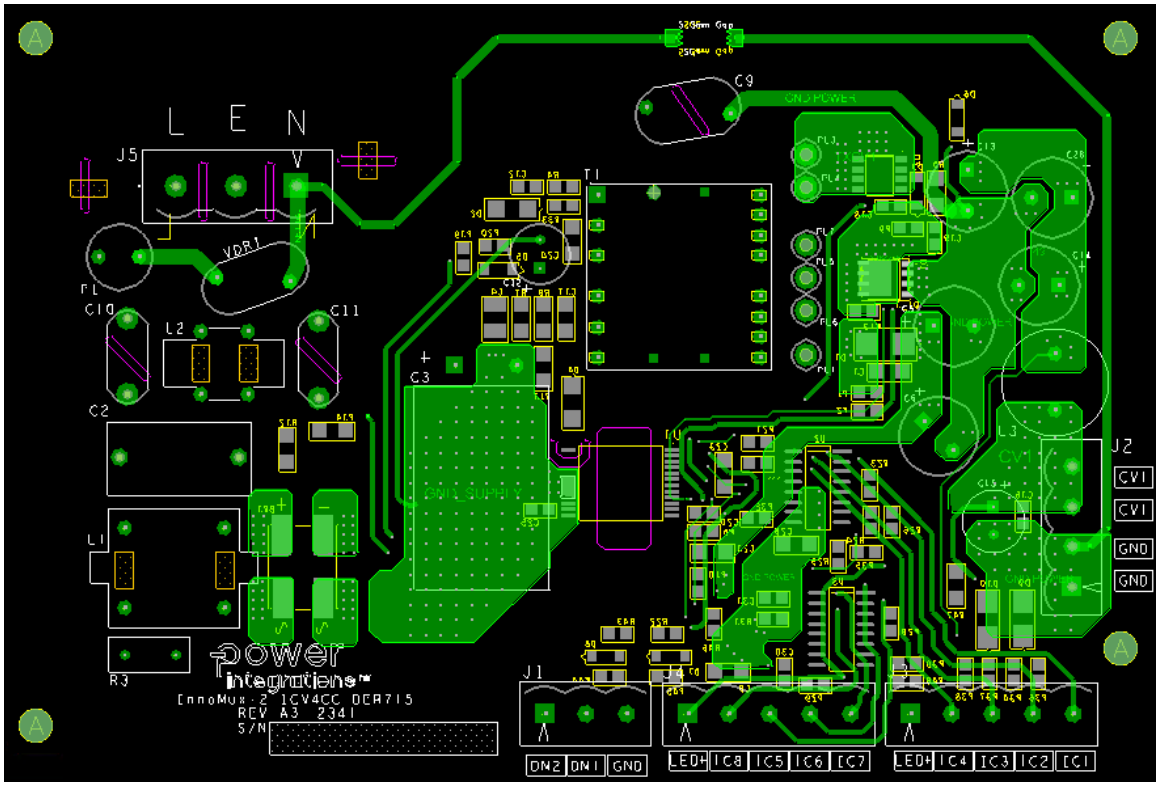


Figure 10 – Printed Circuit Layout, Top.

7 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	RECT BRIDGE, GP, 800 V, 4A, Z4-D	Z4DGP408L-HF	Comchip
2	1	C1	22 pF, 1000 V, Ceramic, COG, 1206	C1206C220KDGACTU	Kemet
3	1	C2	0.47 µF, ±20%, Film Capacitor, 305 VAC 630 VDC, Polypropylene (PP) X2, Radial	B32922C3474M000	TDK
4	1	C3	47 µF, 400 V, Electrolytic, Low ESR, 730 mΩ, (16 x 25)	EKMG401ELL470ML25S	United Chemi-Con
5	2	C5 C6	22 µF, 80 V, Aluminum - Polymer Capacitors, Radial, Can, 35mOhm, 2000 Hrs @ 105°C, (10 x 14)	870056175003	Würth
6	1	C9	2200 PF, ±20%, 500 VAC (Y1),760 VAC (X1), Ceramic, Y5U (E), RADIAL	440LD22-R	Vishay
7	2	C10 C11	330 pF, Ceramic Y1	440LT33-R	Vishay
8	1	C12	100 pF, 200 V, Ceramic, COG, 0805	08052A101JAT2A	AVX
9	3	C13 C14 C26	820 µF, 6.3 V, Al Organic Polymer, Gen. Purpose, 20%	RR50J821MDN1	Nichicon
10	1	C15	1200 µF, ±20%, 6.3 V, Aluminum - Polymer Capacitors Radial, Can 10mΩ, 2000 Hrs @ 105°C, (8 x 10)	RNE0J122MDN1	Nichicon
11	1	C16	1 µF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
12	1	C17	1 nF, 1000 V, Ceramic, X7R, 1206	CC1206KKX7RCBB102	Yageo
13	1	C18	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX
14	1	C20	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
15	1	C21	0.1 µF, 250 V, ±10%, Ceramic, X7R, 1206	C3216X7R2E104K160AA	TDK
16	1	C23	10 µF, ±10%, 25 V, Ceramic Capacitor X7R, 1206	C1206C106K3RACAUTO	KEMET
17	1	C25	4.7 µF ±10% 10V Ceramic Capacitor X7R 0805	LMK212B7475KGHT	Taiyo Yuden
18	1	C28	470 nF, 100 V, Ceramic, X7R, 1206	C3216X7R2A474K	TDK
19	1	C29	100 pF 100V 10 % X7R 0805	08051C101JAT2A	AVX
20	1	C32	27 µF, ±20%, 100 V, Al Electrolytic, Gen. Purpose, Can, (8mm x 13mm)	EEU-FS2A270B	Panasonic
21	1	D1	400 V, 2 A, Superfast, 35 ns, DO-214A, SMB	ES2G-13-F	Diodes, Inc.
22	1	D2	Diode ULTRA FAST, GPP, 400 V, 1 A SMA	US1G-13-F	Diodes, Inc.
23	1	D3	Diode, SCHOTKY, 100 V, 0.075 A, SOD123	BAT46W-TP	Micro Commercial
24	1	D4	1000 V, 1 A, Ultrafast Recovery, GPP, DO-214AC SMA	US1M-13-F	Diode Inc.
25	1	D5	Diode ZENER 47 V 500 mW SOD123	MMSZ5261BT1G	ON Semi
26	2	D6 D8	Diode ZENER 24 V 500 mW SOD123	MMSZ5252BT1G	ON Semi
27	1	D7	Diode ZENER 5.6 V 500 mW SOD123	MMSZ5232B-7-F	Diodes, Inc.
28	1	F1	2 A, 250 V, Slow, TR5	37212000411	Wickman
29	1	J1	3 Position Terminal Block Header, Male Pins, Shrouded (4 Side), 0.200" (5.08 mm), Vertical Solder	EDSTLZ955/3	On Shore Tech
30	1	J2	4 Position Terminal Block Header, Male Pins, Shrouded (4 Side), 0.197" (5.00 mm), Vertical, Through Hole	691311700104	Würth
31	1	J3	5 Position Terminal Block Header, Male Pins, Shrouded (4 Side), 0.200" (5.08 mm), Vertical Solder	EDSTLZ955/5	On Shore Tech
32	1	J7	3 Position Terminal Block Header, Male Pins, Shrouded (4 Side), 0.295" (7.50 mm) 90°, Right Angle, Through Hole	1766356	Phoenix
33	1	L1	CMC, 3.3 mH @ 10 kHz, 2 Line Common Mode Choke, Through Hole, 1.8 A, DCR 140 mΩ (Typ)	B82731M2182A030	Epcos
34	1	L2	200 µH @ 100 kHz, Common Mode Choke	30-00512-00	Power Integrations
35	1	L3	10 µH, Unshielded Wirewound Inductor, 3.45 A, 15 mΩ Max, Radial, Vertical Cylinder	18R103C	Murata
36	1	Q1	MOSFET, N-Channel, 100 V, 69 A (Tc), 195 W (Tc), LFPAK56, Power-SO8, SC-100, SOT-669, SOT-669-4	PSMN015-100YL	Nexperia
37	1	Q2	MOSFET, N-Channel, 40 V, 36 A (Tc), 3.5 W (Ta), 7.8W (Tc), SMT, 8-SO	SI4154DY-T1-GE3	Vishay

38	2	R1 R2	RES, 22 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ220V	Panasonic
39	1	R3	NTC Thermistor, 10 Ω, 1.7 A	CL-120	Thermometrics
40	1	R4	RES, 10 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
41	3	R5 R12 R14	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
42	3	R6 R10 R46	RES, 0 Ω, 5%, 1/8 W, Thick Film, 0805	RMCF0805ZT0R00	Stackpole
43	2	R7 R8	RES, 750 kΩ, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J754V	Panasonic
44	1	R11	RES, 10 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF10R0V	Panasonic
45	2	R13 R33	RES, 47 Ω ±5% 1/8 W Chip Resistor 0805 Automotive AEC-Q200 Thick Film	RMCF0805JT47R0	Stackpole
46	1	R19	RES, 47.0 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF47R0V	Panasonic
47	1	R20	RES, 8.2 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ822V	Panasonic
48	1	R22	RES, 100 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
49	1	R23	RES, 4.53 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4531V	Panasonic
50	1	R24	RES, 10 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
51	1	R25	RES, 2 MΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2004V	Panasonic
52	4	R27 R43 R44 R45	RES, 1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
53	1	R32	RES, 10 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ100V	Panasonic
54	4	R34 R36 R37 R38	RES, 10 MΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ106V	Panasonic
55	1	R35	RES, 402 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4023V	Panasonic
56	1	T1	Bobbin, PQ20/16, Vertical, 14 pins.	BPQ20/16-1114CPFR	TDK
57	1	U1	InnoMux2-BL, InSOP-T24D	IMX2065C	Power Integrations
58	1	U2	Four-Channel LED Backlight Controller IC, SO-16	IML204DG	Power Integrations
59	1	VDR1	275 VAC, 45 J, 10 mm, RADIAL	V275LA10P	Littlefuse

8 Transformer (T1) Specification

8.1 Core Information

Cores B65875B series

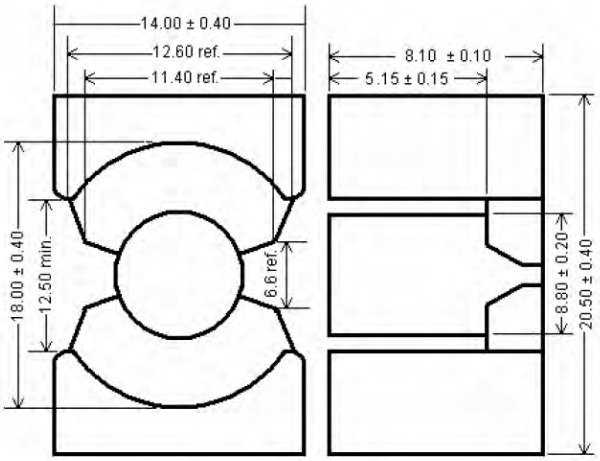
To IEC 62317-13

Delivery mode: sets

Magnetic characteristics (per set)

$\Sigma l/A$	= 0.579	mm^{-1}
l_e	= 37.0	mm
A_e	= 64.0	mm^2
A_{min}	= 57.6	mm^2
V_e	= 2367	mm^3

Approx. weight : 13.0 g/set



Dimensions in mm

Figure 11 – PQ20/16 Core.

8.2 Bobbin Information

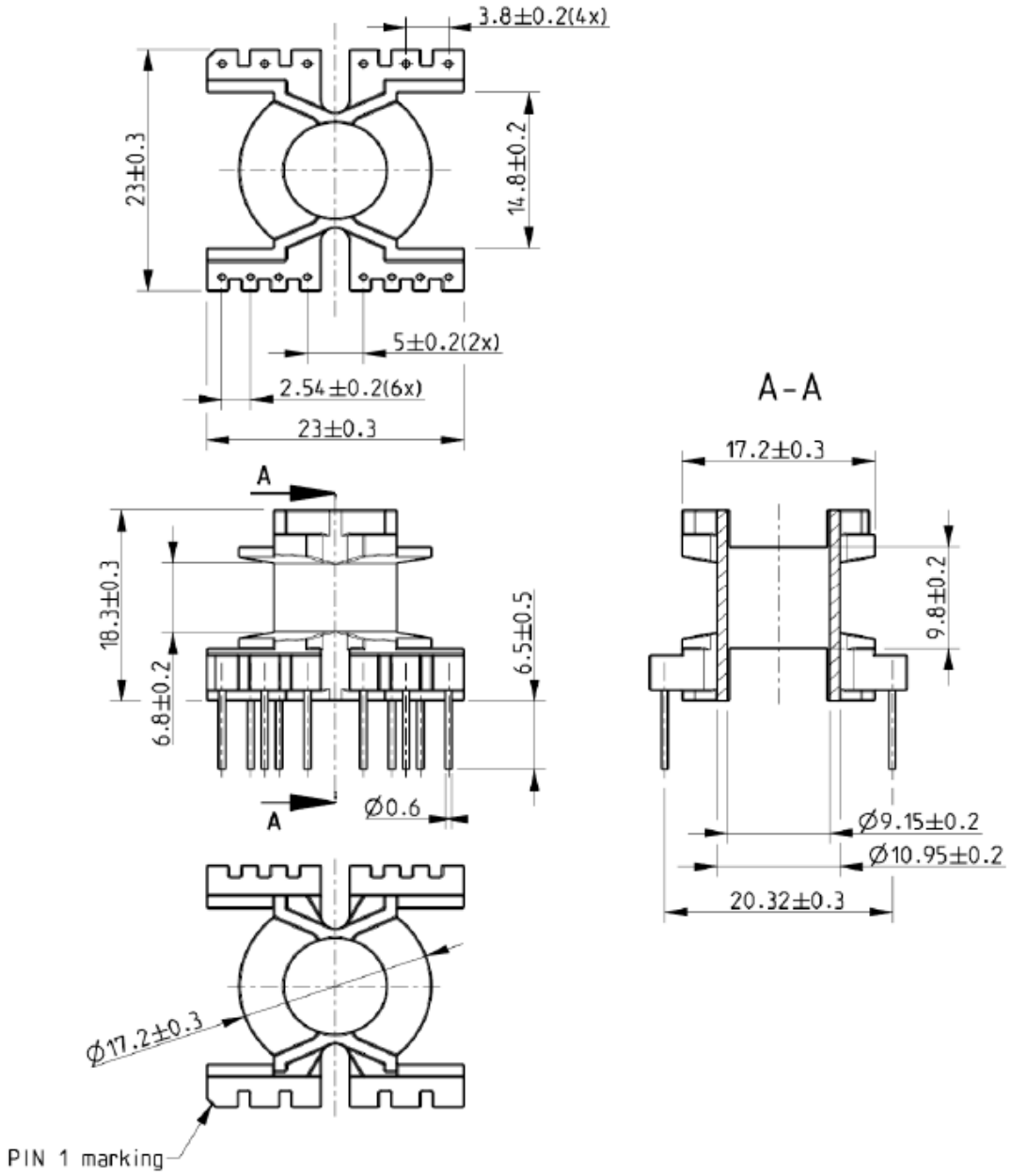


Figure 12 – PQ20/16 Coil Former.

8.3 Electrical Diagram

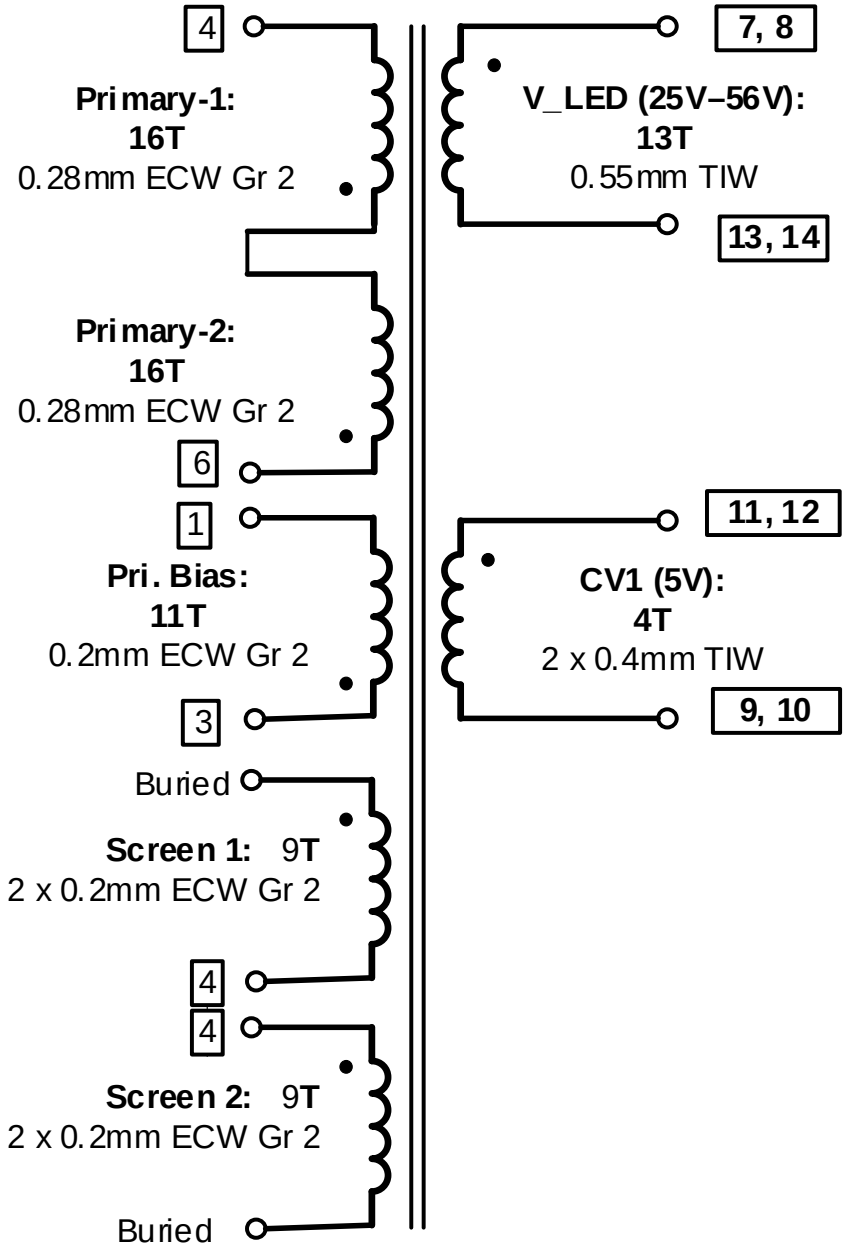


Figure 13 – Transformer Electrical Diagram.

8.4 Winding Stack Diagram

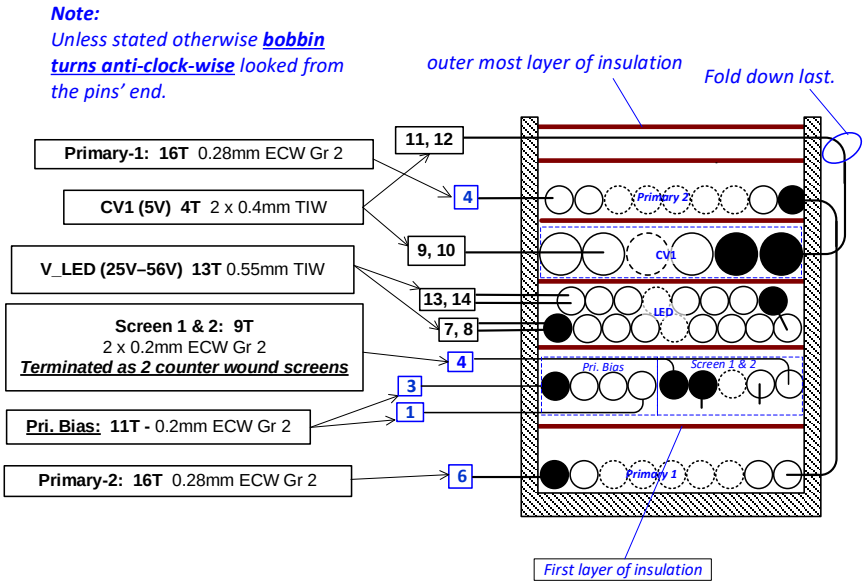


Figure 14 – Transformer Build Diagram.

8.5 Transformer Electrical Specification

Parameter	Condition	Spec.
Electrical strength	1 second, 60 Hz from pins 1-6 to 7-14.	3000 VAC
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 4 and 6, with all other windings open.	474 µH ±5%
Resonant Frequency	Between pin 4 and 6, other windings open.	1100 kHz (Min.)
Primary Leakage Inductance	Between pin 4 and 6, with all secondary 1, 3, 7, 8, 9, 10, 11, 12, 13, 14 are shorted.	6 µH (Max.)

Table 1 – Transformer Electrical Specification.

8.6 List of Materials

Item	Description	Quantities
[1]	Core: PQ 20/16.	2
[2]	Bobbin with Cover: PQ 20/16, 14 pins (6/8).	1
[3]	Magnet Wire: #29, Grade 2 ECW.	Primary-2
[4]	Magnet Wire: #32, Grade 2 ECW.	Primary Bias
[5]	TEX-E Wire: #26, Triple Insulated.	CV1
[6]	TEX-E Wire: #23, Triple Insulated.	VLED
[7]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 8 mm Wide.	
[8]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 9 mm Wide.	
[9]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 5 mm Wide.	
[10]	Varnish: Recommended, E962-A (alternative: Dolph BC-359).	20 cm
[11]	Glue: Recommended, H907 (alternative: Devcon 5-minute Epoxy).	5 ml
[12]	Core Clamp: CLMP/P-PQ20/16.	

Table 2 – Transformer Material List.

8.7 Transformer Construction

Layer 1 Primary-1	Start at pin 6, wind 16 turns of Item [3] in with tight tension. Terminate temporarily on the mandrel with an excess of ~2 meters of tape.
Insulation	Place 1 layer of tape Item [7] for insulation.
Layer 2 Primary Bias	Start at pin 3, wind 11 turns of wire Item [4] in 1/5 layer with tight tension and terminate at pin 1.
Layer 2 Screen: 1&2	Prepare 2 pcs of Item [4]. Mark one end of both wires with a tape to signify the dotted ends of the screen winding. Terminate the taped end of the first wire at pin 4. Bury the non-taped end of the other wire beside the primary bias winding. Wind 9 turns of the two pcs of wires together to fill the rest of the bobbin width. Bury the non-taped end of the first wire on the bobbin. Terminate the taped end of the second wire at pin 4.
Insulation	Place 1 layer of tape Item 7] for insulation.
Layer 3 LED	Start at pin 7 or 8, wind 13 turns of Item [6] with tension and temporarily tape the ending at the mandrel. Add 1 layer of tape, Item [7]. Fold down the wire and terminate the winding at pin 13 or 14.
Insulation	Place 1 layer of tape Item 7] for insulation.
Layer 4 CV1	Start at pin 9, wind 4 turns of 2 pcs of Item [5] in a clockwise direction when looked from pins' end. After the last turn, terminate the wire temporarily by taping an excess of around 5mm to the mandrel.
Insulation	Place 1 layer of tape Item [7] for insulation.
Layer 5 Primary-1	Remove the taped end of Primary-2 winding, Item [3] from the mandrel and wind 16 turns with tight tension terminating at pin 4.
Insulation	Place 1 layer of tape Item [7] for insulation.
CV1 Termination	Fold down the end of CV1 winding to the pins side and terminate at pin 11.
Insulation	Place 1 layer of tape Item [7] for insulation.
Gluing Process	Gap core to achieve a nominal inductance of 340 µH across the primary winding pins, 4 and 6. Make sure glue completely fills the air gap. Recommended glue, Item [11]. Secure core halves into the bobbin and tape core tightly using Item [8]. Secure core halves into the bobbin using Item [12]. Reinforce enclosure using around 55 cm of tape, Item [8]. Apply the tape leaving the bottom uncovered. Use a smaller width of tape, Item [9], wind another layer going through the bottom, in between the core clamp to completely seal the core. Measure inductance again since glue has different permeability than air. Apply glue on core legs on both top side and bottom side.
Finish Assembly	Dry in oven for 1 hour at 100 ºC temp. Vacuum impregnate varnish for 15-20 minutes to make sure varnish is well infiltrated. Recommended varnish, Item [10]. Dry in oven again for 1 hour at 100 ºC temperature. Label "DER715 XXX.X µH" (XXX.X = measured primary inductance value in µH) Varnish – Item [11].

Table 3 – Transformer Construction.

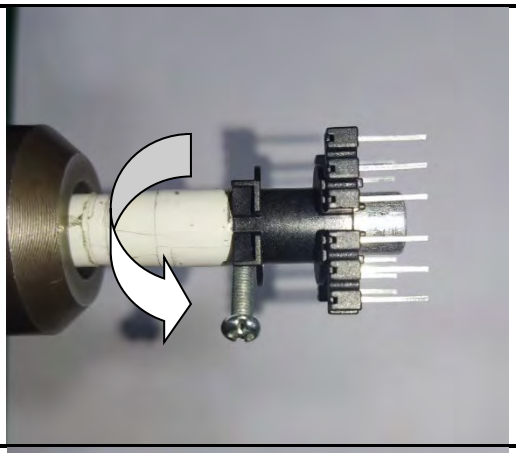
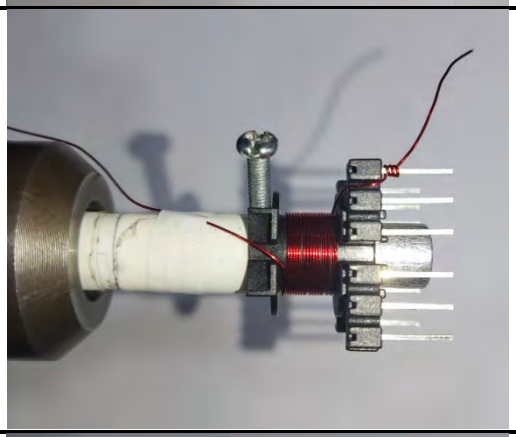
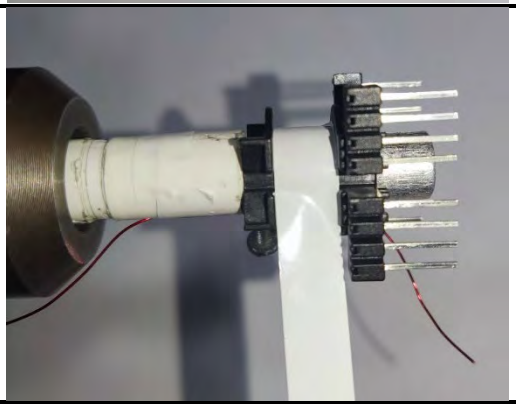
8.8 Transformer Test

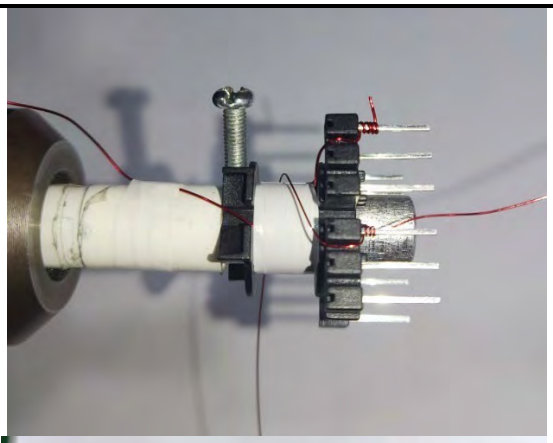
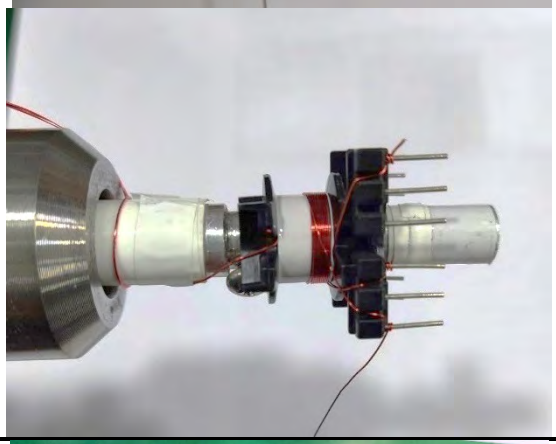
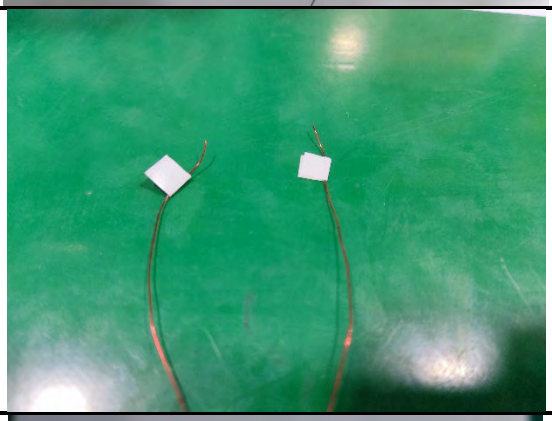
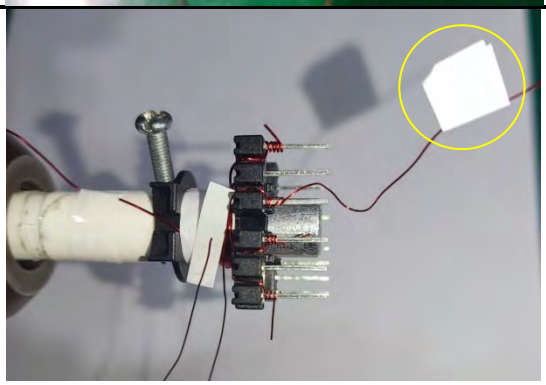
The winding measured inductance of the individual windings as well as the primary leakage inductance of the transformer are shown in the table below:

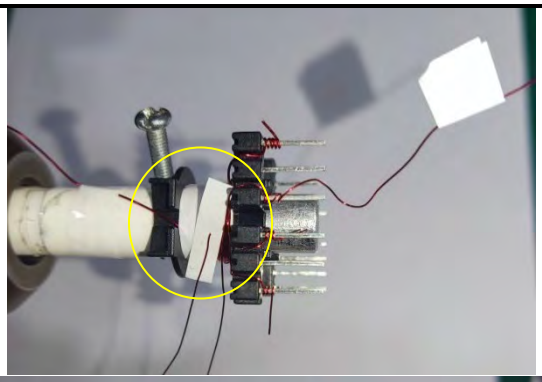
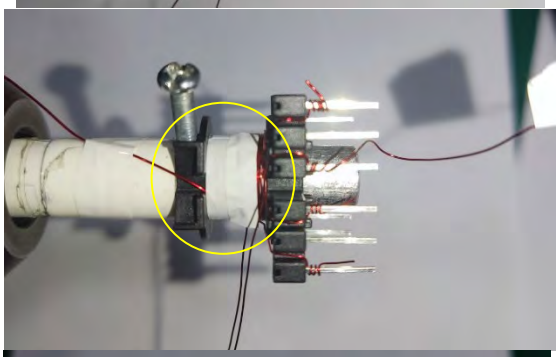
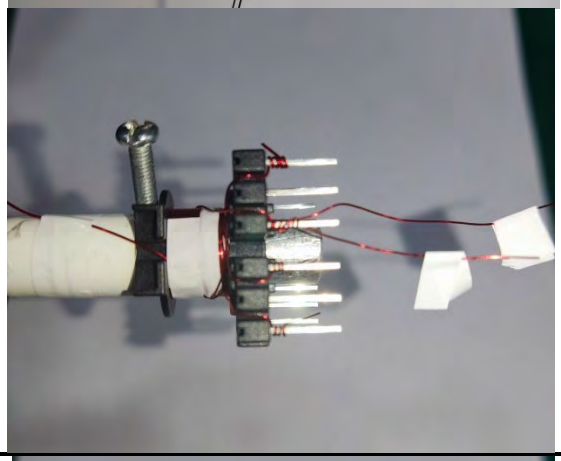
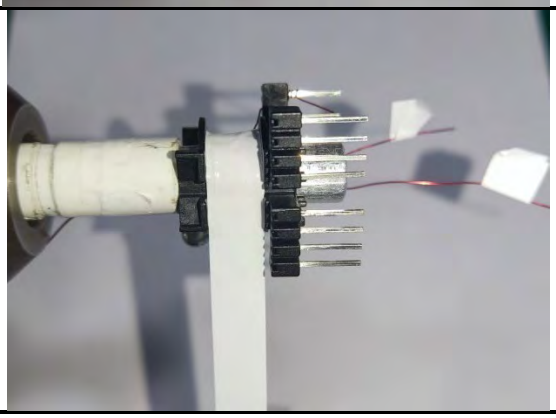
		Between Pins	Pins Shorted
Lpri [µH]	475	4 - 6	
LCV1 [µH]	7.67	9, 10 - 11, 12	
LLED [µH]	78.98	7, 8 - 13, 14	
Lpribias [µH]	57.4	1 - 3	
Llkgpri [µH]	3.08	4 - 6	1,3,7,8,9,10,11,12,13,14

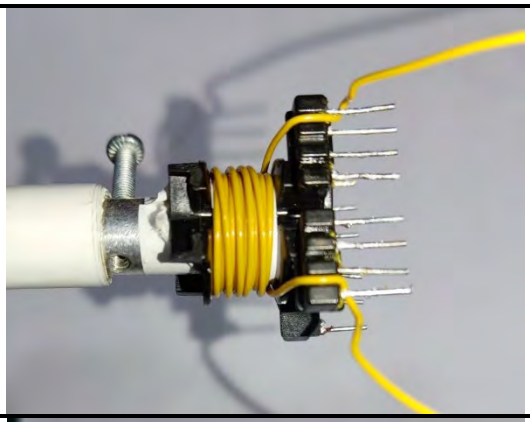
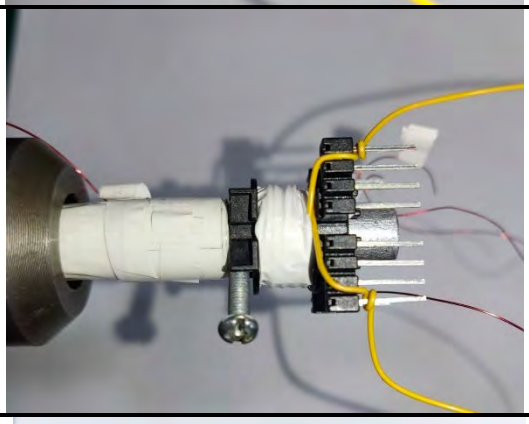
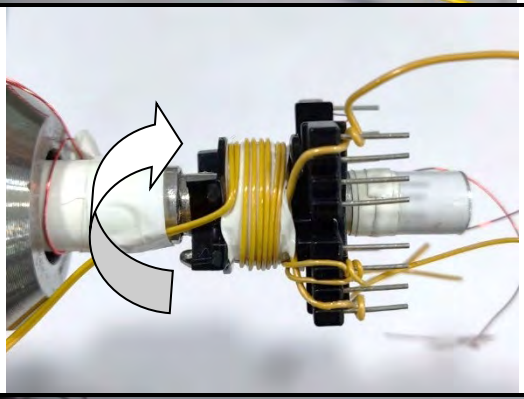
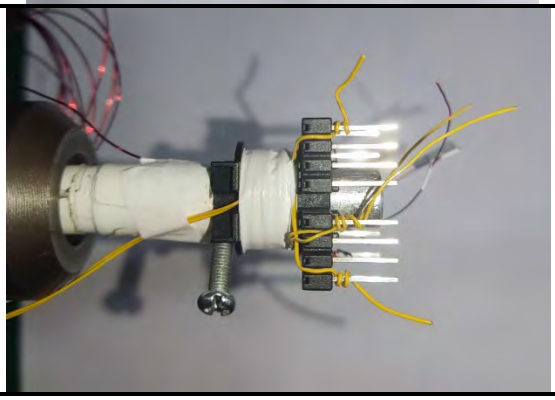
Table 4 – Winding Inductance. All Measurements Done with 100 kHz at 1 $V_{RMS.}$

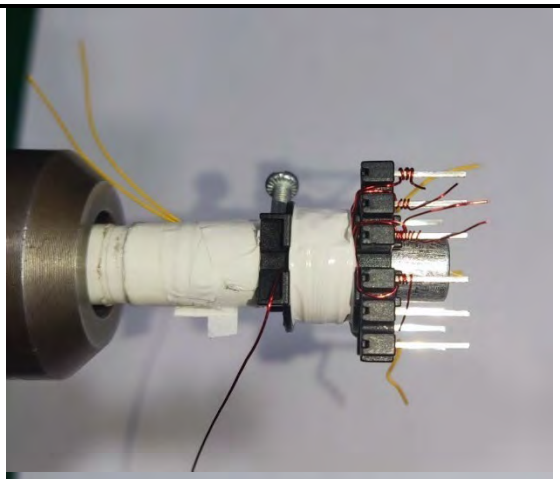
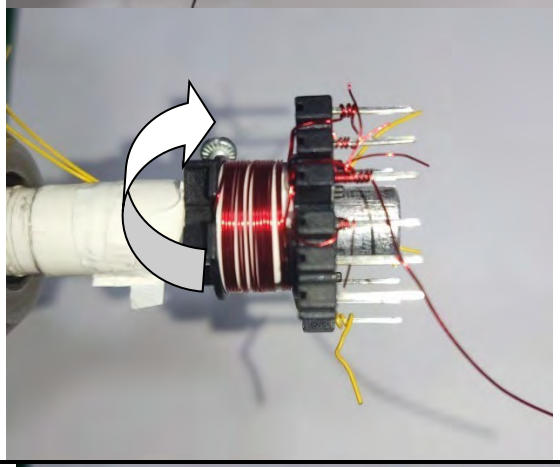
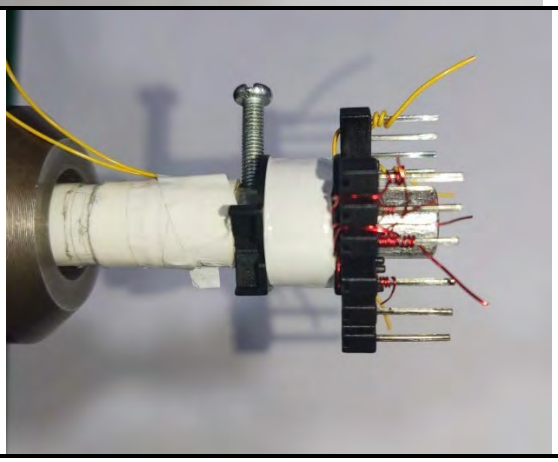
8.9 Winding Illustration

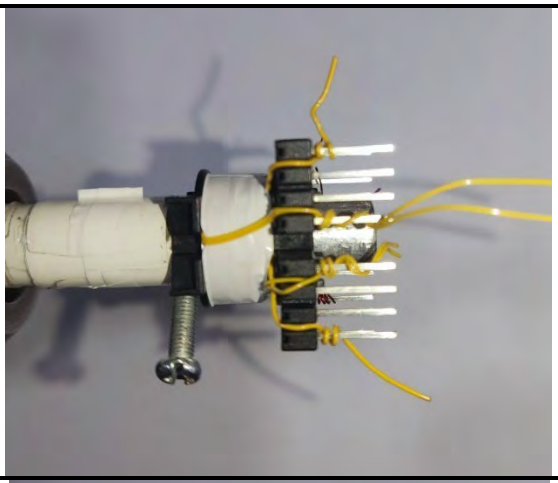
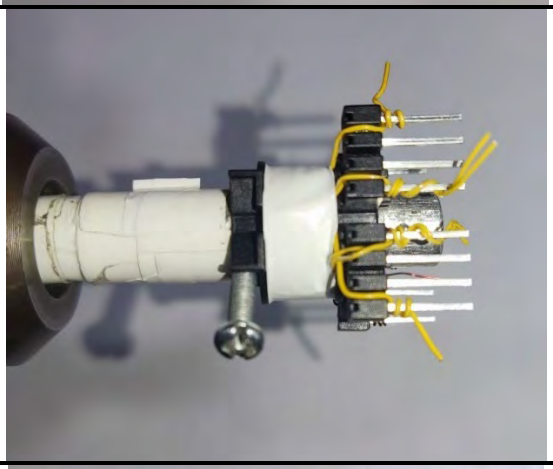
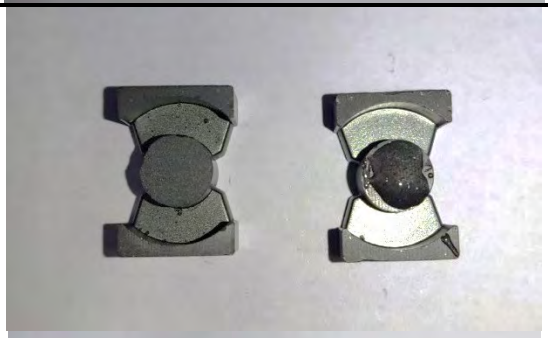
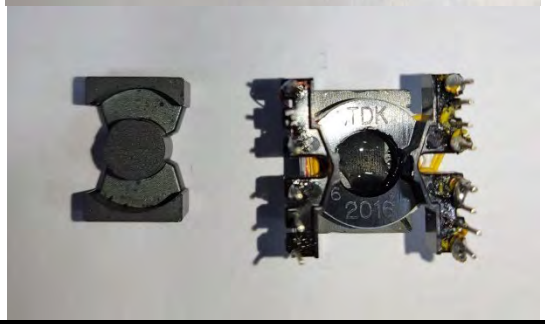
Winding Preparation		Place the bobbin on the mandrel with the pins' side facing to the right. Bobbin winding direction is anti-clockwise when looked from pins' end.
Primary-2		Start at pin 6, wind 16 turns of wire Item [3] in 1 layer, with normal tension from right to left. Terminate the winding temporarily on the mandrel using a piece of tape with an excess of around 2 meters. Do not cut off.
Insulation layer		Add 1 layer of tape Item [7].

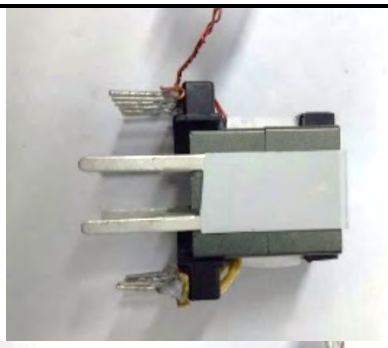
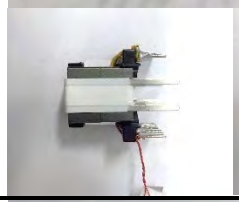
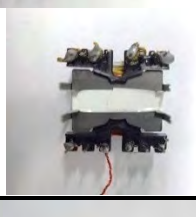
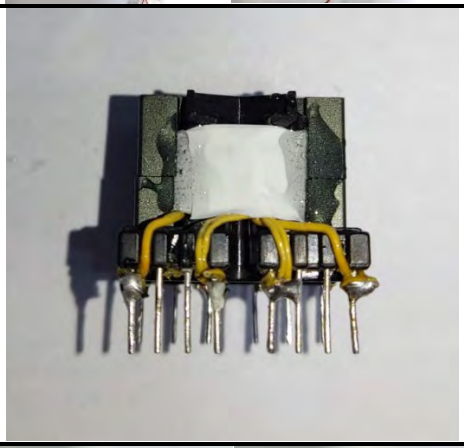
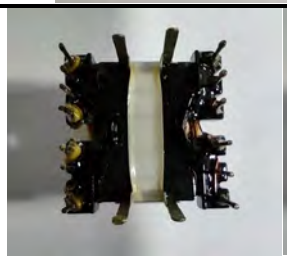
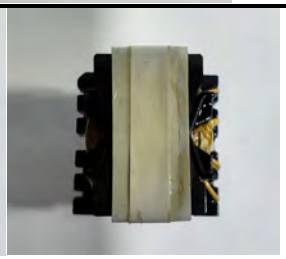
Primary Bias	 	Start at pin 3, wind 11 turns of Item [4] from right to left and terminate at pin 1.
Screen Winding 1 & 2		Prepare 2 pcs of Item [4]. Mark one end of both wires with a tape to signify the dotted ends of the screen winding.
Insulation layer		Terminate the taped end of the first wire at pin 4. Bury the non-taped end of the other wire beside the primary bias winding using a small piece of tape.

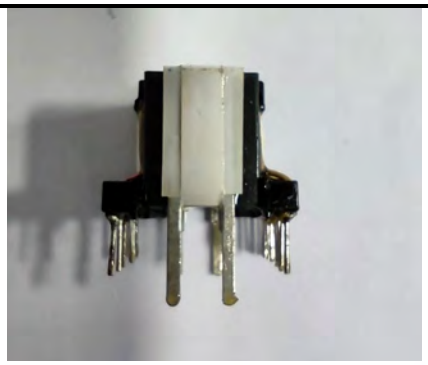
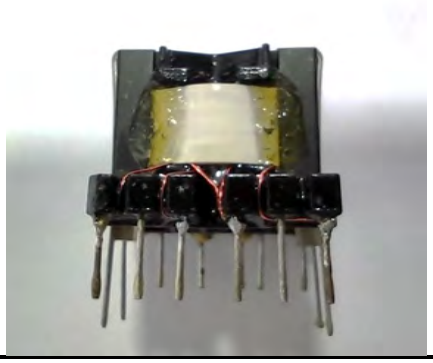
	  	Wind 9 turns of the two pieces of wires together. Bury the non-taped end of the first wire on the body of the bobbin. Terminate the taped end of the second wire at pin 4.
Insulation Layer		Add 1 layer of tape, Item [7].

V_LED winding		Start at pin 7 or 8, wind 13 turns of Item [6] Terminate the winding at pin 13 or 14.
Insulation Layer		Add 1 layer of tape, Item [7].
CV1 winding		Start at pin 9, wind 4 turns of 2 pcs of Item [5] in a clockwise direction when looked from pins' end. After the last turn, terminate the wire temporarily on the mandrel by taping an excess of around 5mm to the mandrel.
Insulation Layer		Add 1 layer of tape, Item [7].

Primary-1	 	Remove the taped end of Primary-2 winding, Item [3] from the mandrel and wind 16 turns from left to right terminating at pin 4.
Insulation Layer		Add 1 layer of tape, Item [7].

CV1 Termination		Fold down the end of CV1 winding to the pins' side and terminate at pin 11.
Insulation Layer		Add 1 layer of tape, Item [7].
Gluing Process (1) **Central Leg Gluing**	 	Gap core to achieve a nominal inductance of 474 µH across the primary winding pins, 4 and 6. Make sure the glue completely fills the air gap. Recommended glue, Item [11].

Gluing Process (2)	   	Secure core halves into the bobbin using Item [12]. Then reinforce the enclosure using around 55 cm of tape, Item [8]. Apply the tape on one side going through the top of the transformer onto the other side leaving the bottom uncovered. Use a smaller width of tape, Item [9], wind another layer going through the bottom, in between the core clamp to completely seal the core. Measure inductance again since glue has different permeability than air.
Gluing Process (3)		Apply glue on core legs on both sides.
Finish Assembly	 	Cure under room temp for 1 day or in oven for 30 minutes. Vacuum impregnate varnish for 30 minutes to make sure varnish is well infiltrated. Recommended varnish, Item [10].

	 	Dry in oven for 30 minutes at 100 ºC temp. Label “DER715 XXX.X µH” (XXX.X = measured primary inductance value in µH)

9 Performance

9.1 Full Load Efficiency vs. Line

The full load efficiency vs. line measurements are shown below. These were obtained for all combinations of:

- All nominal line voltages (90 V, 115 V, 230 V, 265 V)
- LED =
  - 34 V @ 400 mA
  - 45 V @ 400 mA
  - 56 V @ 320 mA
- CV1 = 5 V @ 1.2 A

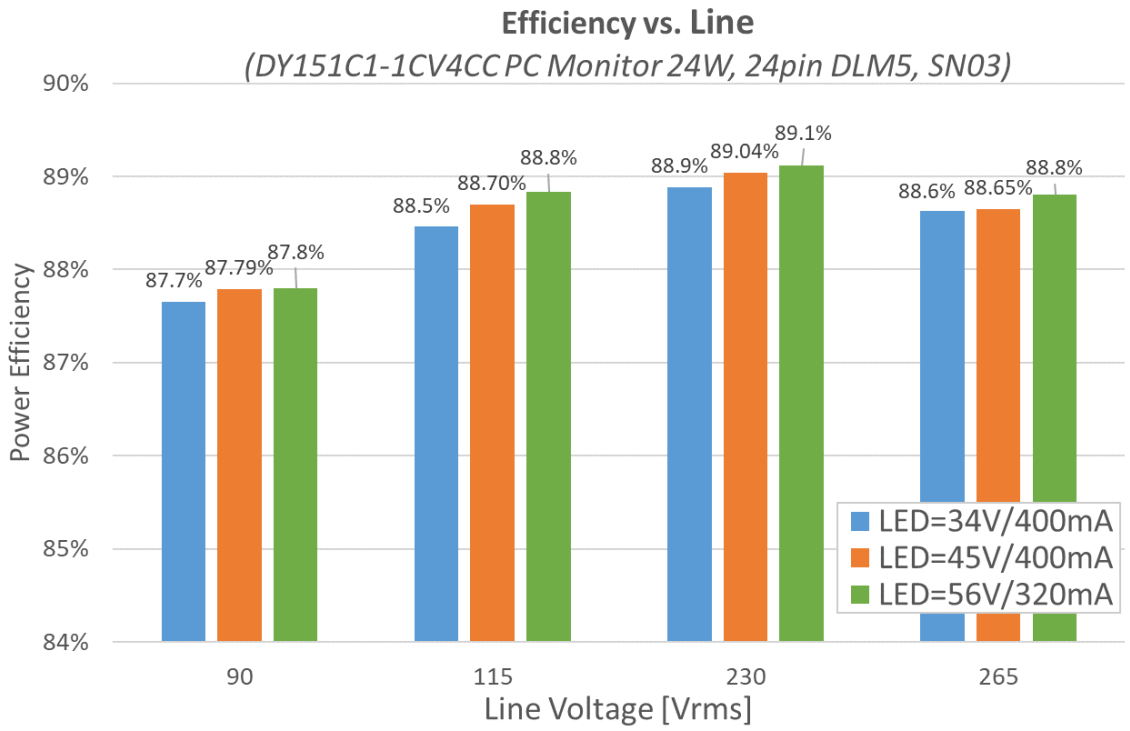


Figure 15 – Full Power Efficiency vs. Line Voltage at Room Temperature.

9.2 Efficiency vs. Load

The efficiency vs. load measurements is shown below. These were obtained for all combinations of:

- All nominal line voltages (90 V, 115 V, 230 V, 265 V)
- LED current of 20 mA, 30 mA, ……, 400 mA (11 points from 5% to 95% dimming duty)
- CV1 output current 0, 0.2 A, 0.4 A, ……, 2 A (11 points from 0 to 100% of CV1 load)

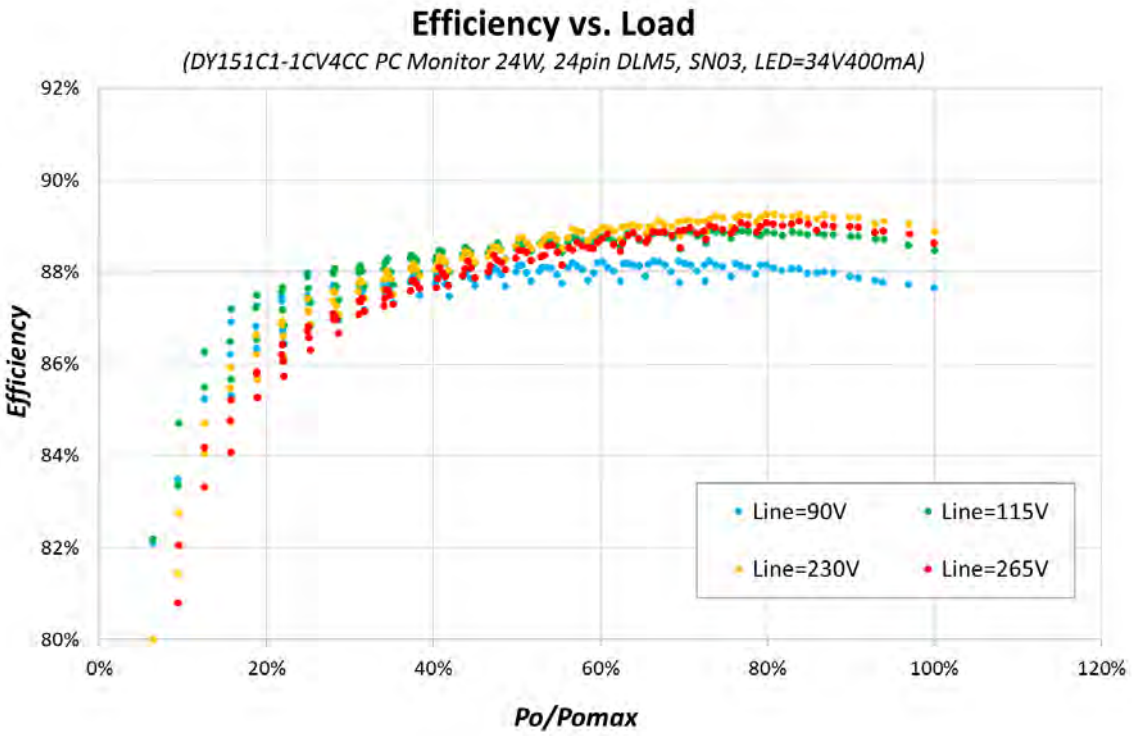


Figure 16 – Efficiency vs. Load for All Input Line Voltages, V_{LED} 34 V, Room Temperature.

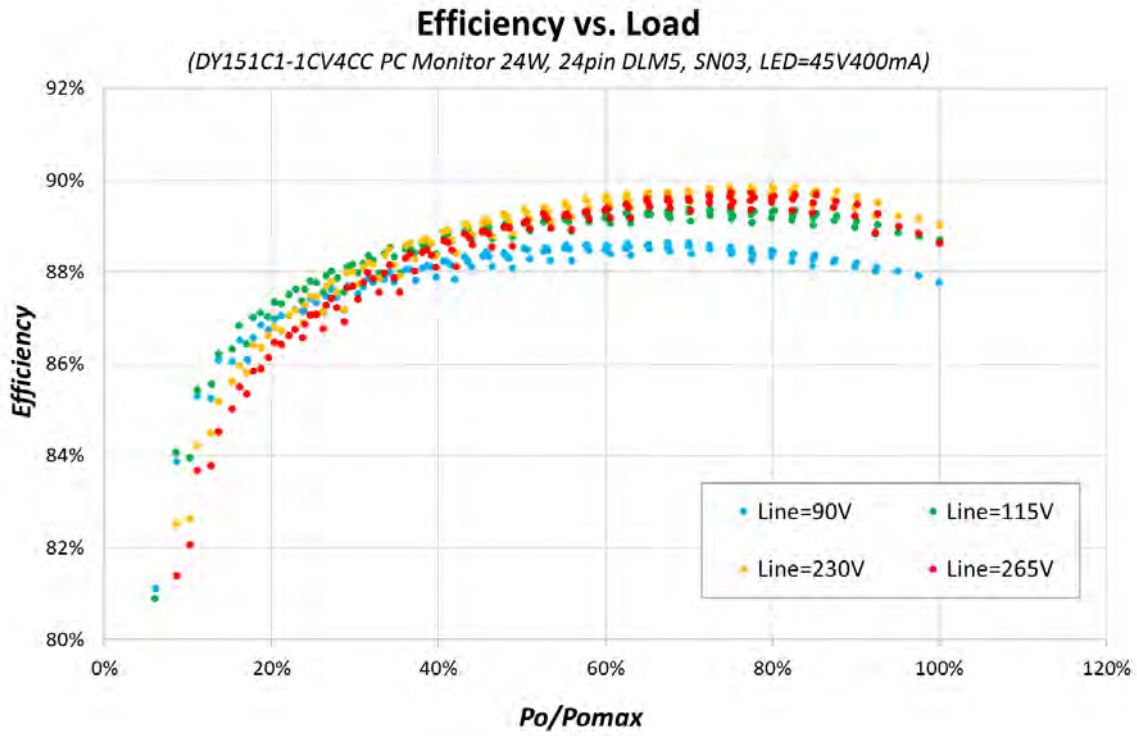


Figure 17 – Efficiency vs. Load for All Input Line Voltages, V_{LED} 45 V, Room Temperature.

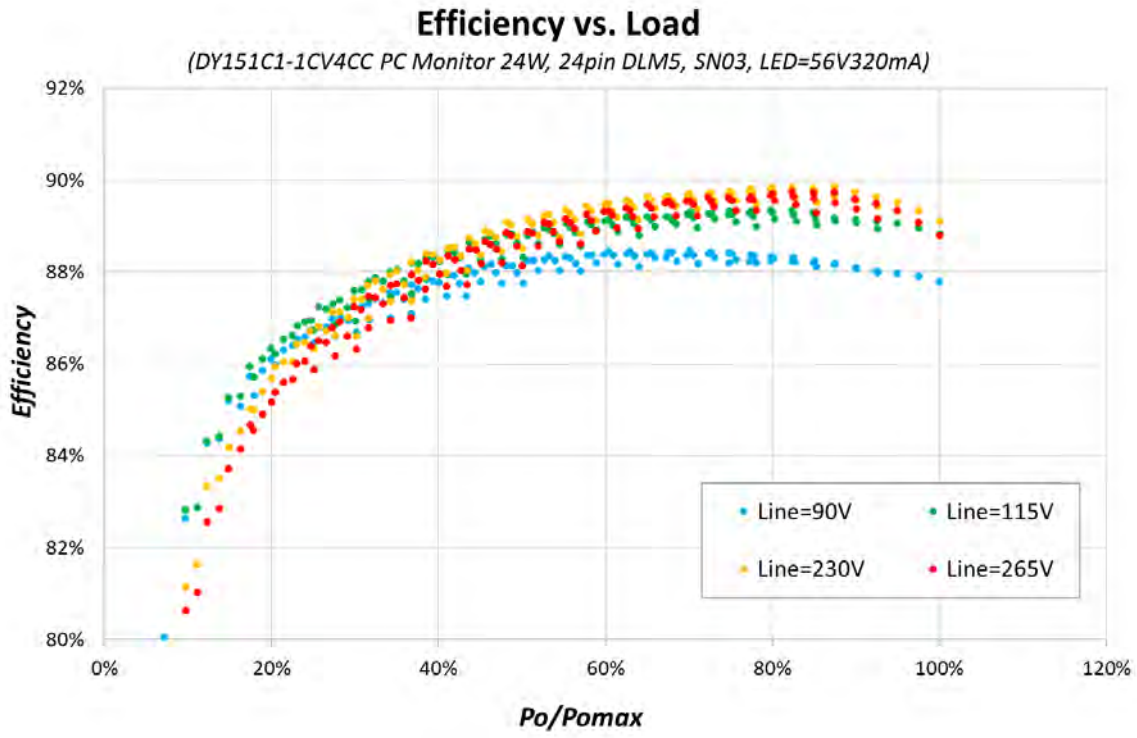


Figure 18 – Efficiency vs. Load for All Input Line Voltages, V_{LED} 56 V, Room Temperature.

9.3 Output Load Regulation

The output voltage regulation error vs. load measurements are shown below. These were obtained for all combinations of:

- All nominal line voltages (90 V, 115 V, 230 V, 265 V)
- LED current of 20 mA, 30 mA, ……, 400 mA (11 points from 5% to 95% dimming duty)
- CV1 output current 0, 0.2 A, 0.4 A, ……, 2 A (11 points from 0 to 100% of CV1 load)

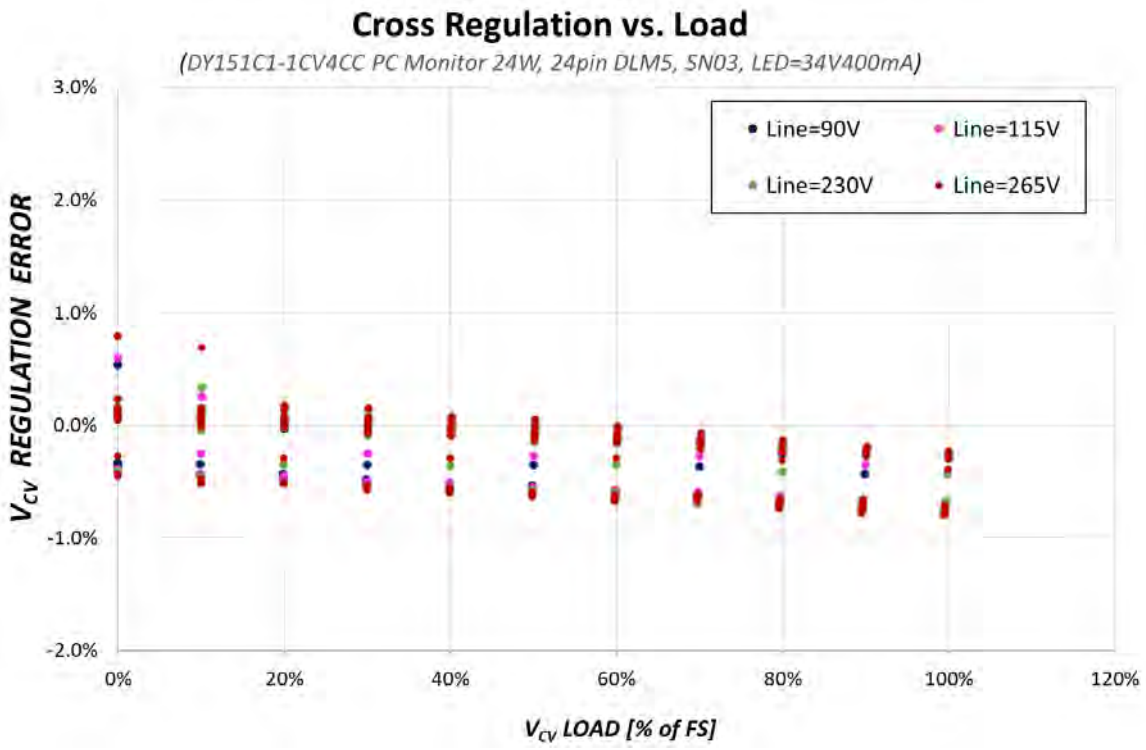


Figure 19 – CV1 Output Voltage Error vs. Line, V_{LED} 34 V, Room Temperature.

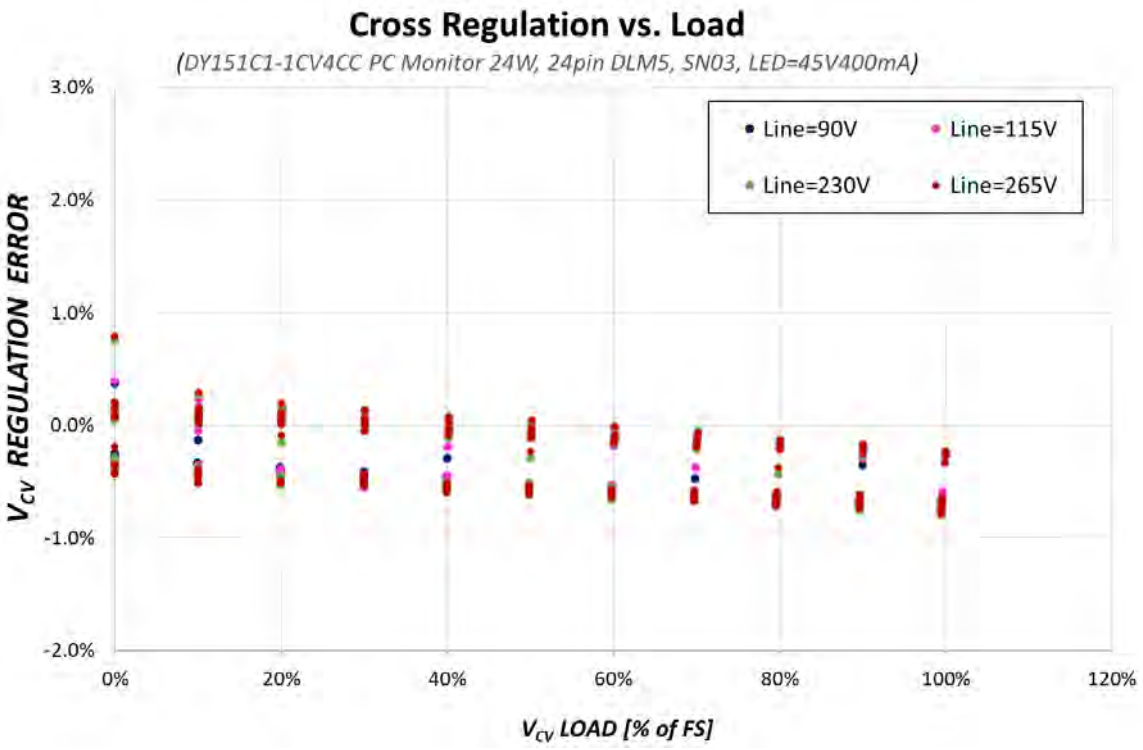


Figure 20 – CV1 Output Voltage Error vs. Line, V_{LED} 45 V, Room Temperature.

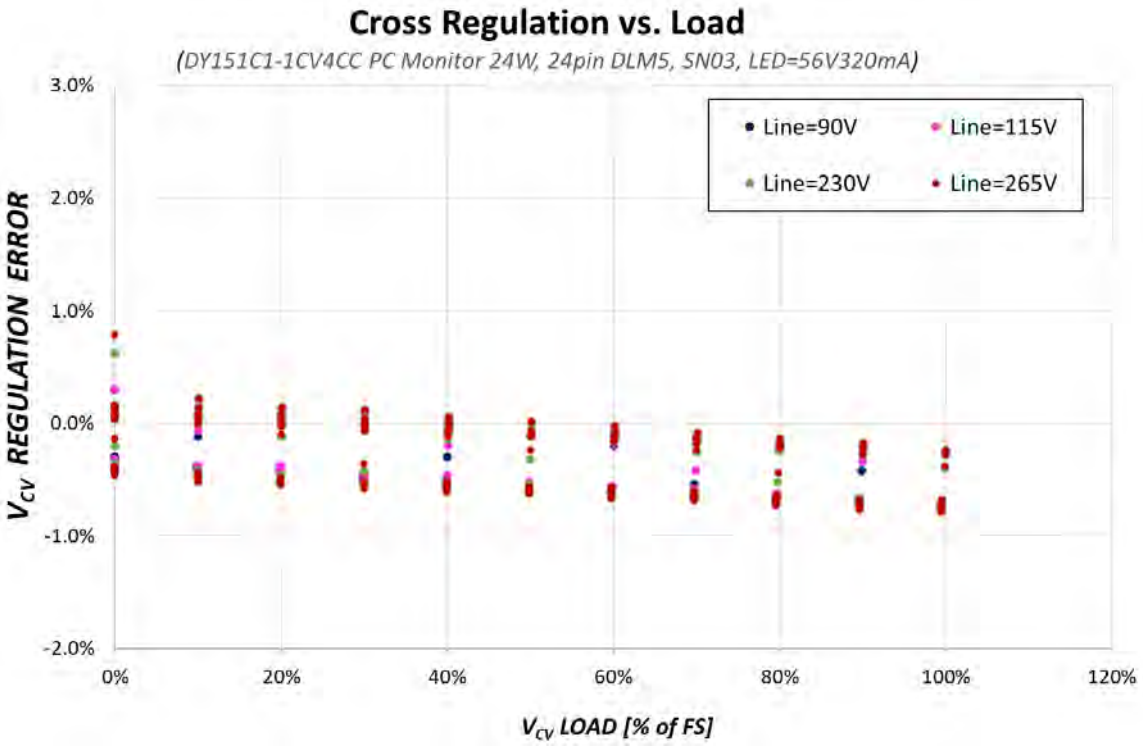


Figure 21 – CV1 Output Voltage Error vs. Line, V_{LED} 56 V, Room Temperature.

9.4 Standby Input Power (All LED Strings Disabled)

The output power vs. input power at standby mode measurements are shown below. These were obtained for all combinations of:

- All nominal line voltages (90 V, 115 V, 230 V, 265 V)
- LED output disabled
- CV1 output 0 mW ~ 300 mW

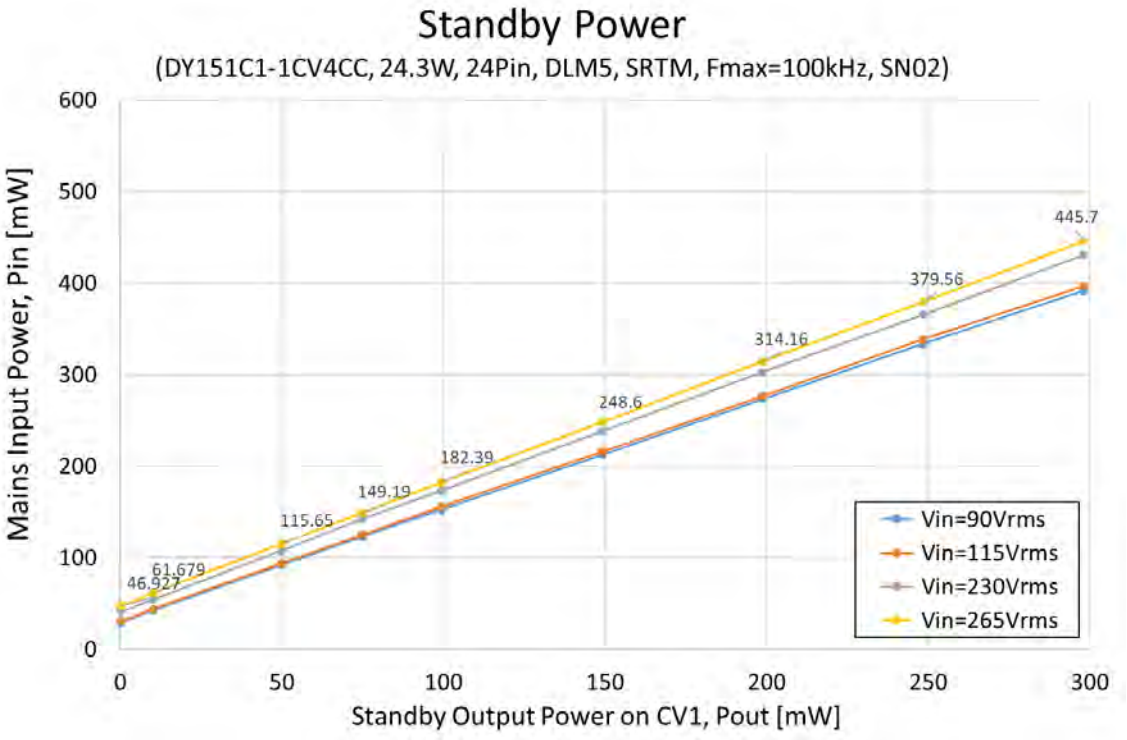


Figure 22 – Standby Power Consumption vs. Line Voltage, Room Temperature.

9.5 LED Dimming

9.5.1 LED Dimming Linearity

This PSU is configured with filtered PWM dimming mode. The dimming PWM duty vs. LED current linearity measurements are shown below. These were obtained for all combinations of:

- All nominal line voltages (90 V, 115 V, 230 V, 265 V)
- LED current of 20 mA, 30 mA, ……, 400 mA (11 points from 5% to 95% dimming duty)
- CV1 output current 0, 0.2 A, 0.4 A, ……, 2 A (11 points from 0 to 100% of CV1 load)

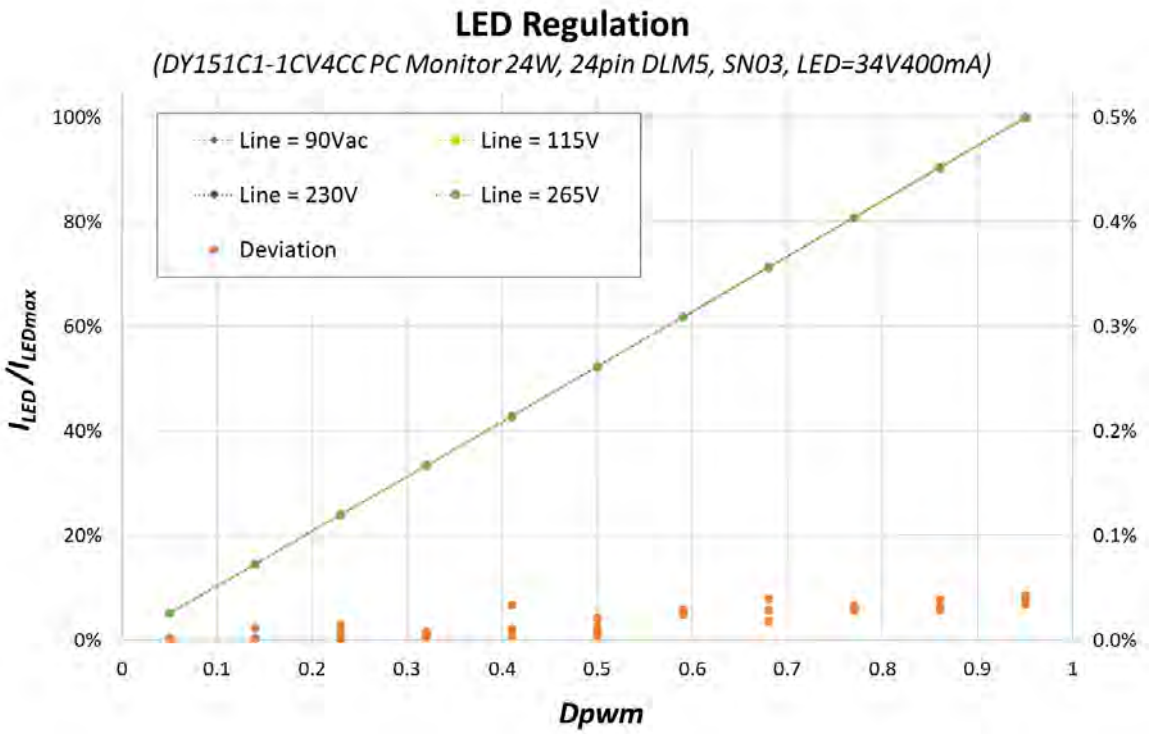


Figure 23 – LED Current Regulation vs. Dimming Duty, V_{LED} 34 V, Room Temperature.

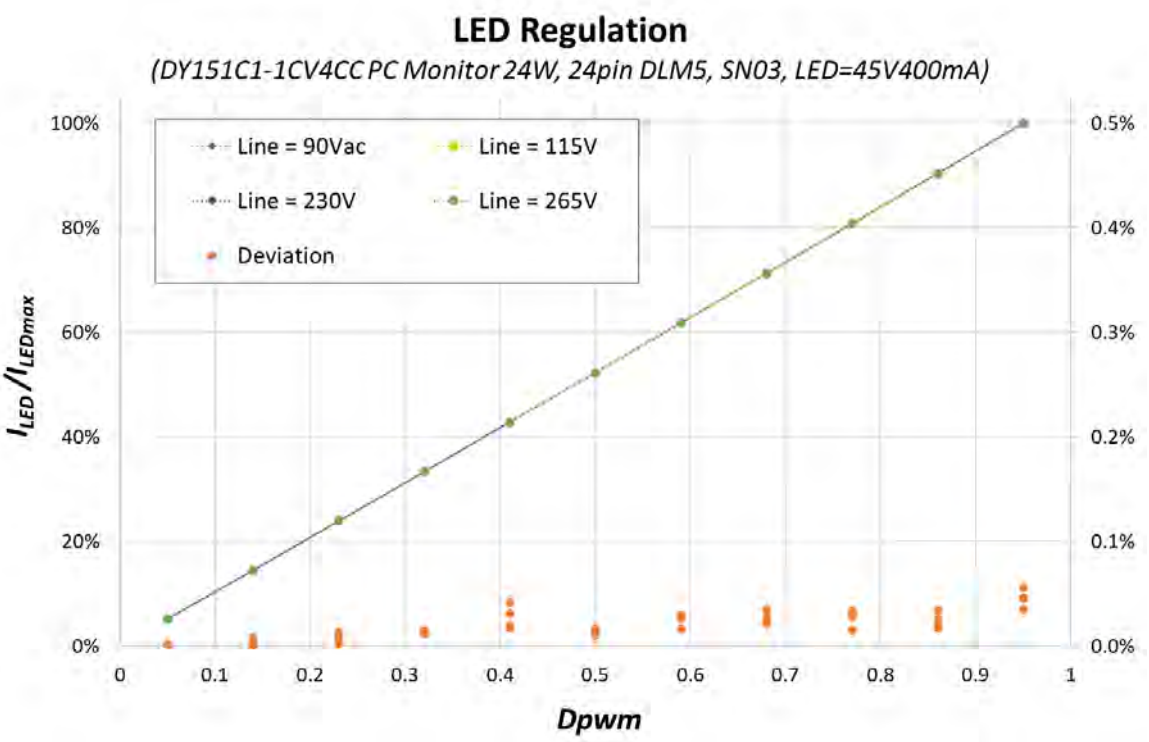


Figure 24 – LED Current Regulation vs. Dimming Duty, V_{LED} 45 V, Room Temperature.

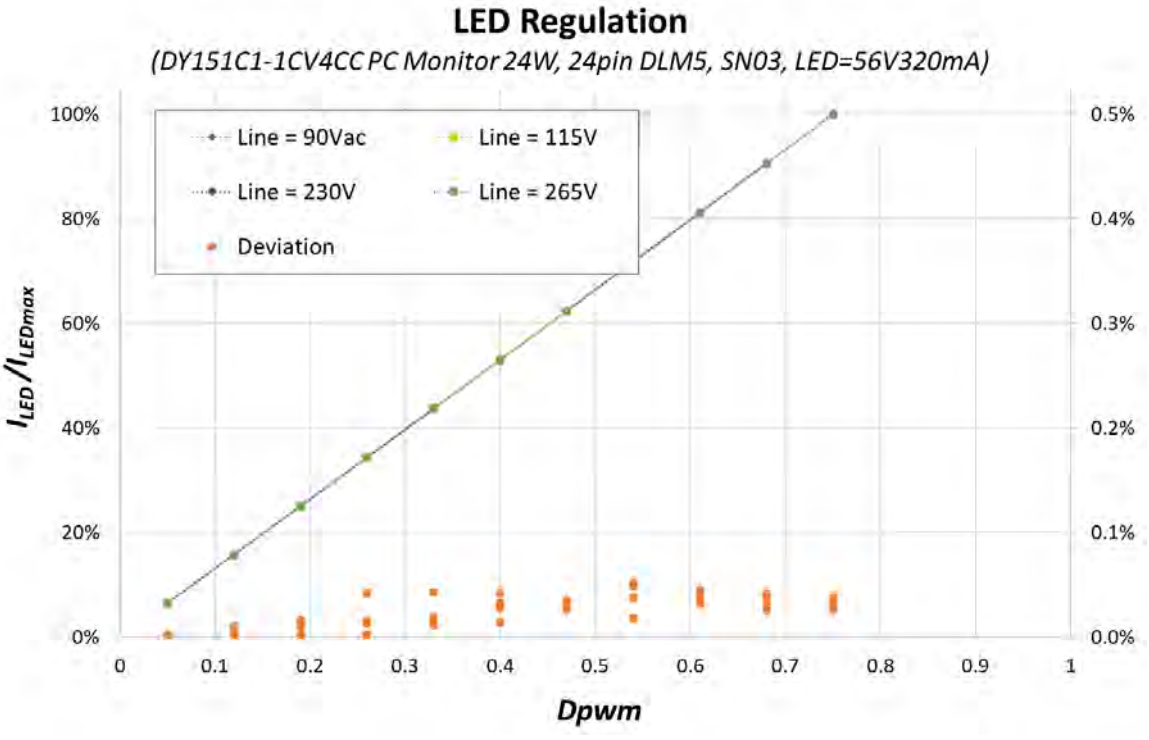


Figure 25 – LED Current Regulation vs. Dimming Duty, V_{LED} 56 V, Room Temperature.

9.5.2 LED Current Matching Accuracy

The dimming PWM duty vs. LED current matching error measurements are shown below. These were obtained for all combinations of:

- Nominal line voltages (115 V, 230 V)
- LED = 45 V string from 3.5 mA to 100 mA per string
- CV1 = 5 V @ 1.2 A

The current matching error is calculated using below formula:

$$\Delta = \frac{I_{MAX} - I_{MIN}}{2 \times I_{AVE}} \times 100\%$$

Where I_{MAX} is maximum current in all four strings,
I_{MIN} is the minimum current in all four strings,
I_{AVE} is the average current of all four strings.

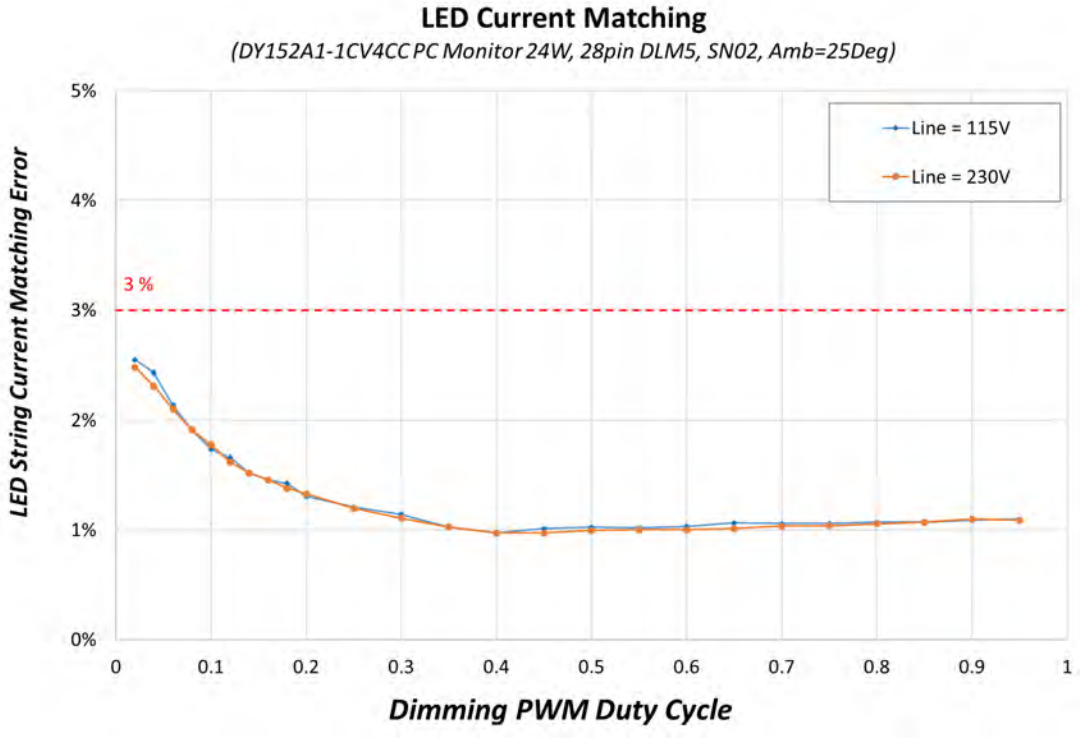


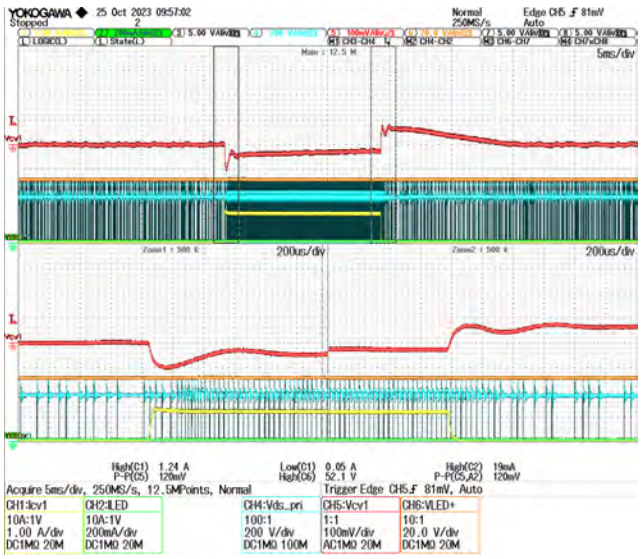
Figure 26 – LED Current Matching Error vs. Dimming Duty, V_{LED} 45 V, Room Temperature.

9.6 Load Transient Response

9.6.1 CV1 Step Load Transient Response

The load transient test was performed on power supply covering below test conditions:

- Line input voltage 265 V
- LED strings with below load combinations
  - 56 V, current of 16.5 mA, 82.5 mA, 165 mA, 330 mA (4%, 20%, 39% and 78% dimming duty)
  - 45 V, current of 25 mA, 100 mA, 200 mA, 400 mA (6%, 24%, 47% and 94% dimming duty)
  - 29 V, current of 25 mA, 100 mA, 200 mA, 400 mA (6%, 24%, 47% and 94% dimming duty)
- CV1 load step from 20 mA to 1.2 A and back to 20 mA



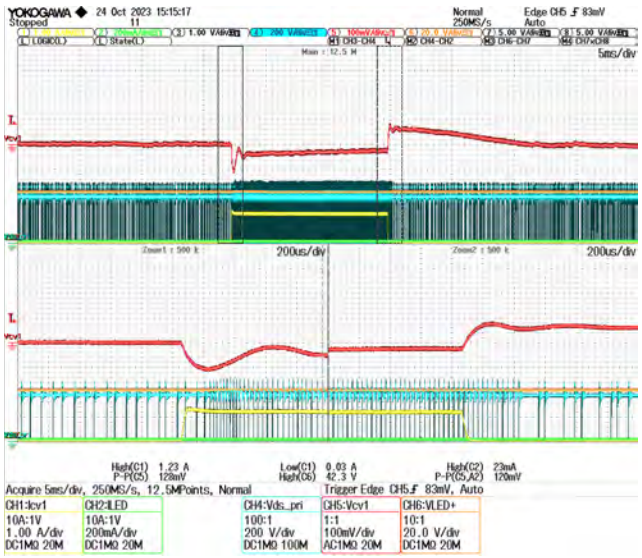
265 VAC, ICV1 = 20 mA -> 1.2 A -> 20 mA;
VLED = 56 V, ILED = 16.5 mA;
Overshoot 120 mV (2.4%); Undershoot 120 mV (2.4%).

265 VAC, ICV1 = 20 mA -> 1.2 A -> 20 mA;
VLE = 56 V, ILED = 82.5 mA;
Overshoot 125 mV (2.5%); Undershoot 118 mV (2.4%).

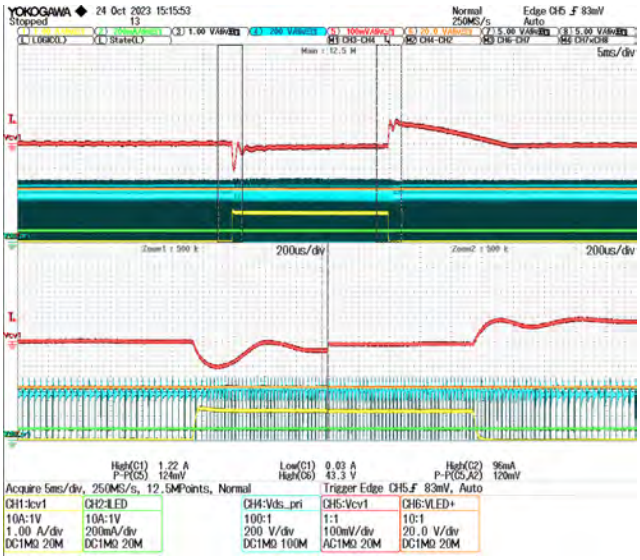
265 VAC, ICV1 = 20 mA -> 1.2 A -> 20 mA;
VLED = 56 V, ILED = 165 mA;
Overshoot 154 mV (3.1%); Undershoot 124 mV (2.5%).

265 VAC, ICV1 = 20 mA -> 1.2 A -> 20 mA;
VLED = 56 V, ILED = 330 mA;
Overshoot 159 mV (3.2%); Undershoot 128 mV (2.6%).

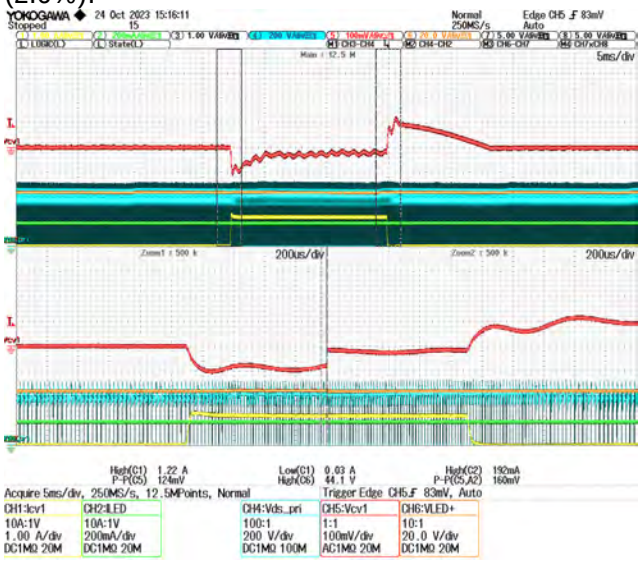
Figure 27 – 56 V LED String, CV1 (5 V) Load Transient Response.



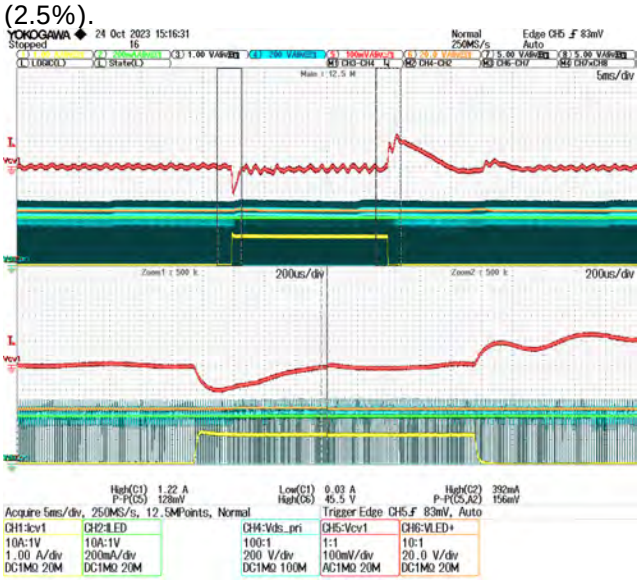
265 VAC, ICV1 = 20 mA -> 1.2 A -> 20 mA;
VLED = 45 V, ILED = 25 mA;
Overshoot 120 mV (2.4%); Undershoot 128 mV (2.6%).



265 VAC, ICV1 = 20 mA -> 1.2 A -> 20 mA;
VLED = 45 V, ILED = 100 mA;
Overshoot 120 mV (2.4%); Undershoot 124 mV (2.5%).



265 VAC, ICV1 = 20 mA -> 1.2 A -> 20 mA;
VLED = 45 V, ILED = 200 mA;
Overshoot 160 mV (3.2%); Undershoot 124 mV (2.5%).



265 VAC, ICV1 = 20 mA -> 1.2 A -> 20 mA;
VLED = 45 V, ILED = 400 mA;
Overshoot 156 mV (3.1%); Undershoot 128 mV (2.6%).

Figure 28 – 45 V LED String, CV1 (5 V) Load Transient Response.

265 VAC, ICV1 = 20 mA -> 1.2 A -> 20 mA;
VLED = 29 V, ILED = 25 mA;
Overshoot 120 mV (2.4%); Undershoot 120 mV (2.4%).

265 VAC, ICV1 = 20 mA -> 1.2 A -> 20 mA;
VLED = 29 V, ILED = 100 mA;
Overshoot 119 mV (2.4%); Undershoot 120 mV (2.4%).

265 VAC, ICV1 = 20 mA -> 1.2 A -> 20 mA;
VLED = 29 V, ILED = 200 mA;
Overshoot 144 mV (2.9%); Undershoot 120 mV (2.4%).

265 VAC, ICV1 = 20 mA -> 1.2 A -> 20 mA;
VLED = 29 V, ILED = 400 mA;
Overshoot 156 mV (3.1%); Undershoot 136 mV (2.7%).

Figure 29 – 29 V LED String, CV1 (5 V) Load Transient Response.

9.7 Switching Waveforms

9.7.1 Primary Switch Maximum Voltage Waveform

The primary switch maximum voltage test was performed on power supply covering below test conditions:

- Line input voltage 380 VDC (equivalent of the peak voltage of 265 VAC)
- Full load on both outputs:
  - LED = 56 V @ 330 mA
  - CV1 = 5 V @ 1.2 A

Figure 30 – Primary Switch Worst Case Peak Voltage ($V_{DS(PK)}$ = 552 V).

9.7.2 SR FET Voltage Waveform

The SR FET maximum voltage test was performed on power supply covering below test conditions:

- 265 VAC input line voltage
- Full load on both outputs:
  - LED = 56 V @ 330 mA
  - CV1 = 5 V @ 1.2 A

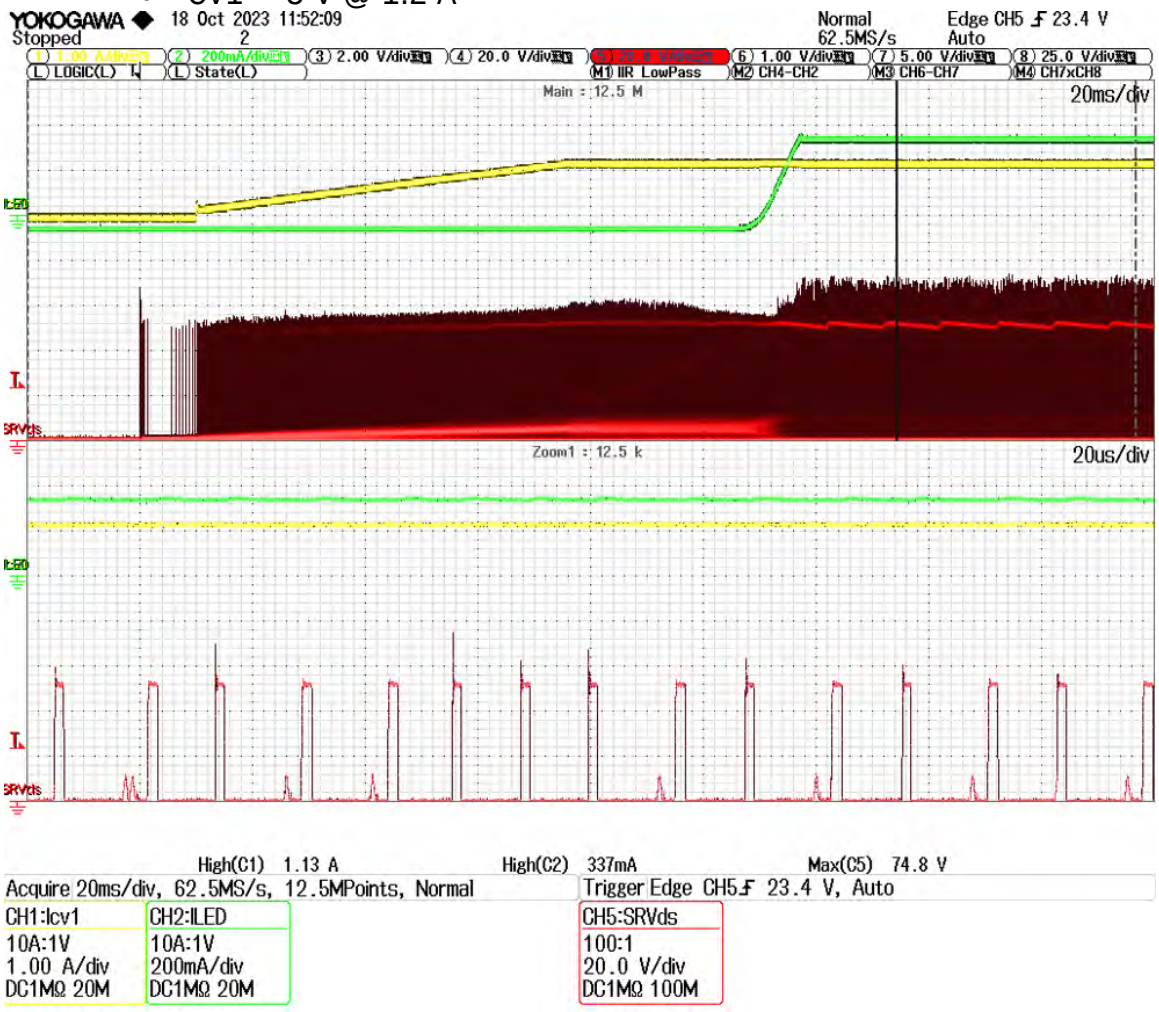


Figure 31 – SR FET Worst Case Peak Voltage ($V_{(SR\_DS\_PK)}$ = 74.8 V).

9.7.3 Selection FET Voltage Waveform

The Selection FET (Q2) maximum voltage test was performed on power supply covering below test conditions:

- 90 VAC input line voltage
- Full load on both outputs:
  - LED = 56 V @ 330 mA
  - CV1 = 5 V @ 1.2 A

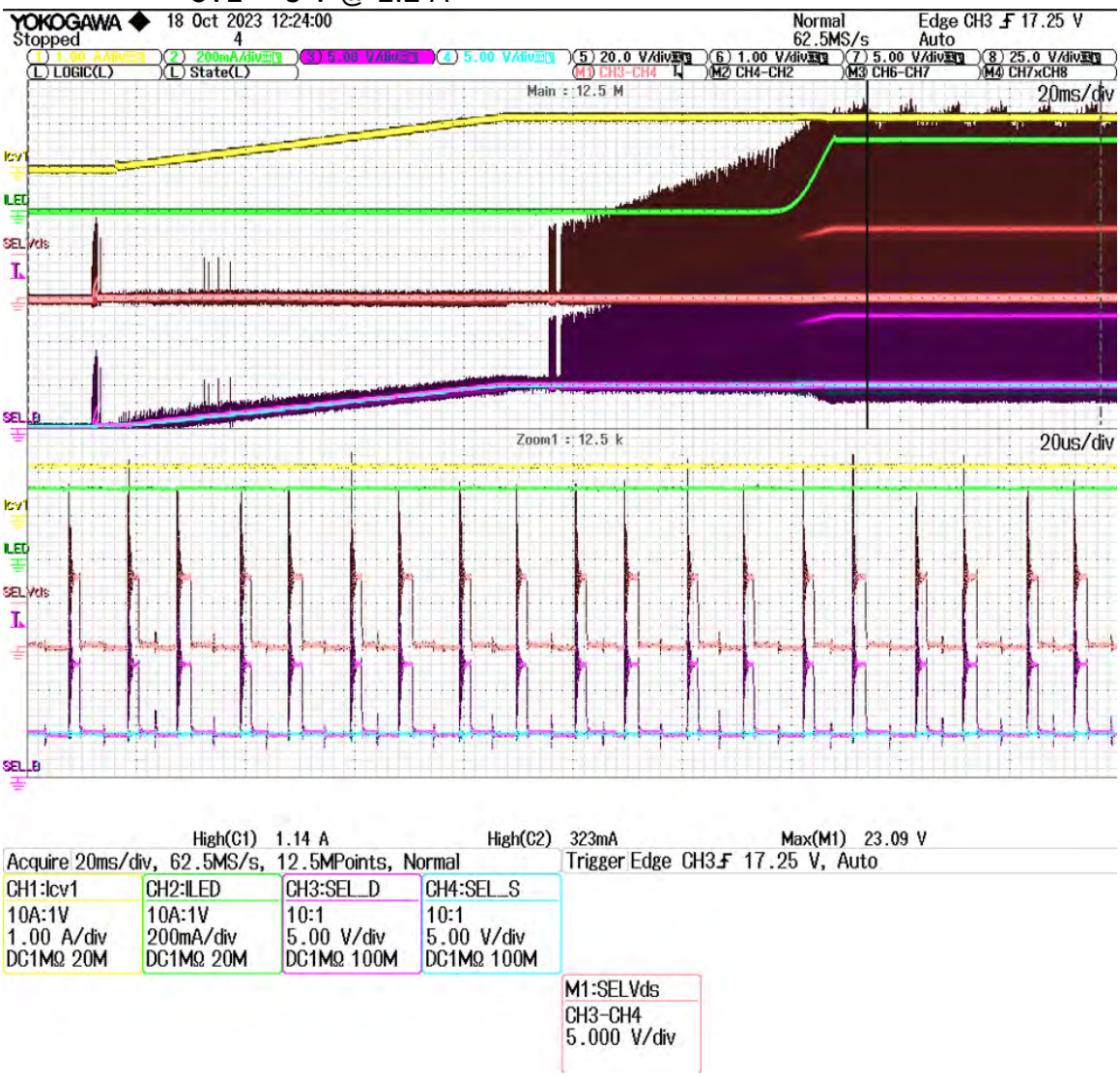


Figure 32 – Selection FET Worst Case Peak Voltage ($V_{(SEL\_DS\_PK)}$ = 23.09 V).

9.7.4 LED Diode Reverse Biased Voltage Waveform

The LED Diode (D1) maximum reverse biased voltage test was performed on power supply covering below test conditions:

- 265 VAC input line voltage
- Full load on both outputs:
  - 56 V LED string with 330 mA
  - CV1 5 V @ 1.2 A

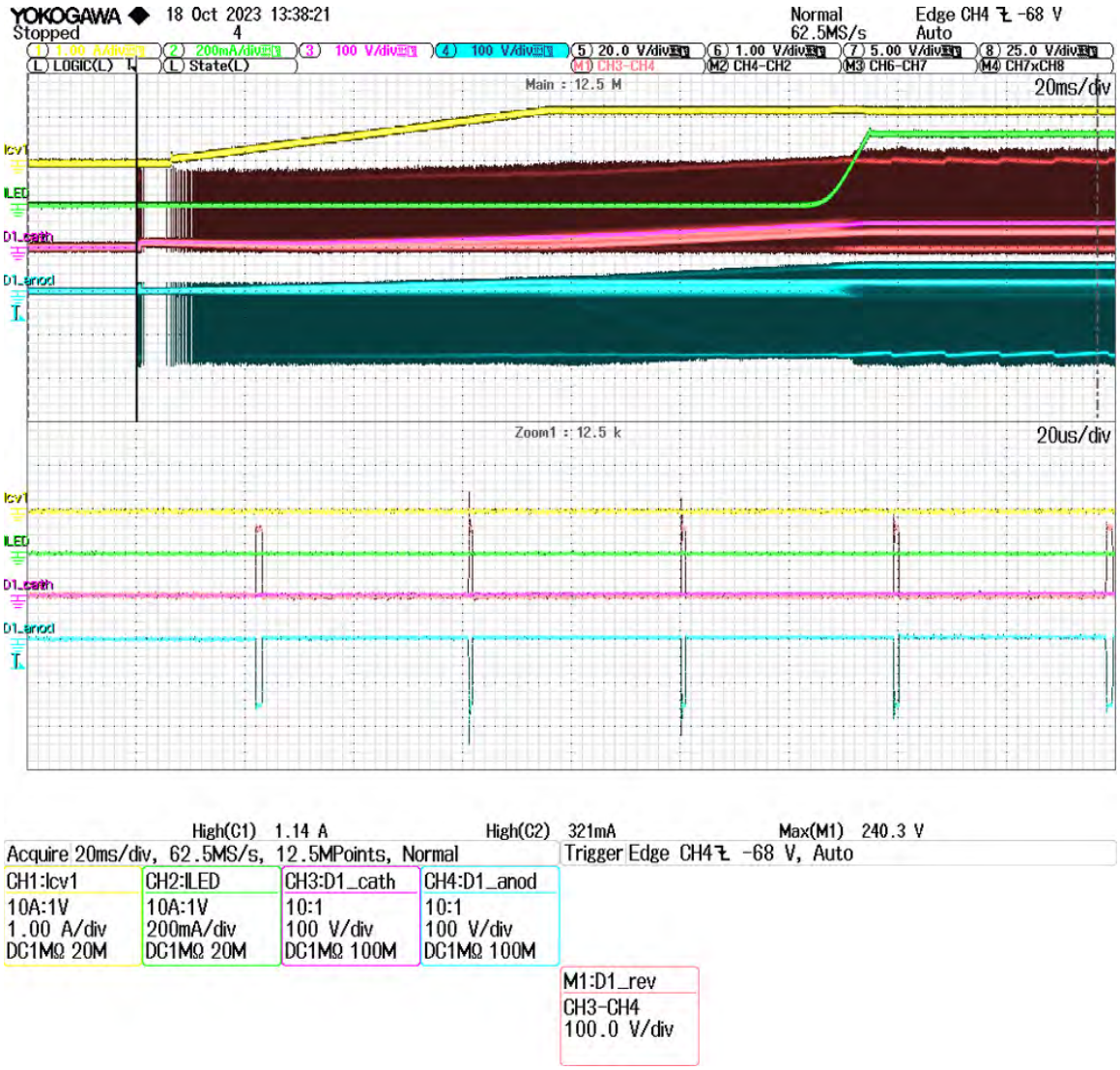


Figure 33 – LED Diode Worst Case Reverse Biased Voltage ($V_{(D1\_PK)}$ = 240.3 V).

9.7.5 BPP Rectifier Diode Reverse Biased Voltage Waveform

The BPP rectifier diode (D2) maximum reverse biased voltage test was performed on power supply covering below test conditions:

- 265 VAC input line voltage
- Full load on both outputs:
  - 56 V LED string with 330 mA
  - CV1 5 V @ 1.2 A

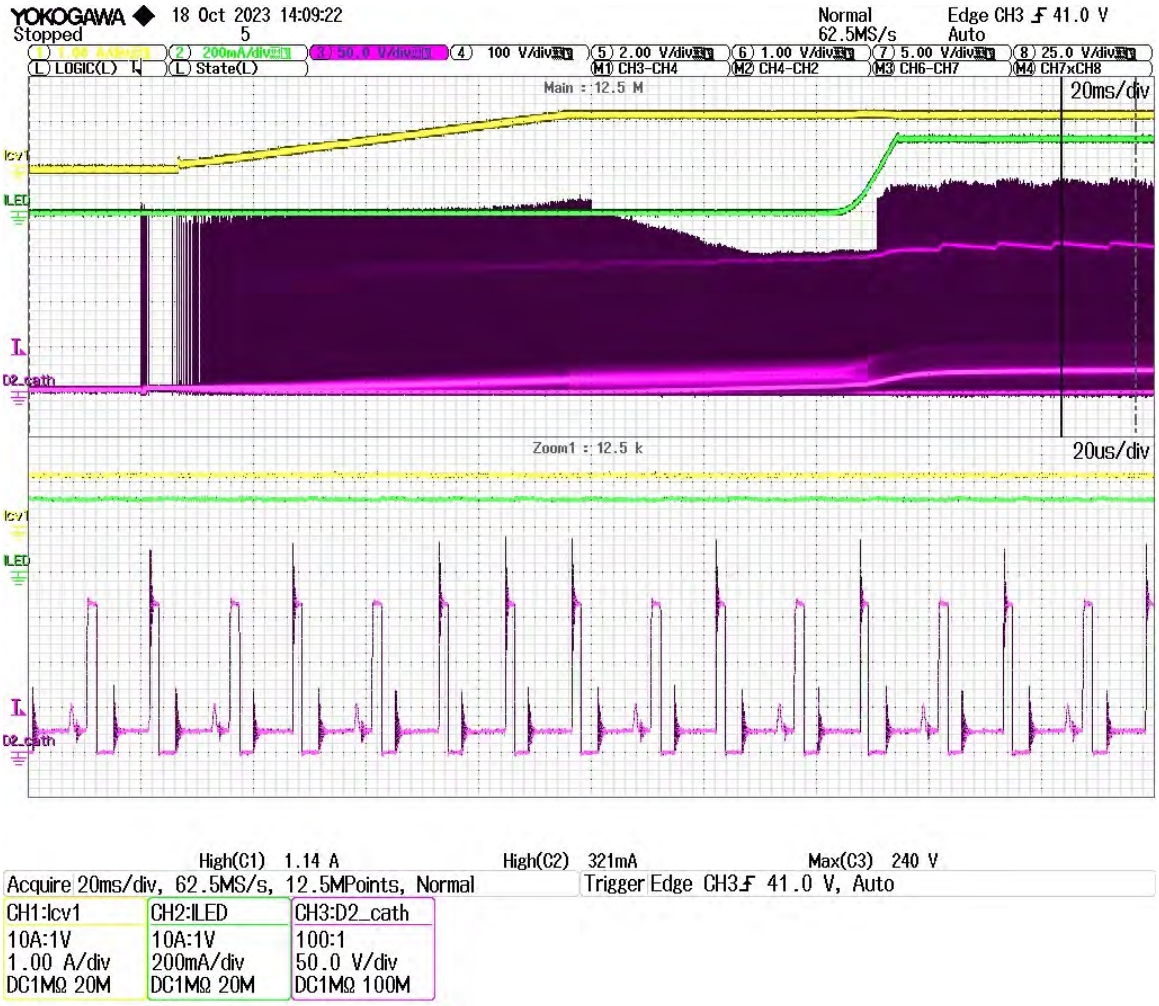


Figure 34 – BPP Rectifier Diode Worst Case Reverse Biased Voltage ($V_{(D2\_PK)}$ = 240 V).

9.7.6 Primary Switching Frequency

The primary switching frequency of the converter varies depending on the line and load conditions. It was measured under peak load at minimum line input of 90 VAC. The maximum switching frequency occurs at the minimum bulk voltage - 112 kHz instantaneous frequency and 94 kHz average frequency. Under the same condition over a cycle of the mains cycle, the average primary switching frequency was 91 kHz.

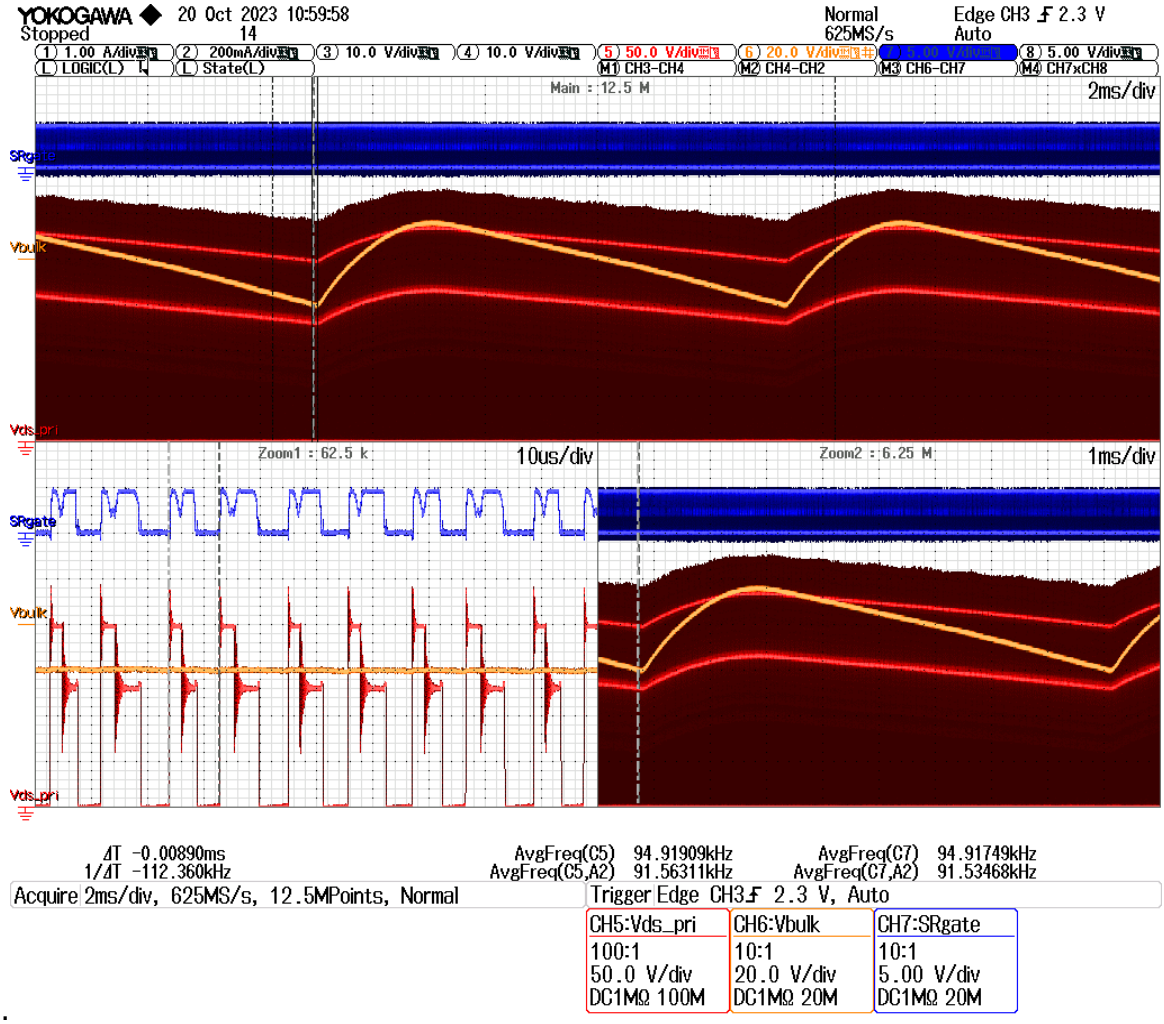


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Figure 35 – Primary Switching Frequency at 90 VAC Input Line Voltage.

9.7.7 Transformer Current Waveforms

Figure 36 – Transformer All Winding Currents Over a Mains Cycle, 90 VAC.

		I_{PK} [A]	I_{RMS} [A]	I_{AVG} [A]
Primary	**CH1**	1.18	0.45	0.263
SR	**CH2**	6.47	2.221	1.607
ICV1	**CH3**	6.56	2.108	1.268
ILED	**CH4**	2.88	0.83	0.426

Table 5 – Figure 36 Current Values.

Figure 37 – Transformer All Winding Currents at Minimum Bulk Capacitor Voltage, 90 VAC.

		I_{PK} [A]	I_{RMS} [A]	I_{AVG} [A]
Primary	**CH1**	1.16	0.5	0.316
SR	**CH2**	6.32	2.351	1.631
ICV1	**CH3**	6.4	2.245	1.296
ILED	**CH4**	2.85	0.832	0.424

Table 6 – Figure 37 Current Values.

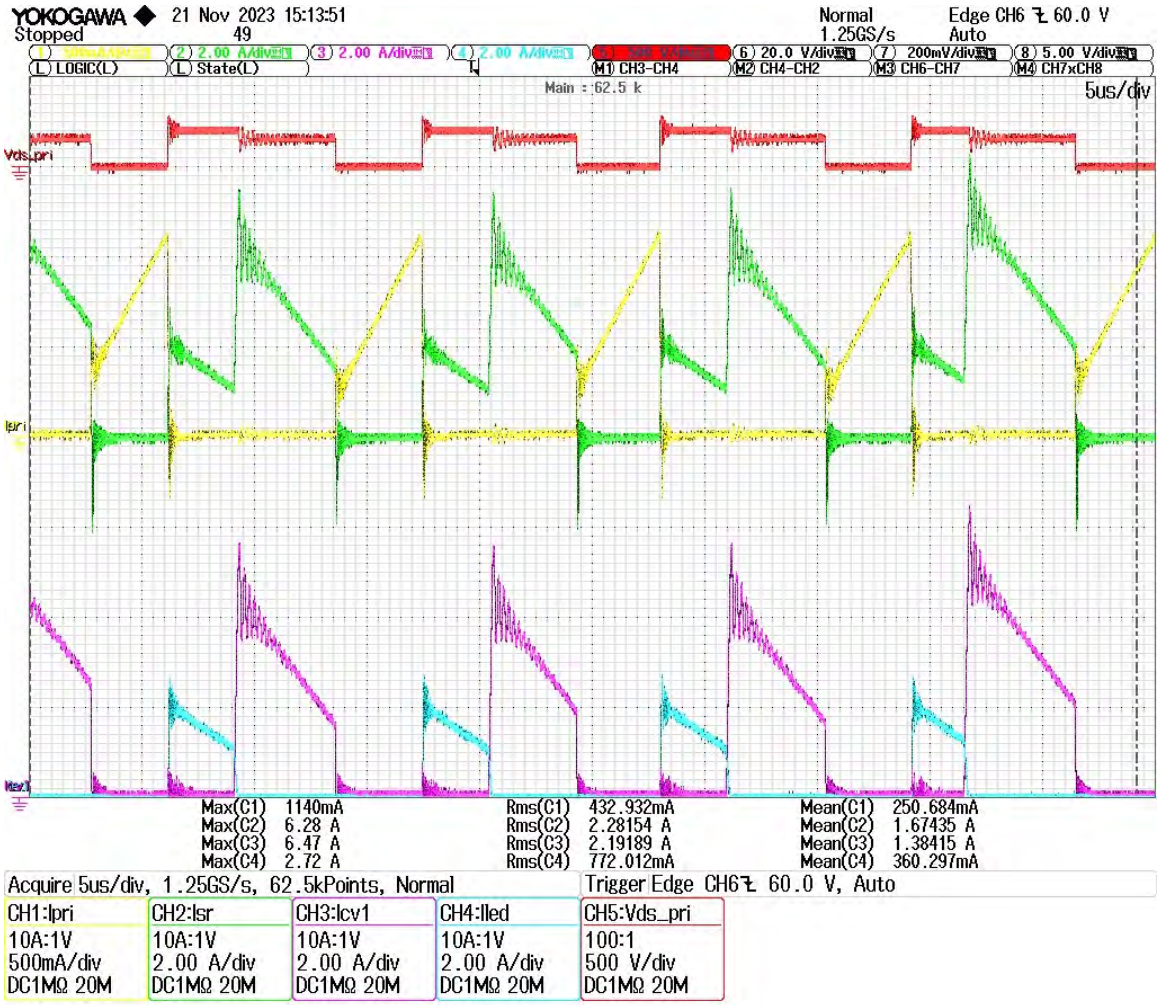


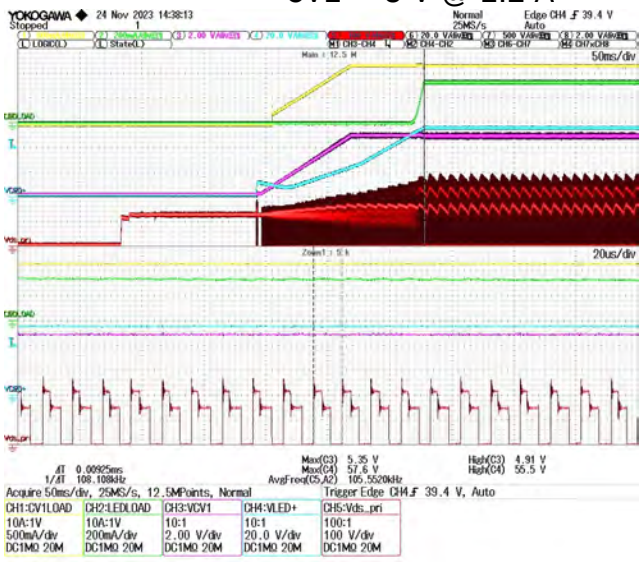
Figure 38 – Transformer Currents – Detailed View.

9.8 Start-Up Waveforms

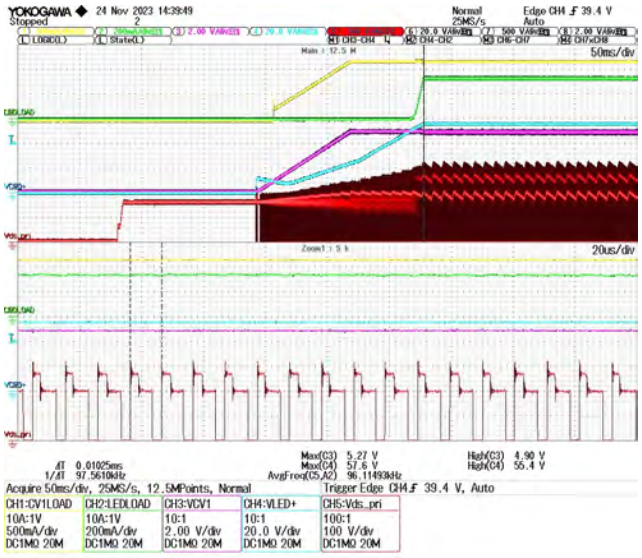
9.8.1 Full Load Start-up

The full load start-up test was performed on power supply covering below test conditions:

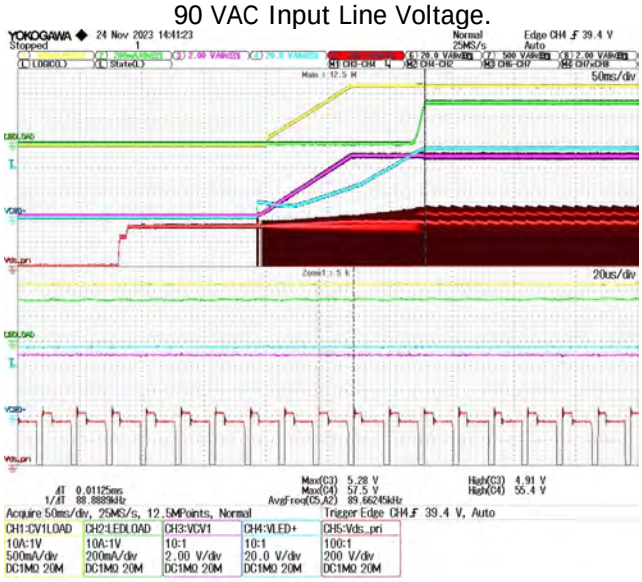
- All nominal line voltages (90 V, 115 V, 230 V, 265 V)
- Full load on both outputs:
  - LED = 56 V @ 330 mA
  - CV1 = 5 V @ 1.2 A



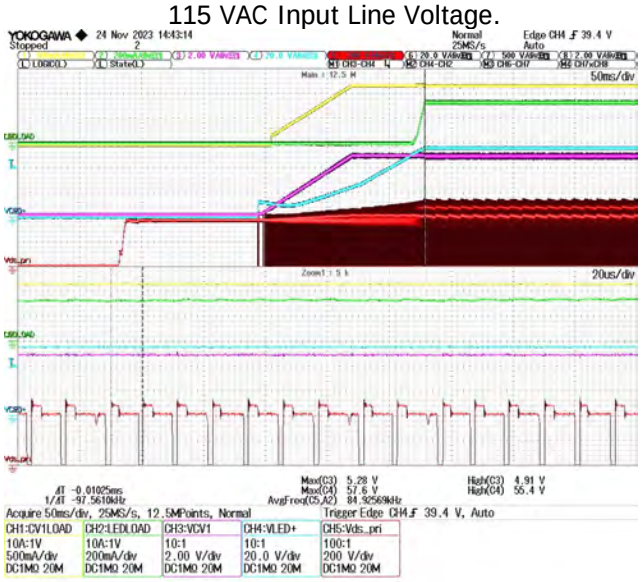
90 VAC Input Line Voltage.



115 VAC Input Line Voltage.



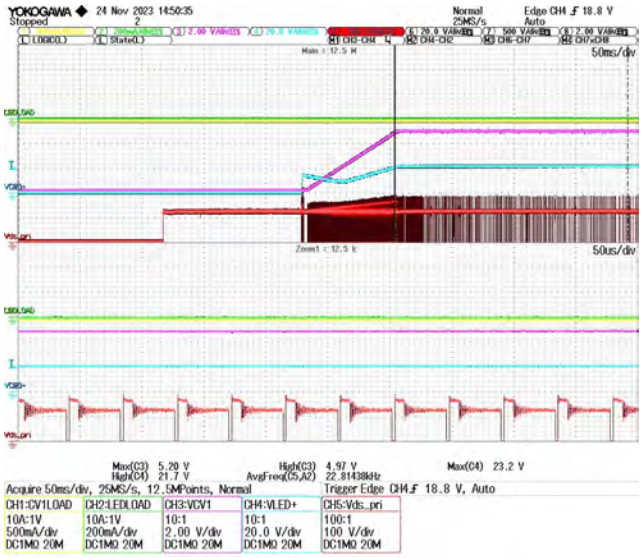
230 VAC Input Line Voltage.



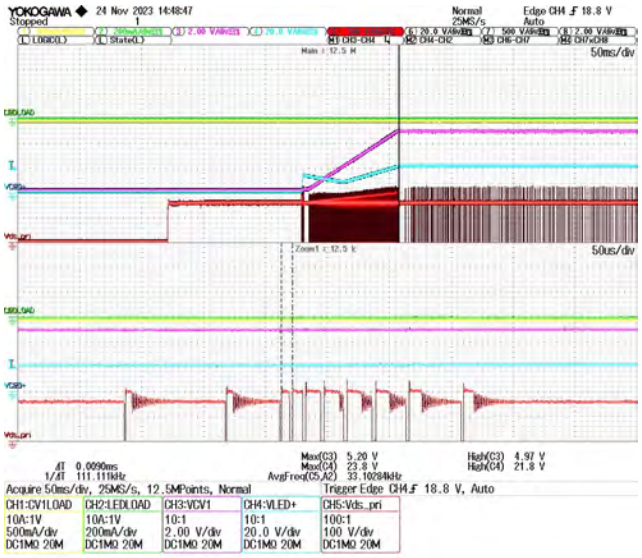
265 VAC Input Line Voltage.

Figure 39 – Full Load Start-up.

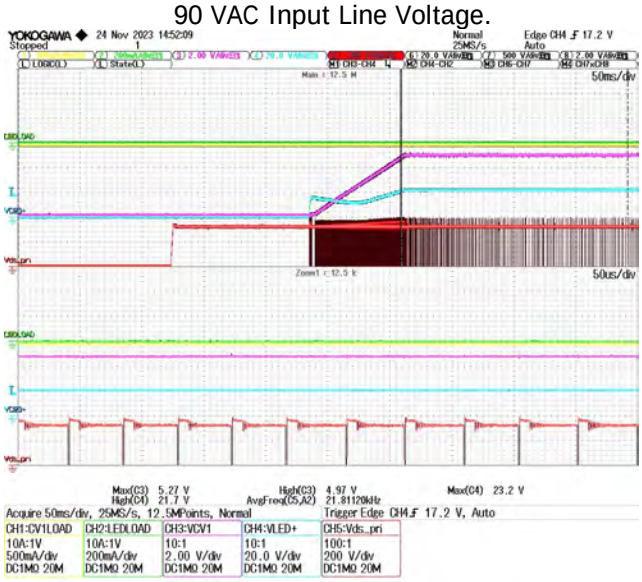
9.8.2 No-Load Start-up



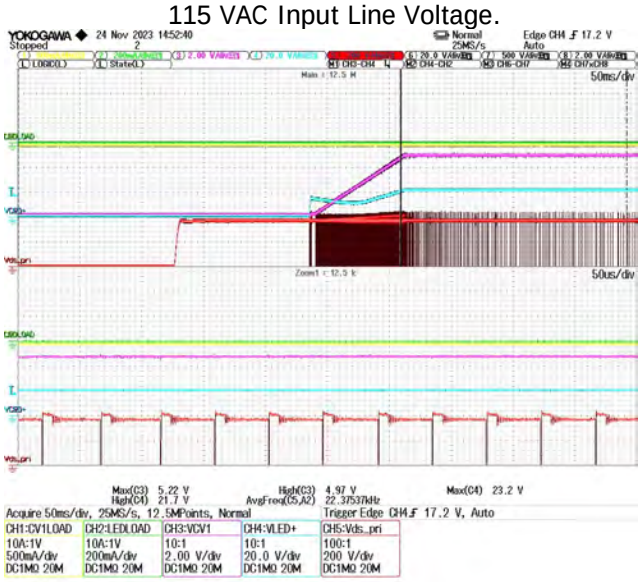
90 VAC Input Line Voltage.



115 VAC Input Line Voltage.



230 VAC Input Line Voltage.



265 VAC Input Line Voltage.

Figure 40 – No-load Start-up.

9.8.3 Start-up Under Single Fault Conditions

The start-up test under fault conditions was tested covering below test conditions:

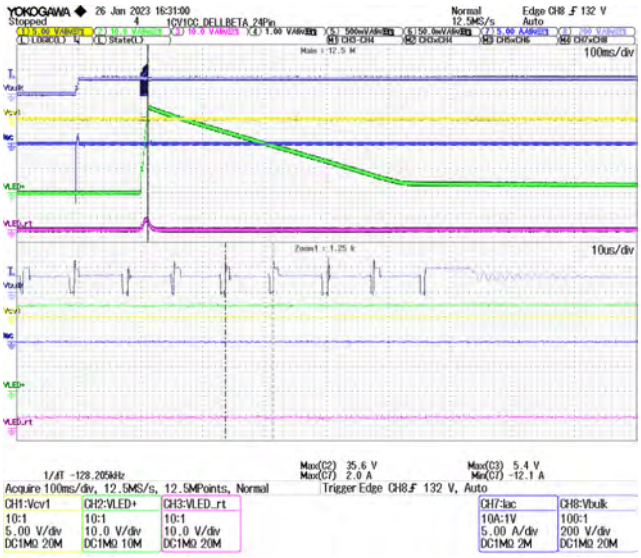
- All nominal line voltages (90 V, 115 V, 230 V, 265 V)
- Full load on both outputs:
  - LED = 56 V @ 330 mA
  - CV1 = 5 V @ 1.2 A

The fault conditions include:

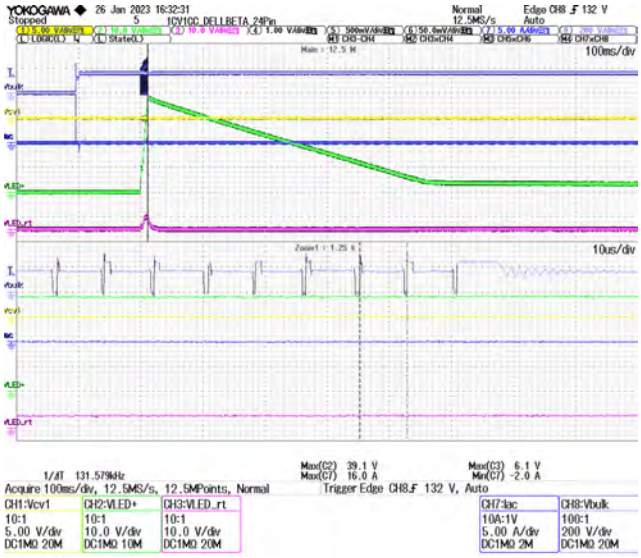
- Short-circuit to GND on one of the outputs：
  - CV1 or
  - LED
- No FB on one of the outputs
  - CV1 or
  - LED

In all cases, the power supply was able to prevent any permanent damage to any component. Line fuse F1 remained intact.

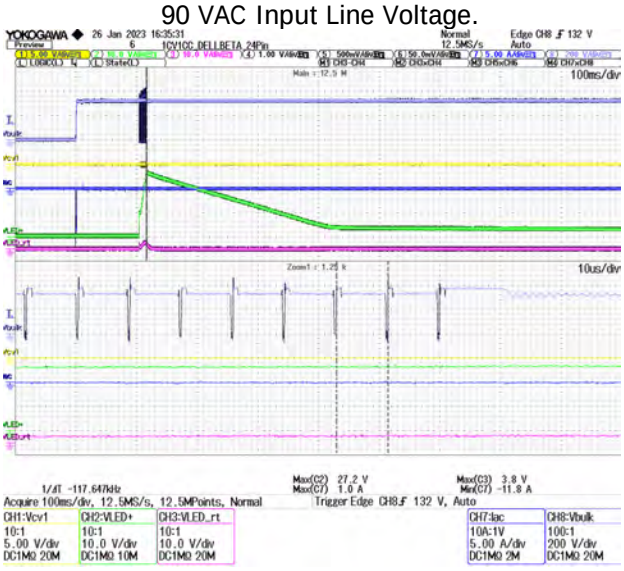
9.8.3.1 Start-up with CV1 Shorted to GND



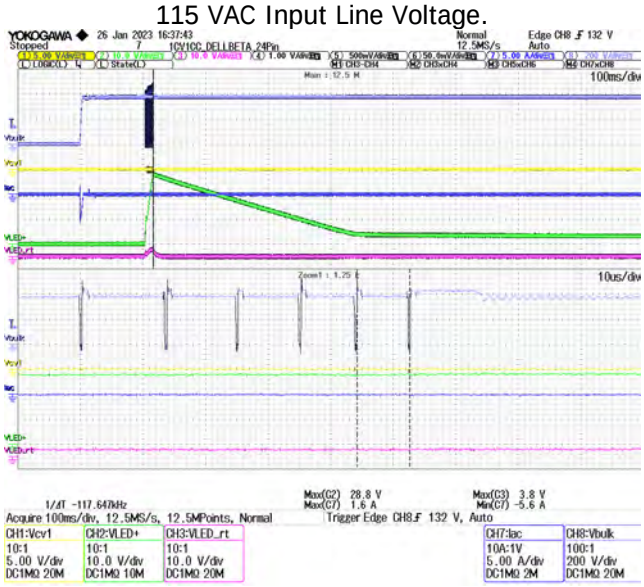
90 VAC Input Line Voltage.



115 VAC Input Line Voltage.



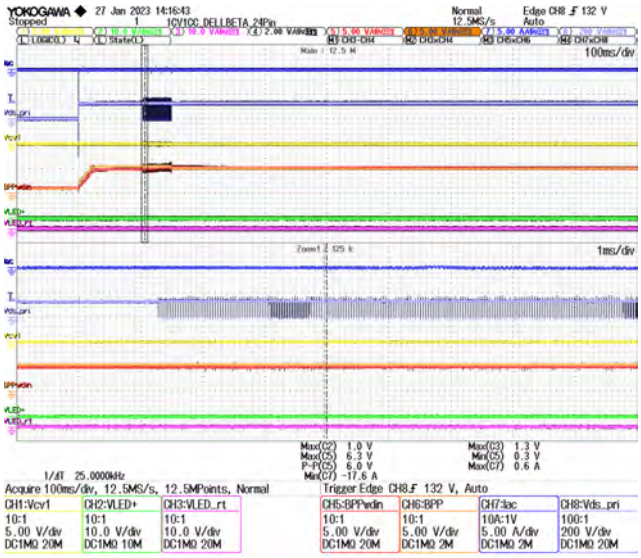
230 VAC Input Line Voltage.



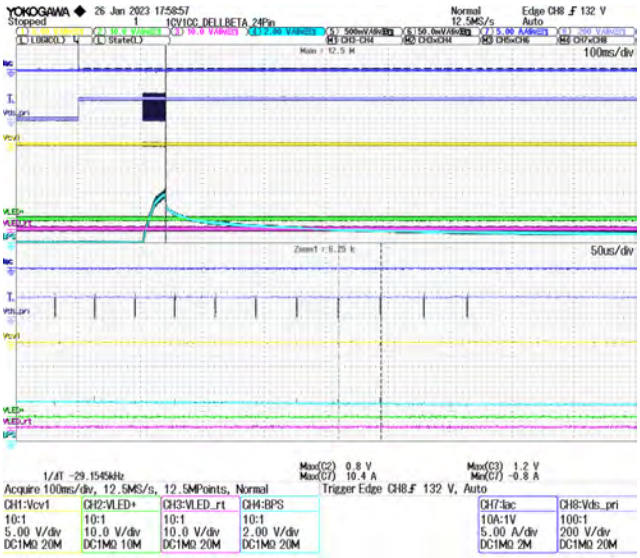
265 VAC Input Line Voltage.

Figure 41 – Start-up with CV1 Shorted to GND.

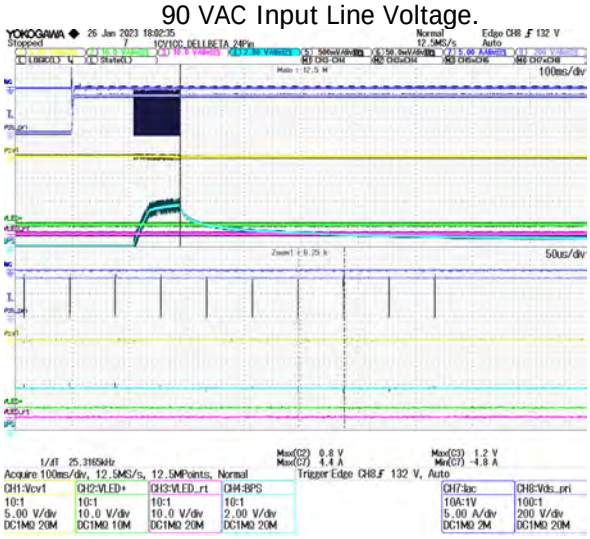
9.8.3.2 Start-up with VLED+ Shorted to GND



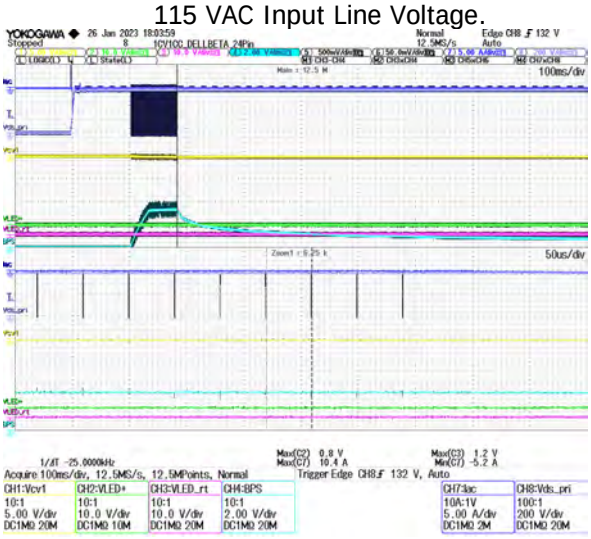
90 VAC Input Line Voltage.



115 VAC Input Line Voltage.



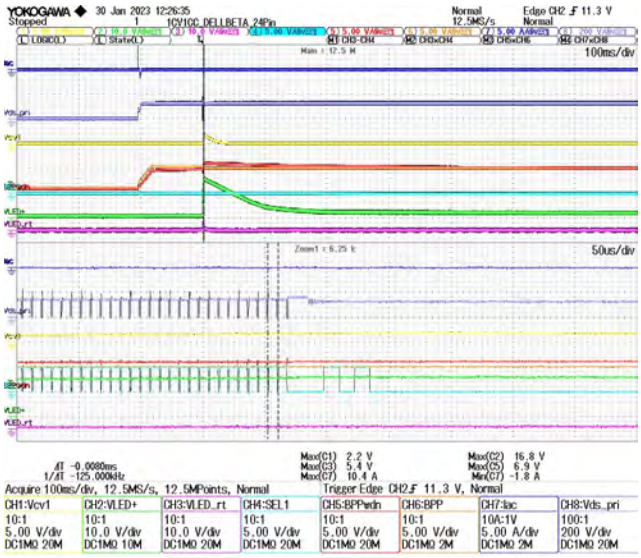
230 VAC Input Line Voltage.



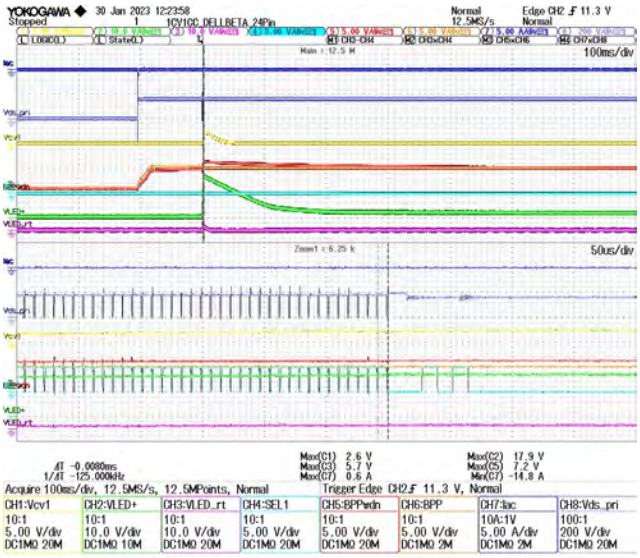
265 VAC Input Line Voltage.

Figure 42 – Start-up with LED Shorted to GND.

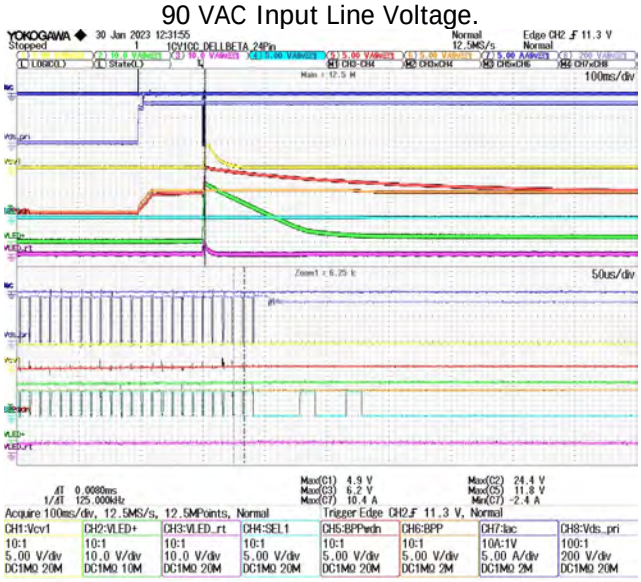
9.8.3.3 Start-up with No FB on CV1



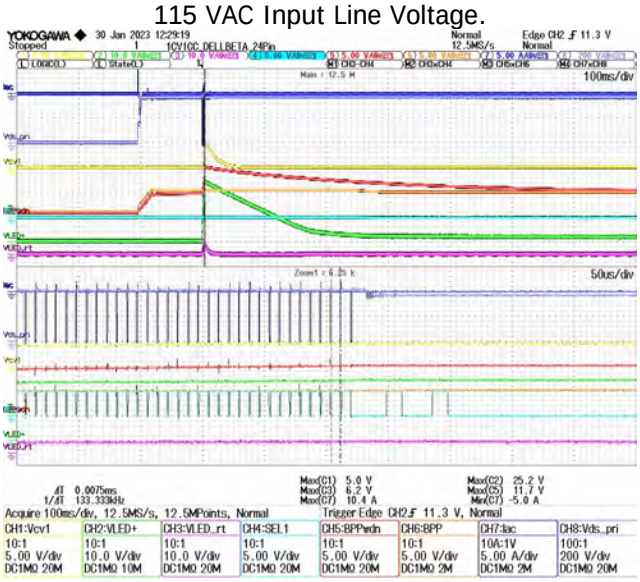
90 VAC Input Line Voltage.



115 VAC Input Line Voltage.



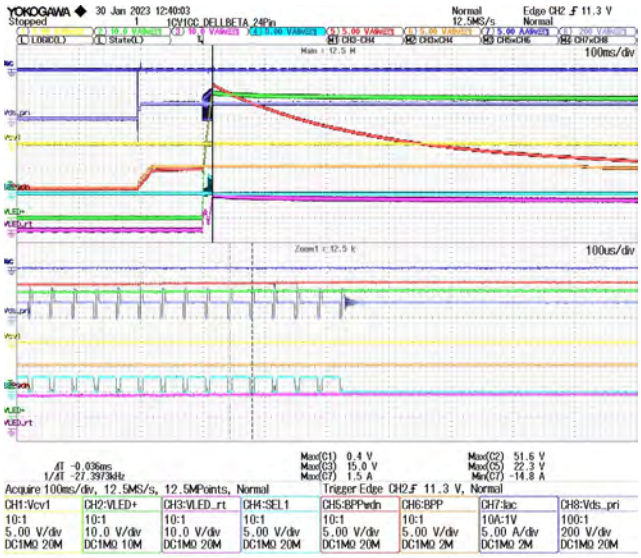
230 VAC Input Line Voltage.



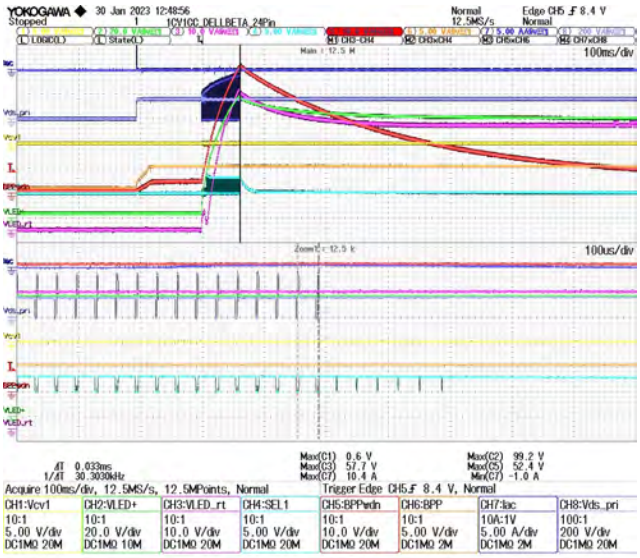
265 VAC Input Line Voltage.

Figure 43 – Start-up with No FB on CV1.

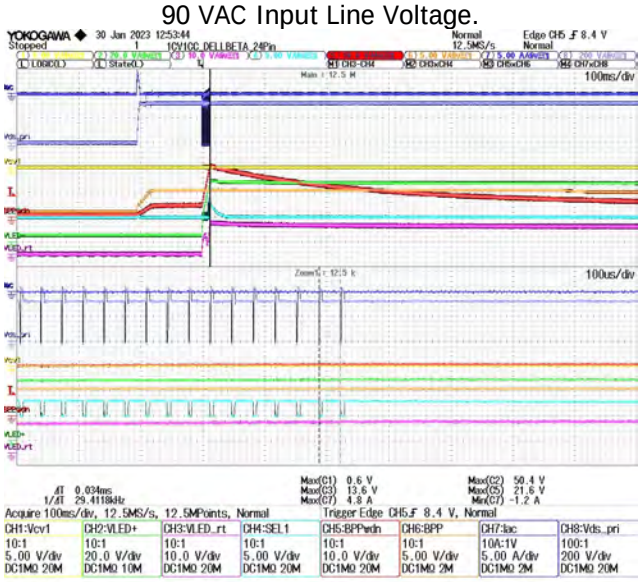
9.8.3.4 Start-up with No FB on LED



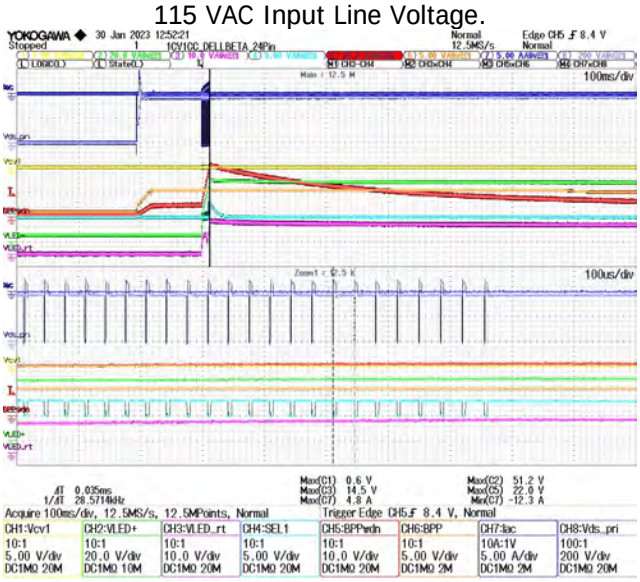
90 VAC Input Line Voltage.



115 VAC Input Line Voltage.



230 VAC Input Line Voltage.



265 VAC Input Line Voltage.

Figure 44 – Start-up with No FB on LED.

9.9 Brown-In and Brown-Out

The brown-in and brown-out results were measured with below conditions to avoid unit shut down due to Request Not Clear/PLIM fault:

- LED disabled
- CV1 = 5 V @ 1.2 A

The results are shown in the table below.

Brown-Out Threshold	Brown-In Threshold
[V_{RMS}]	[V_{RMS}]
62.5	76.3

Table 7 – Brown-In and Brown-Out Thresholds at Full Power.

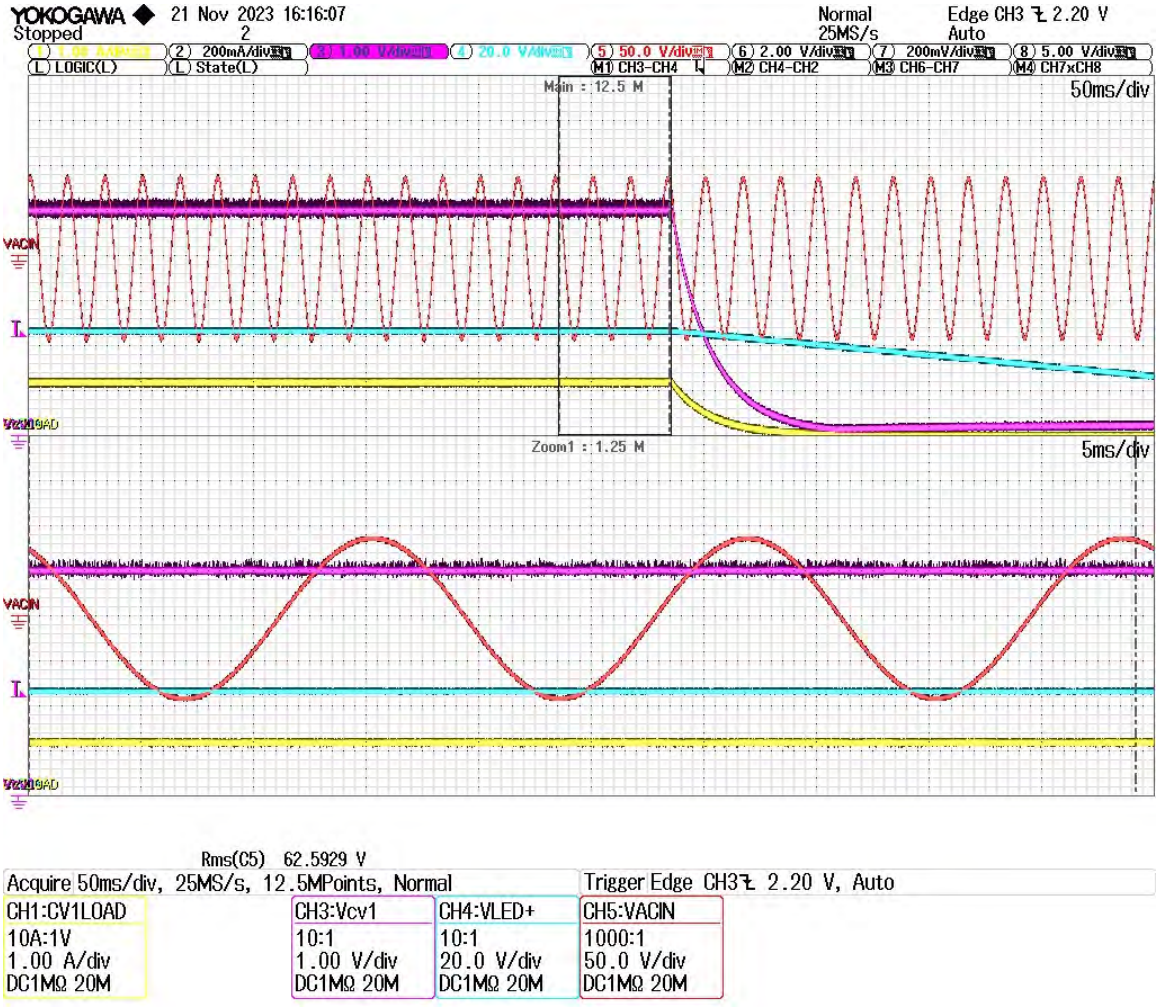


Figure 45 – Brown-Out Response, LED Disabled, CV1 = 5 V @ 1.2 A.

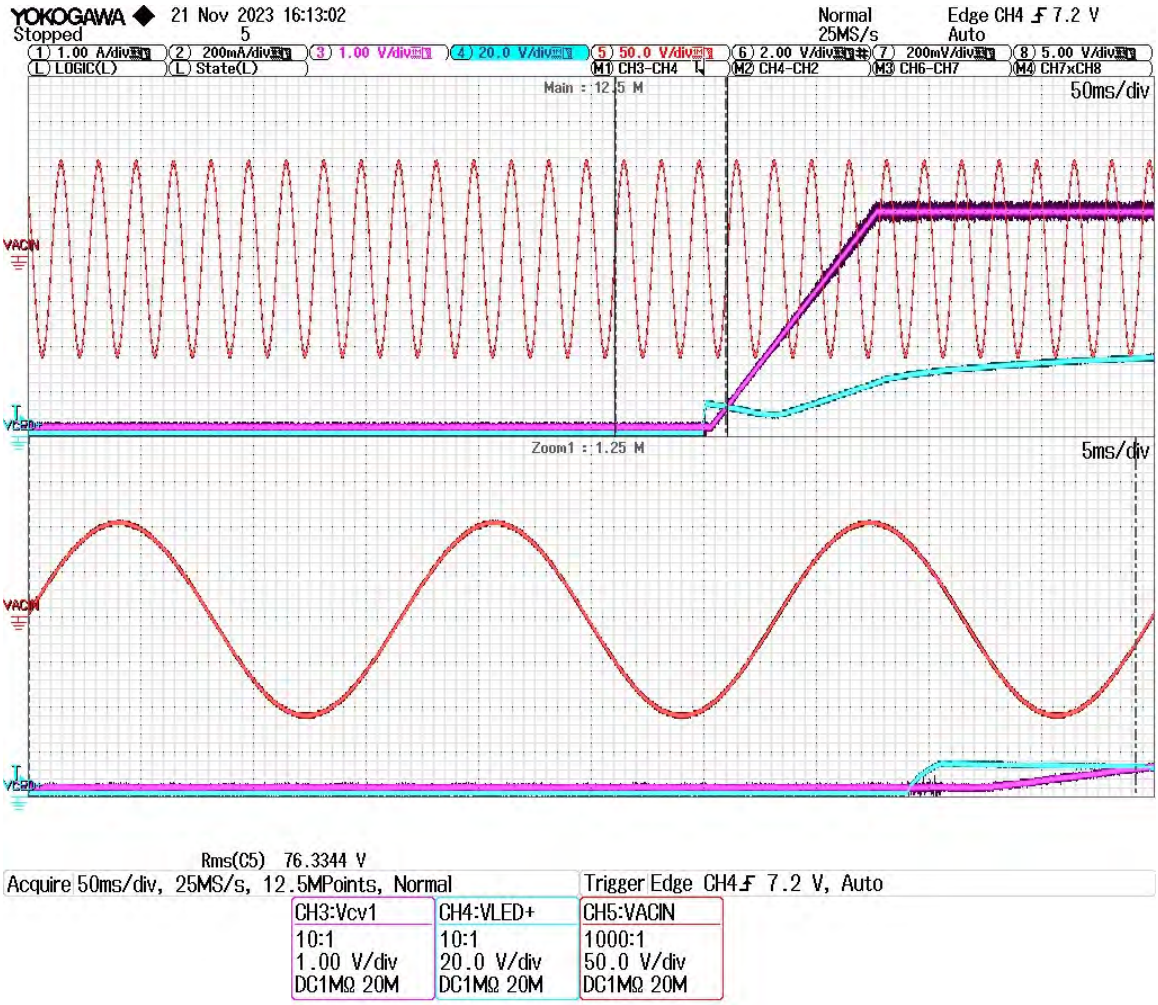


Figure 46 – Brown-In Response, LED Disabled, CV1 = 5 V @ 1.2 A.

9.10 Output Protections

9.10.1 CV1 Power Limit

The power limit test was performed on power supply covering below test conditions:

- All nominal line voltages (90 V, 115 V, 230 V, 265 V)
- LED string:
  - LED = 56 V @ 43 mA and 330 mA
  - LED = 45 V @ 43 mA and 400 mA

The fault condition is shown by a 'death rattle', a small number of bits output sequentially to the CDR1 pin, indicating the InnoMux2-BL stop condition. In this case, the death rattle on the selection FET (Q2) gate reads 010100 – indicating Request Not Clear/PLIM fault. To be noted, below test results are measured on a part where CV1 power limit was trimmed to 73 kHz and no power limit was trimmed on LED output. For a standard part, there will be no power limit trimmed on either CV1 or LED outputs. If power limit is required on any output, a custom part is needed.

V_{IN} [V_{RMS}]	I_CV1 [A_{DC}] when unit shuts down	I_CV1 / I_CV1_nom [%]
90	3.61	301
115	3.94	328
230	4.63	386
265	4.62	385

Table 8 – CV1 Output Power Limit with LED = 56 V @ 43 mA.

V_{IN} [V_{RMS}]	I_CV1 [A_{DC}] when unit shuts down	I_CV1 / I_CV1_nom [%]
90	2.06	172
115	2.61	218
230	3.62	302
265	3.83	319

Table 9 – CV1 Output Power Limit with LED = 56 V @ 330 mA.

V_{IN} [V_{RMS}]	I_CV1 [A_{DC}] when unit shuts down	I_CV1 / I_CV1_nom [%]
90	3.66	305
115	4.05	338
230	4.52	377
265	4.81	401

Table 10 – CV1 Output Power Limit with LED = 45 V @ 43 mA.

V_{IN} [V_{RMS}]	I_CV1 [A_{DC}] when unit shuts down	I_CV1 / I_CV1_nom [%]
90	1.99	166
115	2.52	210
230	3.55	296
265	3.75	313

Table 11 – CV1 Output Power Limit with LED = 45 V @ 400 mA.

Death rattle on CV1 selection FET (Q2) gate indicated that the unit shut down due to Request Not Clear/PLIM fault with error code 010010. Results are shown in Figure 47 and Figure 48.

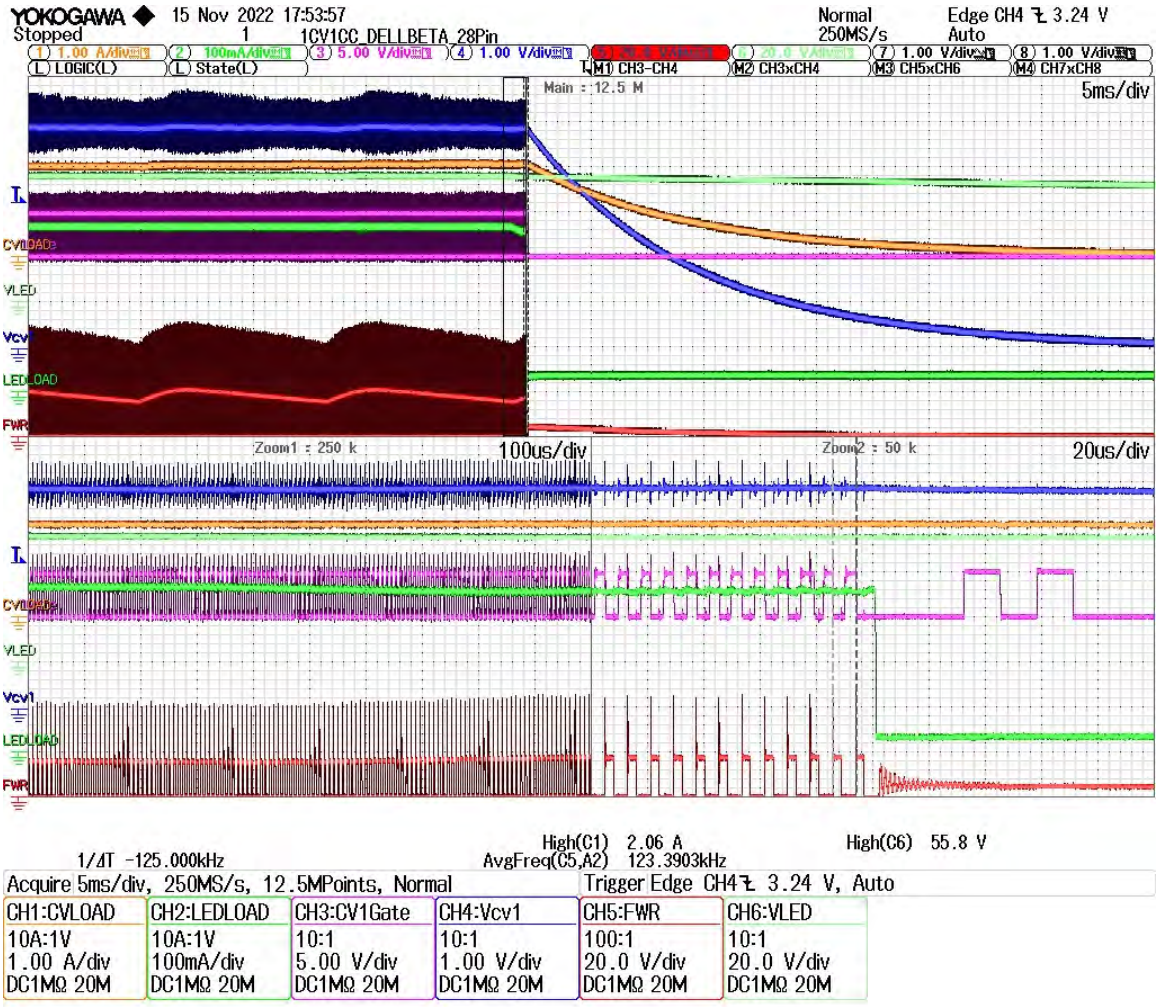


Figure 47 – CV1 Output Power Limit Test (WC) at 90 VAC, LED = 56 V @ 330 mA.

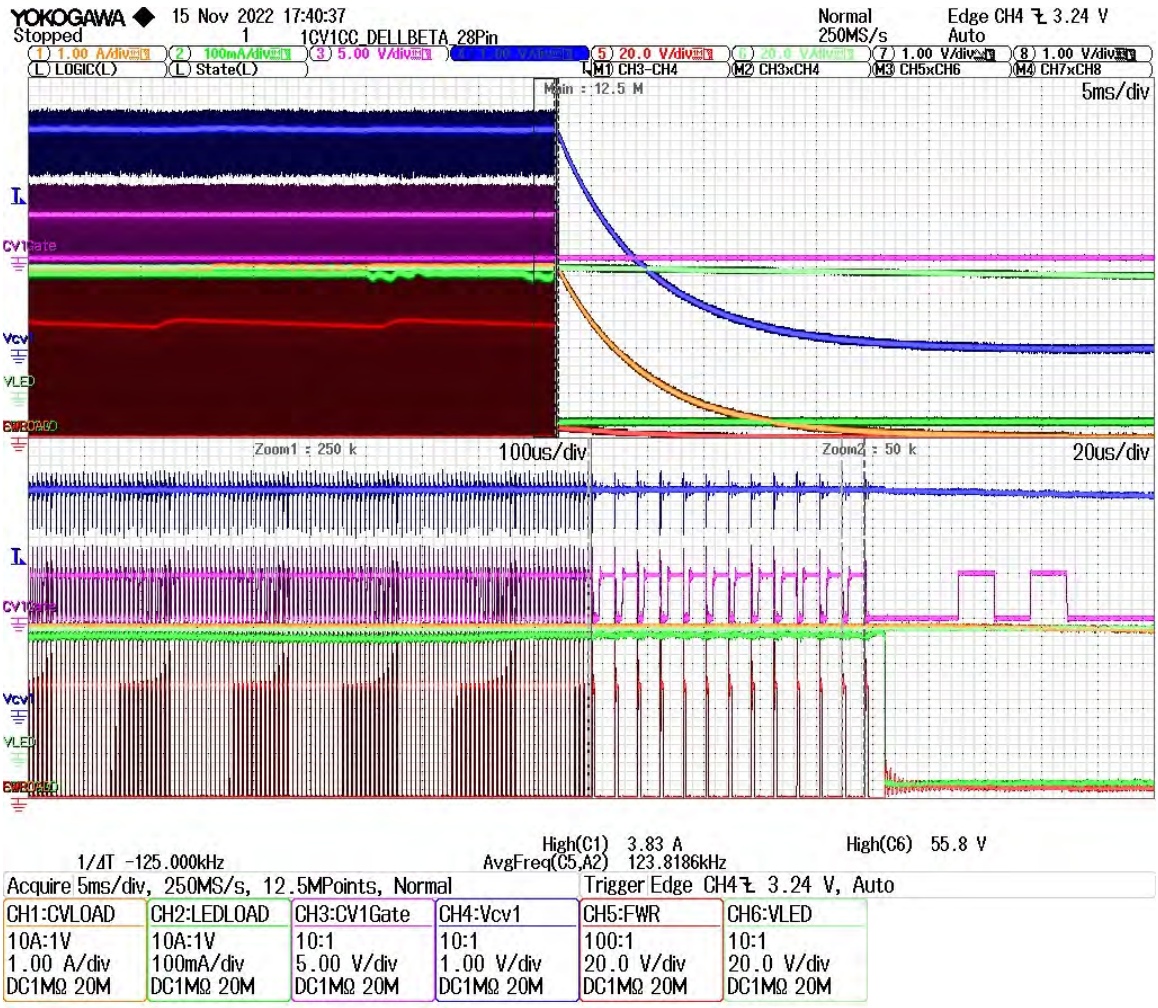


Figure 48 – CV1 Output Power Limit Test (WC) at 265 VAC, LED = 56 V @ 330 mA.

9.10.2 CV1 Output Overvoltage Protection

The overvoltage protection thresholds of CV1 was tested with full power on LED and no-load on CV1. Additional charge was injected into the output filter capacitor of the output under test until the converter went into an auto-restart. The test was carried out with all nominal line voltages 90 V, 115 V, 230 V and 265 V with 45 V LED stack voltage. The results are shown in the table below. The death rattle on selection FET (Q2) gate reads 010001 – indicating output overvoltage fault.

V_{IN} [V_{RMS}]	CV1 OVP [V_{DC}]	CV1 OVP [%]	VLED+ [V_{DC}]	I_CV1 [A_{DC}]	I_LED [A_{DC}]
90	5.63	112	45	0	0.4
115	5.62	112	45	0	0.4
230	5.63	112	45	0	0.4
265	5.63	112	45	0	0.4

Table 12 – CV Outputs OVP Test.

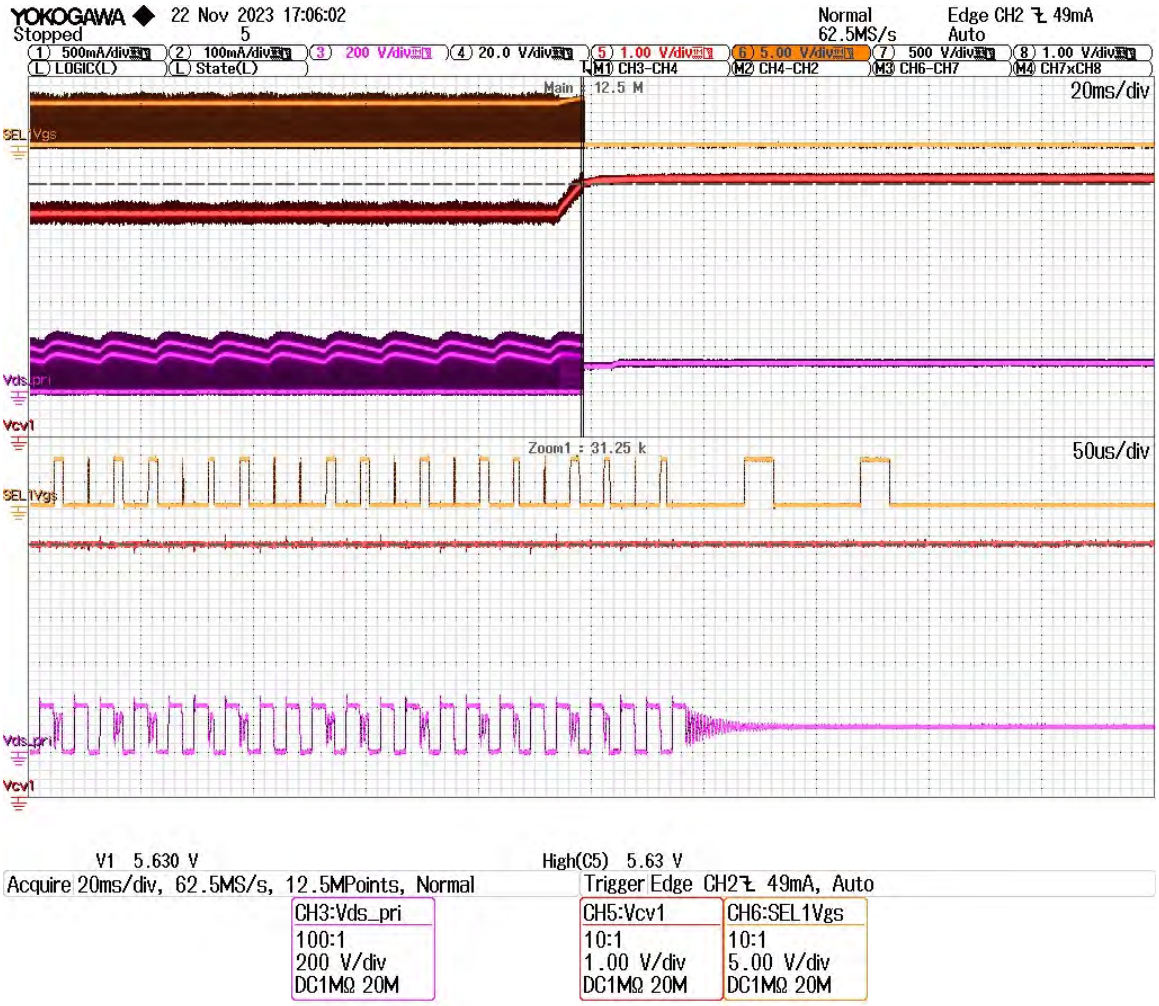


Figure 49 – CV1 Output OVP at Line Voltage 90 V.

9.10.3 LED Output Overvoltage Protection

The overvoltage protection thresholds of the LED output was tested at no-load on all outputs. Additional charge was injected into the output filter capacitor of the LED output until the converter went into an auto-restart. The test was carried out at line voltages 90 V, 115 V, 230 V and 265 V with 40 V LED stack voltage. The results are shown in the table below. Tests are further illustrated in Figure 50.
The death rattle on selection FET (Q2) gate reads 010001 – indicating output overvoltage fault.

V_{IN} [V_{RMS}]	CV1 [V_{DC}]	VLED+ OVP [V_{DC}]	VLED+ OVP [%]	I_CV1 [A_{DC}]	I_LED [A_{DC}]
90	5	70.3	117	0	0
115	5	70.3	117	0	0
230	5	70.2	117	0	0
265	5	70.2	117	0	0

Table 13 – LED Output OVP Test.

Figure 50 – LED Output OVP at Line Voltage 90 V.

9.11 Output Ripple Measurements

9.11.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe was utilized to reduce noise pick-up. Details of the probe modification are provided in Figure 51.

The probe adapter is shown in Figure 51. It includes a coaxial cable with two parallel capacitors connected to the points of measurement. The capacitors include a 0.1 µF / 100 V ceramic type and a 10 µF / 50 V aluminum electrolytic type. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be ensured.

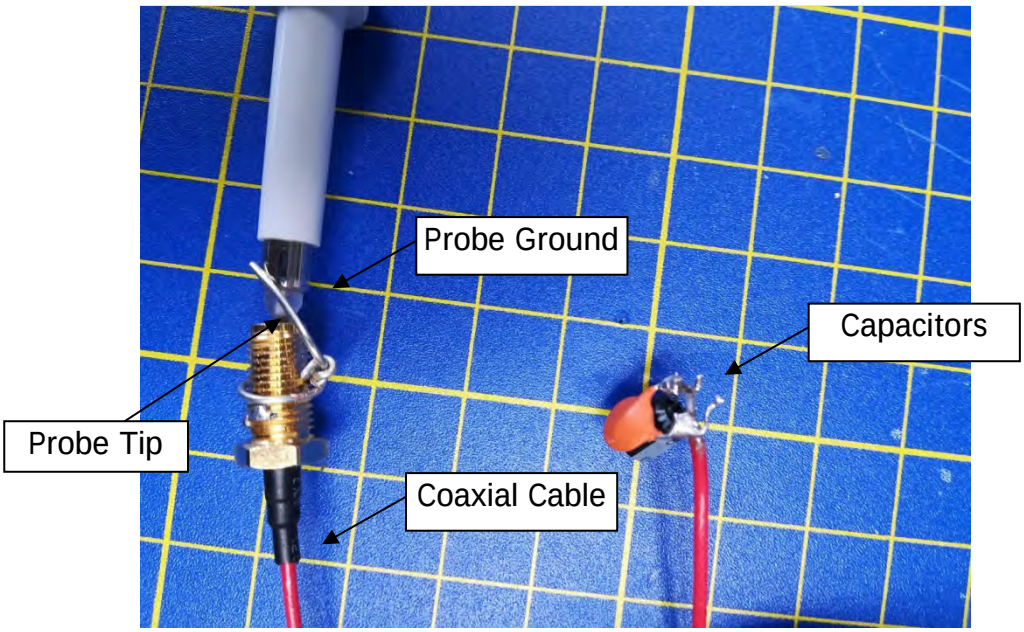
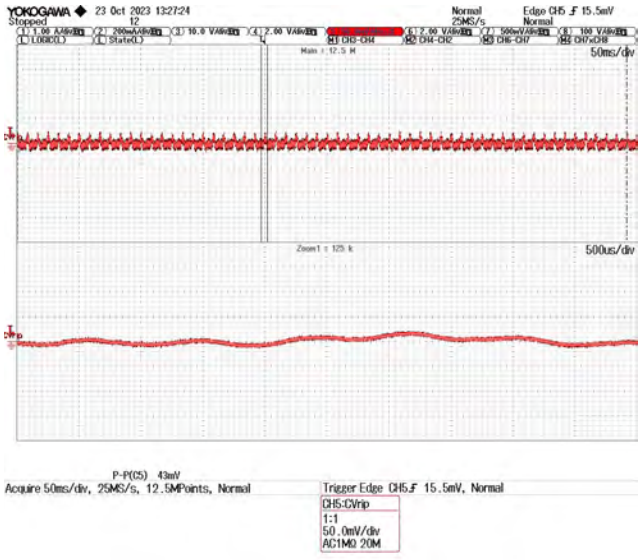


Figure 51 – Oscilloscope Probe Used in Ripple Measurement.

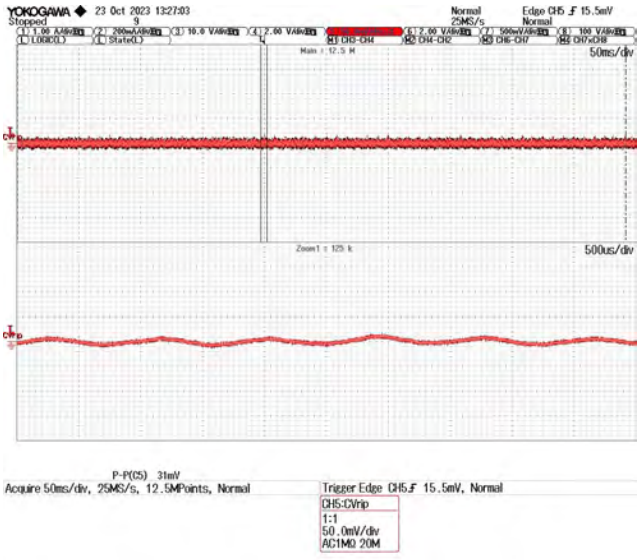
9.11.2 CV1 Output Ripple

9.11.2.1 Test Conditions

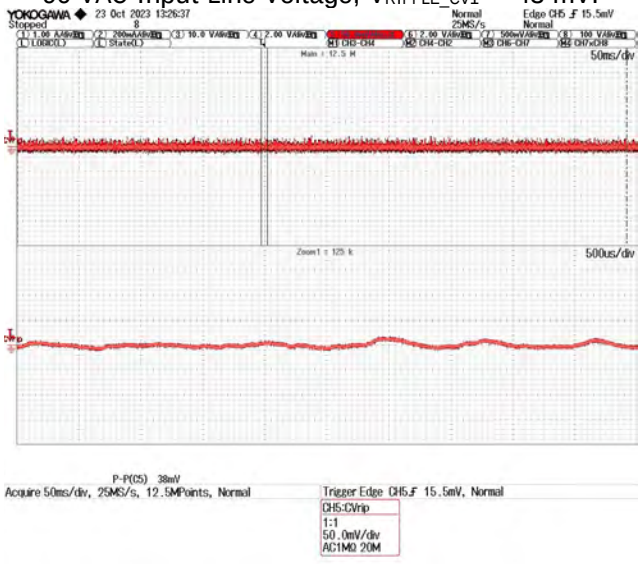
- All nominal line voltages (90 V, 115 V, 230 V, 265 V)
- CV1 = 5 V @ 1.2 A
- 20 MHz bandwidth selected on the scope



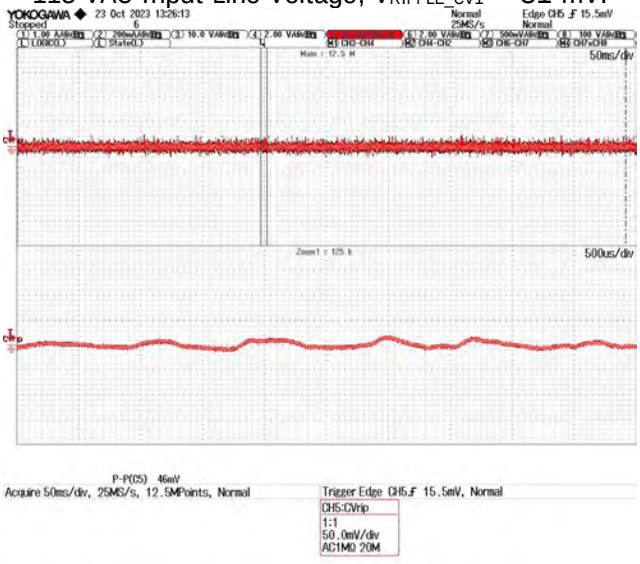
90 VAC Input Line Voltage, V_{RIPPLE_CV1} = 43 mV.



115 VAC Input Line Voltage, V_{RIPPLE_CV1} = 31 mV.

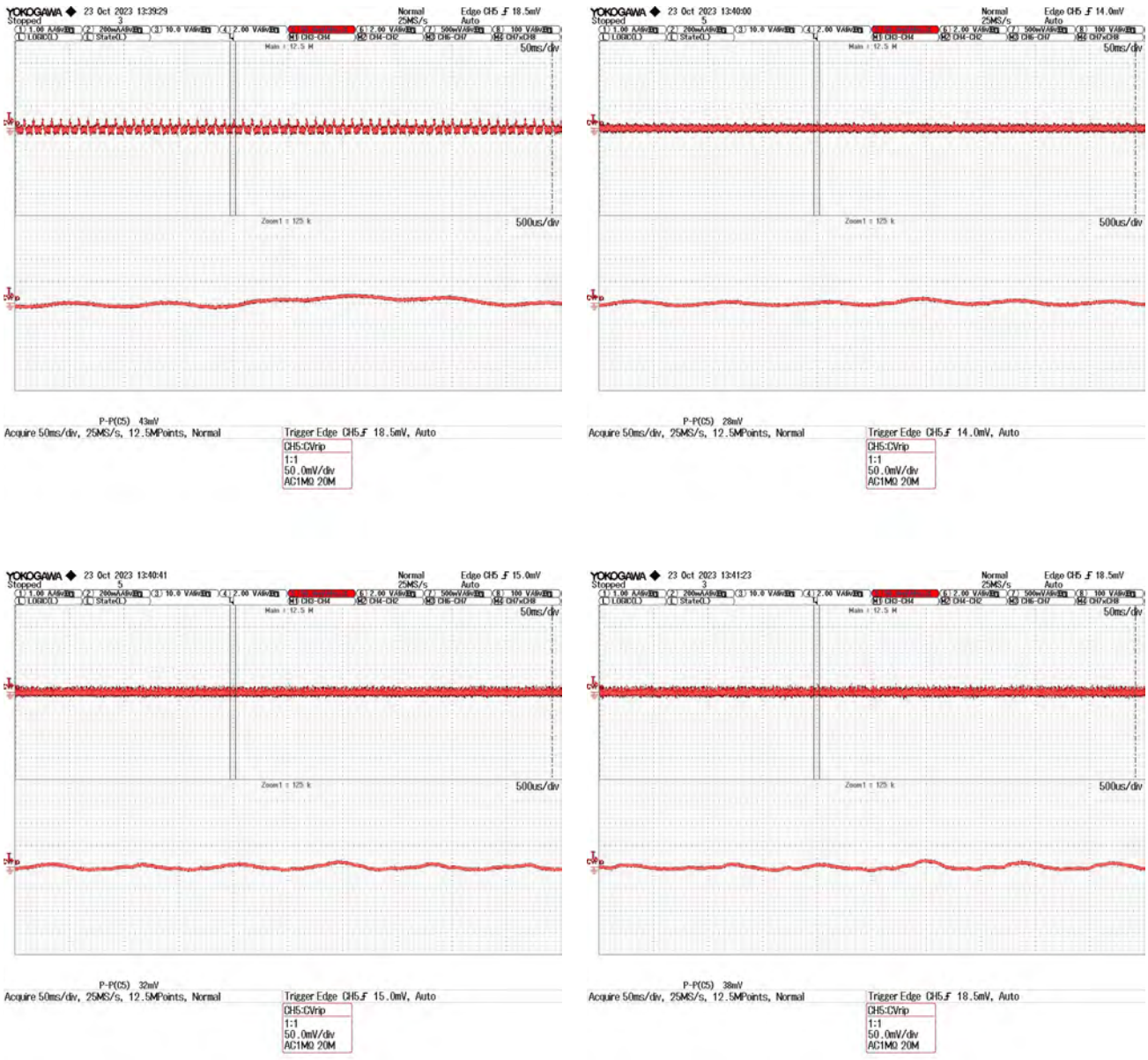


230 VAC Input Line Voltage, V_{RIPPLE_CV1} = 38 mV.



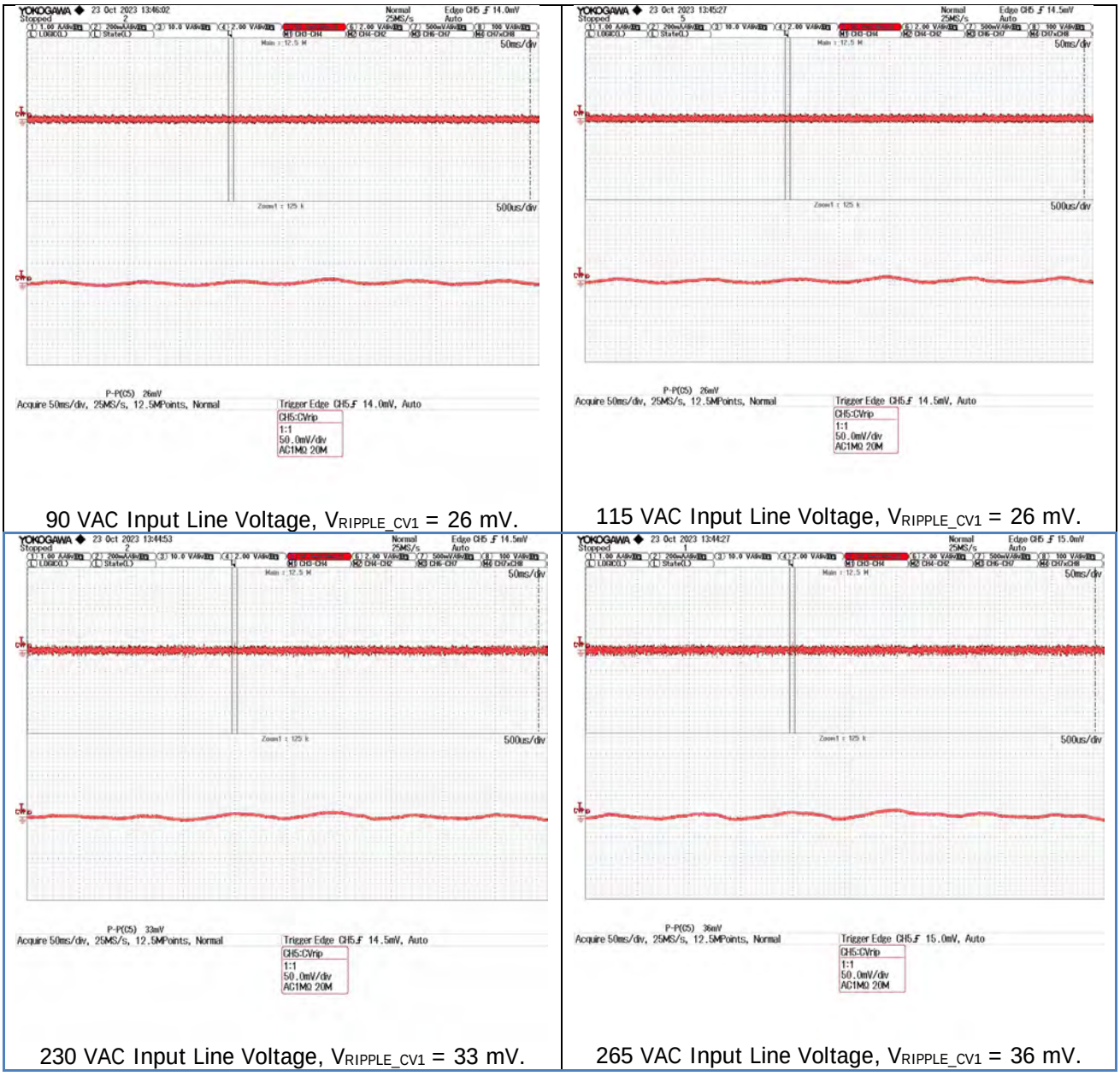
265 VAC Input Line Voltage, V_{RIPPLE_CV1} = 46 mV.

Figure 52 – VCV1 Ripple and Noise, LED = 56 V @ 330 mA.



230 VAC Input Line Voltage, VRIPPLE_CV1 = 32 mV. 265 VAC Input Line Voltage, VRIPPLE_CV1 = 38 mV.

Figure 53 – VCV1 Ripple and Noise, LED = 45 V @ 400 mA.



90 VAC Input Line Voltage, V_{RIPPLE_CV1} = 26 mV.

115 VAC Input Line Voltage, V_{RIPPLE_CV1} = 26 mV.

230 VAC Input Line Voltage, V_{RIPPLE_CV1} = 33 mV.

265 VAC Input Line Voltage, V_{RIPPLE_CV1} = 36 mV.

Figure 54 – VCV1 Ripple and Noise, LED = 29 V @ 400 mA.

9.12 Conducted EMI

The EMI scans were carried out at full power, with the secondary GND connected to EARTH. Note that the negative terminals of all main outputs (CV1 and LED) are connected to the same (secondary) GND.

9.12.1 Line Input 115 VAC

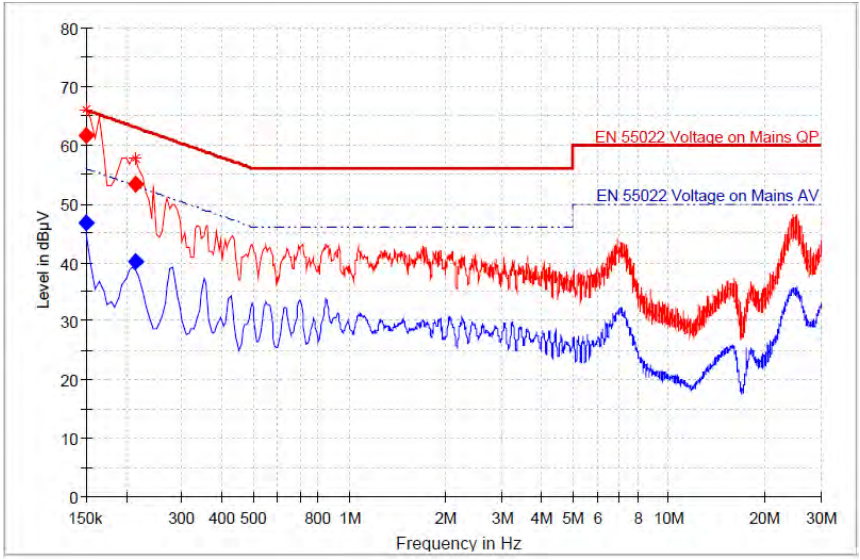


Figure 55 – EMI Test Results at 115 V.

Final_Result

Frequency (MHz)	QuasiPeak (dBµV)	Average (dBµV)	Limit (dBµV)	Margin (dB)	Bandwidth (kHz)	Line	Filter	Corr. (dB)
0.150000	61.61	---	66.00	4.39	10.000	N	ON	20.3
0.150000	---	46.82	56.00	9.18	10.000	N	ON	20.3
0.215000	53.36	---	63.01	9.65	10.000	L1	ON	20.3
0.215000	---	40.11	53.01	12.90	10.000	L1	ON	20.3

Table 14 – EMI Test Results at 115 V.

9.12.2 Line Input 230 VAC

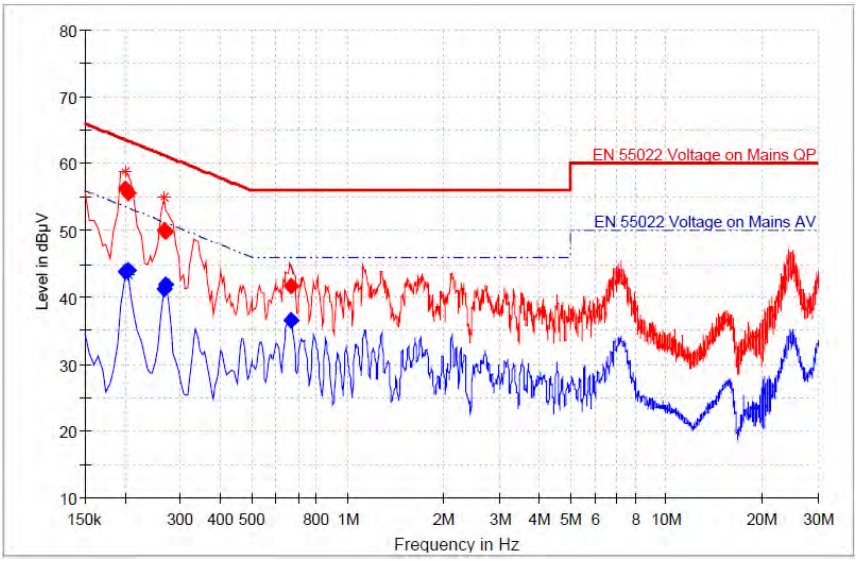


Figure 56 – EMI Test Results at 230 V.

Final_Result

Frequency (MHz)	QuasiPeak (dBµV)	Average (dBµV)	Limit (dBµV)	Margin (dB)	Bandwidth (kHz)	Line	Filter	Corr. (dB)
0.200000	---	43.78	53.61	9.83	10.000	L1	ON	20.3
0.200000	56.30	---	63.61	7.31	10.000	L1	ON	20.3
0.205000	---	44.06	53.41	9.34	10.000	L1	ON	20.3
0.205000	55.54	---	63.41	7.86	10.000	L1	ON	20.3
0.265000	---	41.31	51.27	9.96	10.000	L1	ON	20.3
0.265000	50.05	---	61.27	11.22	10.000	L1	ON	20.3
0.270000	---	41.94	51.12	9.17	10.000	L1	ON	20.3
0.270000	49.76	---	61.12	11.35	10.000	L1	ON	20.3
0.665000	---	36.58	46.00	9.42	10.000	L1	ON	20.4
0.665000	41.59	---	56.00	14.41	10.000	L1	ON	20.4

Table 15 – EMI Test Results at 230 V.

9.13 Line Immunity

9.13.1 Differential Surge Test

Repetition Rate: 1/60 s
Input Voltage VAC: 230 V
Passed ±2 kV Differential Surge Test.

Surge Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number of Strikes	Result
+2	0	L > N	2	5	PASS
+2	90	L > N	2	5	PASS
+2	180	L > N	2	5	PASS
+2	270	L > N	2	5	PASS
-2	0	L > N	2	5	PASS
-2	90	L > N	2	5	PASS
-2	180	L > N	2	5	PASS
-2	270	L > N	2	5	PASS

Table 16 – Differential Mode Surge Test Results.

9.13.2 Common Mode Surge Test

Repetition Rate: 1/60 s
Input Voltage VAC: 230 V
Passed ±2 kV Common Mode Surge Test.

Surge Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number of Strikes	Result
+2	0	L, N > PE	12	10	PASS
+2	90	L, N > PE	12	10	PASS
+2	180	L, N > PE	12	10	PASS
+2	270	L, N > PE	12	10	PASS
-2	0	L, N > PE	12	10	PASS
-2	90	L, N > PE	12	10	PASS
-2	180	L, N > PE	12	10	PASS
-2	270	L, N > PE	12	10	PASS

Table 17 – Common Mode Surge Test Results.

9.13.3 Ringwave Test

Repetition Rate: 1/60 s
Input Voltage VAC: 230 V
Passed ±4 kV Ringwave Test.

Surge Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number of Strikes	Result
+4kV	0	L, N > PE	12	10	PASS
+4kV	90	L, N > PE	12	10	PASS
+4kV	180	L, N > PE	12	10	PASS
+4kV	270	L, N > PE	12	10	PASS
-4kV	0	L, N > PE	12	10	PASS
-4kV	90	L, N > PE	12	10	PASS
-4kV	180	L, N > PE	12	10	PASS
-4kV	270	L, N > PE	12	10	PASS

Table 18 – Ring Wave Test Results.

9.14 ESD Test Results

The ESD tests were carried out at output full power, with the secondary GND connected to EARTH. Note that the negative terminals of all main outputs (CV1 and LED) are connected to the same (secondary) GND.

9.14.1 Line Input 115 VAC

Air Discharge (kV)	Result	Contact Discharge (kV)	Result
+10	PASS	+8	PASS
-10	PASS	-8	PASS
+15	PASS		
-15kV	PASS		
Extended Levels			
+16.5	PASS		
-16.5	PASS		

Table 19 – ESD Test Result, 115 VAC.

9.14.2 Line Input 230 VAC

Air Discharge (kV)	Result	Contact Discharge (kV)	Result
+10	PASS	+8	PASS
-10	PASS	-8	PASS
+15	PASS		
-15	PASS		
Extended Levels			
+16.5	PASS		
-16.5	PASS		

Table 20 – ESD Test Result, 230 VAC.

9.15 Thermal Performance

There are no heat sinks in cooling arrangements of the assembly. Copper pours are used for the cooling of the two control ICs – InnoMux2-BL IC and IML204DG IC. No forced air-cooling was deployed during any test. The temperatures of the hottest components in the assembly are shown in Table 21.

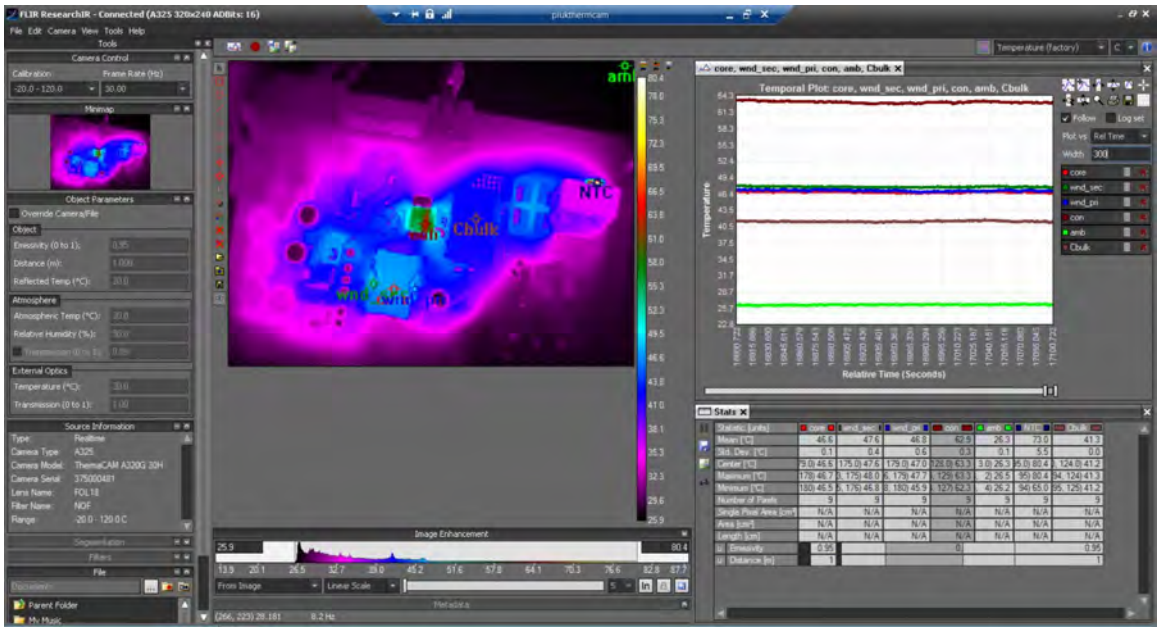


Figure 57 – Thermal Image Top View, 90 VAC, Full Power.

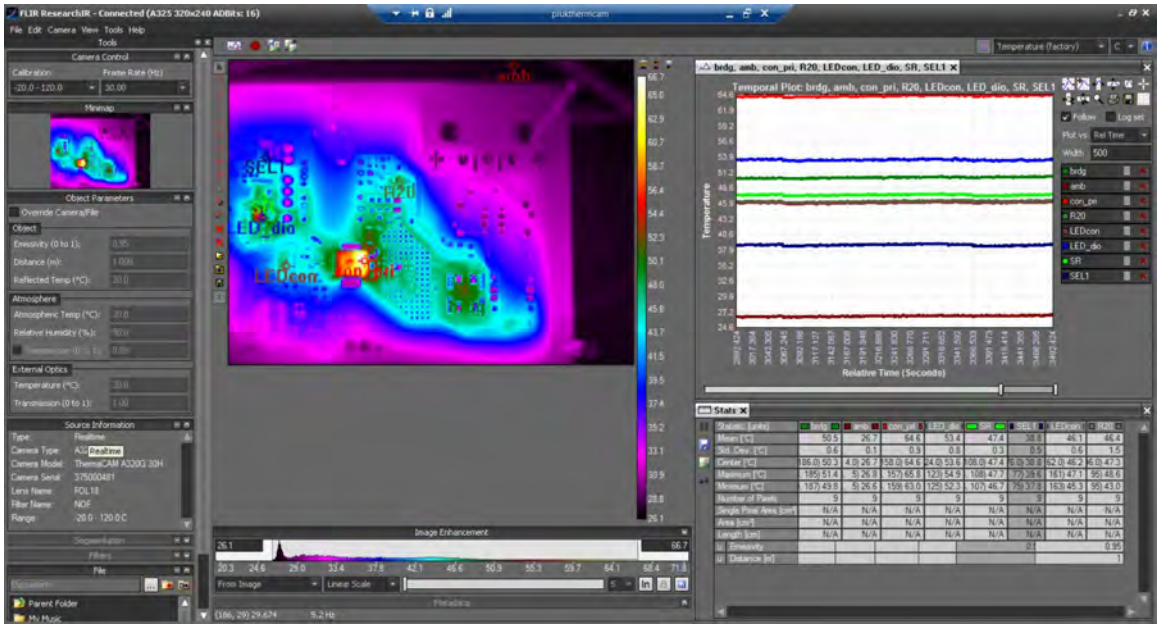


Figure 58 – Thermal Image Bottom View, 90 VAC, Full Power.

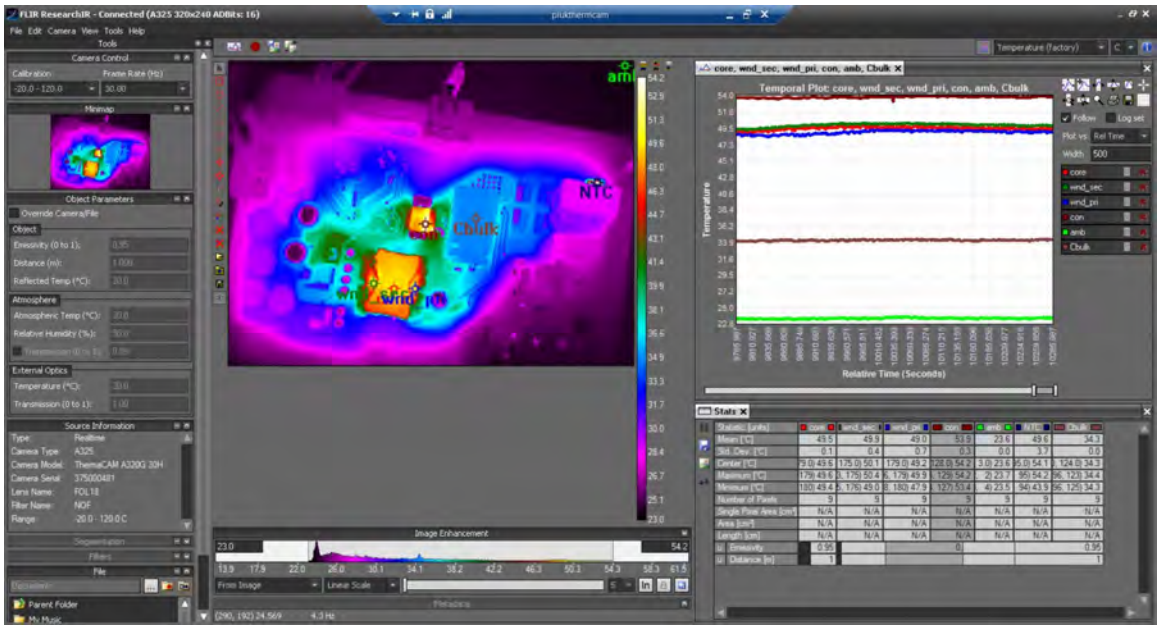


Figure 59 – Thermal Image Top View, 265 VAC, Full Power.

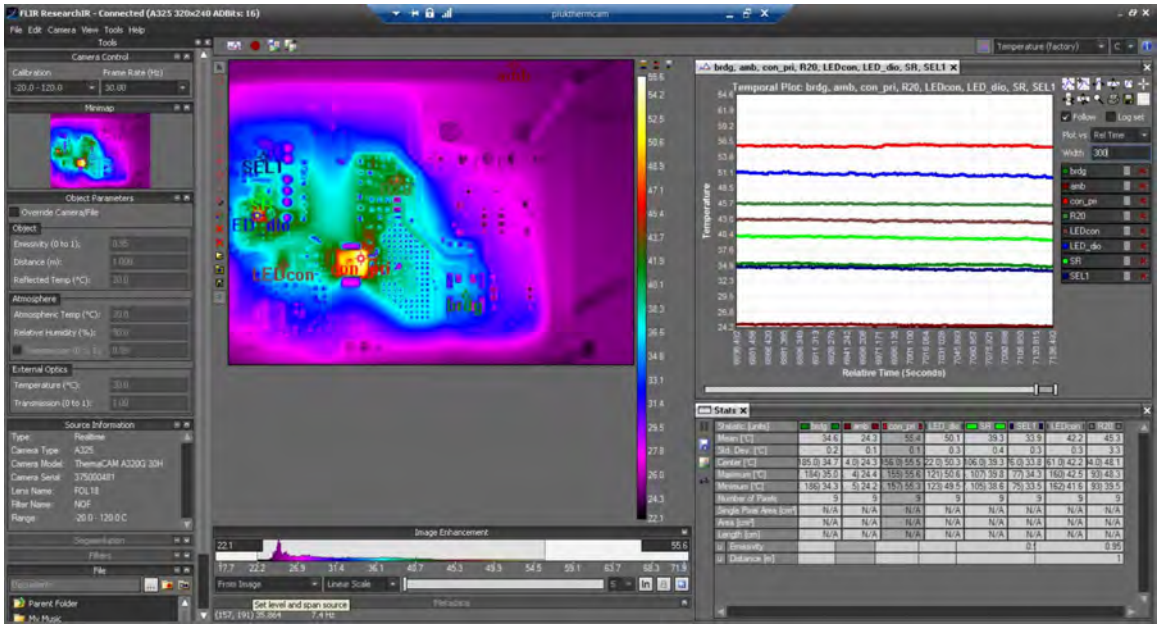


Figure 60 – Thermal Image Bottom View, 265 VAC, Full Power.

Component	Description	90 VAC			265 VAC		
		T [°C]	Ambient [°C]	ΔT [°C]	T [°C]	Ambient [°C]	ΔT [°C]
U1	InnoMux2-BL Pri	64.6	26.7	37.9	55.4	24.3	31.1
Q2	Selection FET	38.8	26.7	12.1	33.9	24.3	9.6
D1	LED Diode	53.4	26.7	26.7	50.1	24.3	25.8
Q1	SR FET	47.4	26.7	20.7	39.3	24.3	15
BR1	Bridge	50.5	26.7	23.8	34.6	24.3	10.3
U2	IML204DG	46.1	26.7	19.4	42.2	24.3	17.9
T1	Trf_winding_pri	46.8	26.3	20.5	49	23.6	25.4
T1	Trf_winding_sec	47.6	26.3	21.3	49.9	23.6	26.3
T1	Trf_core	46.6	26.3	20.3	49.5	23.6	25.9
R3	NTC	73	26.3	46.7	49.6	23.6	26
C3	Bulk Cap	41.3	26.3	15	34.3	23.6	10.7

Table 21 – Component Temperatures, 90 VAC and 265 VAC, Full Power.

9.16 Audible Noise Performance

The audible noise measurements are shown below. These were obtained covering below test conditions:

- 115 V, 230 V input line voltages
- LED = 45 V @ 0 – 400 mA
- CV1 = 5 V @ 0 – 1.2 A

The passing criteria for the test is that audible noise must not surpass 28 dBA during normal operation mode (LED enabled) and 24 dBA during standby operation mode (LED disabled, CV1 output power <500 mW).

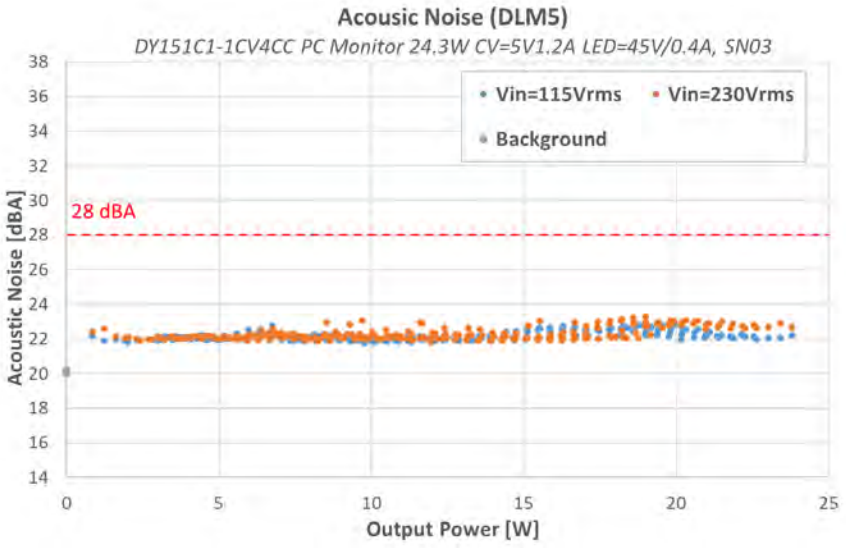


Figure 61 – Audible Noise at Normal Operation Mode.

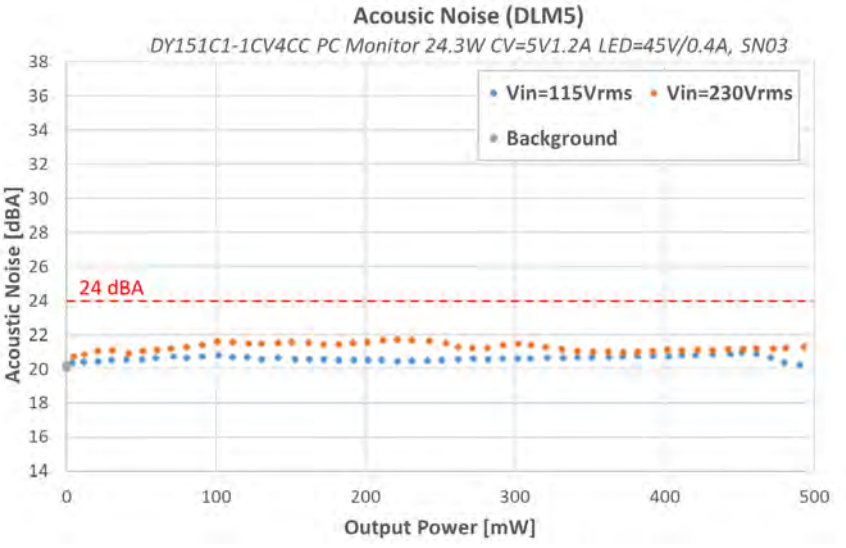


Figure 62 – Audible Noise at Standby Mode.

10 Revision History

Date	Author	Revision	Description & Changes	Reviewed
26-Feb-24	HC	1.0	Initial Release	Apps & Mktg

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