Design Example Report

Title	***4 W High Power Factor (>0.94 Typical) Non-Isolated Buck-Boost GU10 TRIAC Dimmable LED Driver Using LinkSwitch™-PL LNK456DG***
Specification	190 VAC – 265 VAC Input; 100 V_{TYP}, 40 mA Output
Application	GU10 LED Driver
Author	Applications Engineering Department
Document Number	DER-335
Date	December 11, 2012
Revision	1.0

Summary and Features

- Single-stage power factor correction combined with constant current (CC) output
- TRIAC dimmable
  - Works with a wide selection of TRIAC dimmers from 300 W to 1200 W
  - Fast start-up time (<200 ms) – no perceptible delay
- Low cost, low component count, small size and single-sided PCB
- Integrated protection and reliability features
  - Output short-circuit protected with auto-recovery
  - Auto-recovering thermal shutdown with large hysteresis
  - No damage during brown-out conditions
- PF >0.94 at 230 VAC
- Meets IEC ring wave, differential line surge and EN55015 conducted EMI
- Open load protection

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Table of Contents

Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

The document describes a non-isolated, high power factor (PF), TRIAC dimmable LED driver designed to drive a nominal LED string voltage of 100 V at 40 mA from an input voltage range of 190 VAC to 265 VAC (50 Hz typical). The LED driver utilizes the LNK456DG from the LinkSwitch-PL family of ICs.

The topology used is a single-stage non-isolated buck-boost that meets high power factor, constant current regulation, and dimming requirements for this design.
LinkSwitch-PL based designs provide a high power factor (>0.94) meeting international requirements.

This document contains the LED driver specification, schematic, PCB details, bill of materials, transformer documentation and typical performance characteristics.

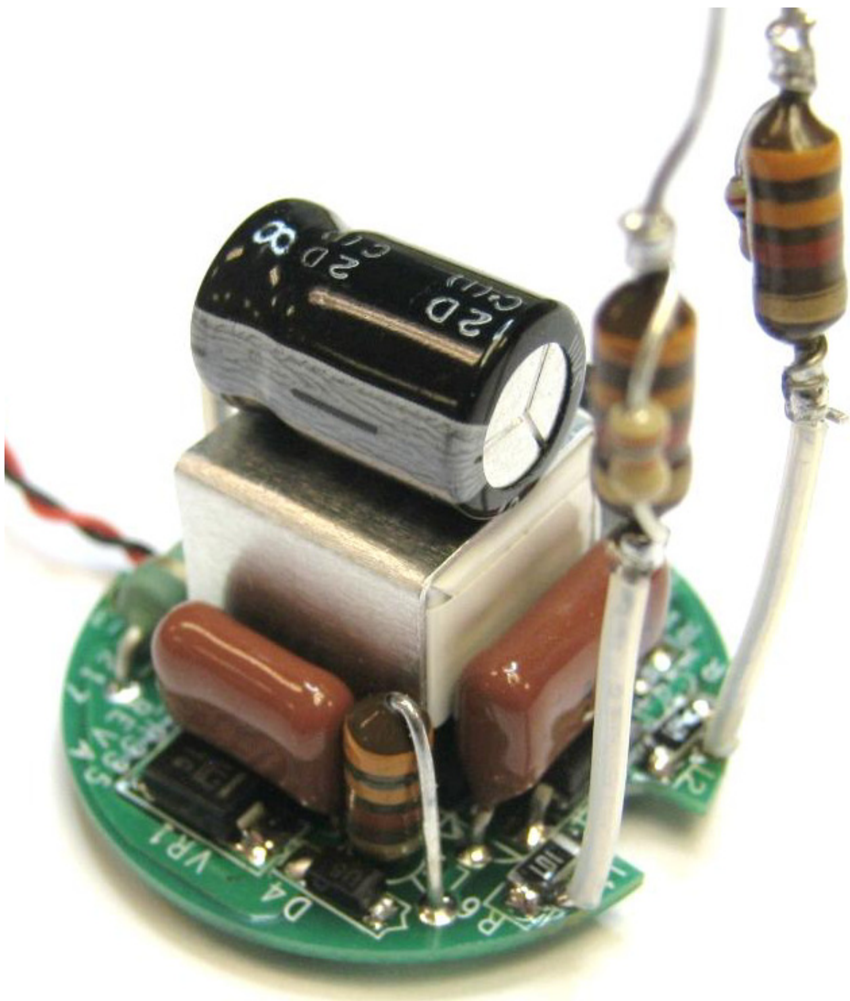

Figure 1 – Populated Circuit Board.

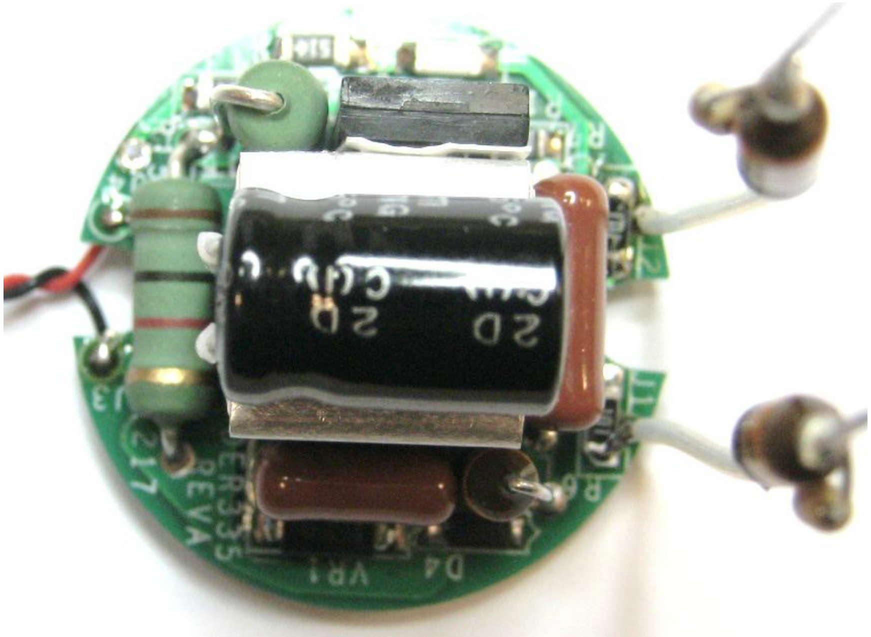

Figure 2 – Populated Circuit Board, Top View.

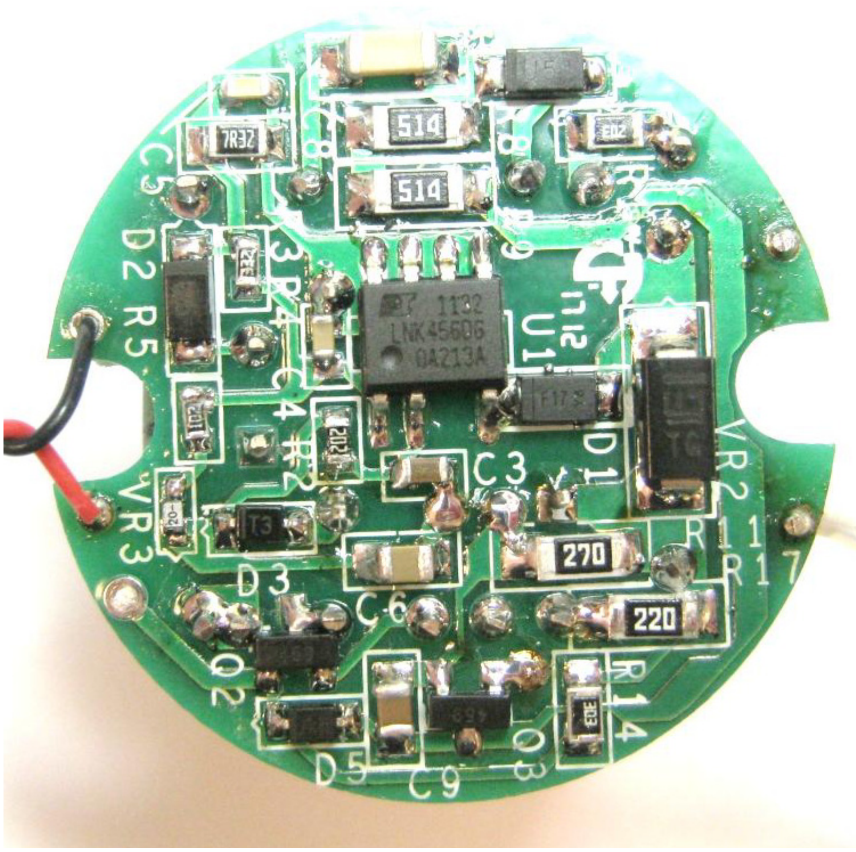

Figure 3 – Populated Circuit Board, Bottom View.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	190	230	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}		50		Hz	
Output						
Output Voltage	V_{OUT}		100		V	
Output Current	I_{OUT}		40		mA	V_{OUT} = 40 V, V_{IN} = 230 VAC, 25 °C
Total Output Power						
Continuous Output Power	P_{OUT}		4		W	
Efficiency						
Full Load	η	74			%	Measured at P_{OUT} 25 °C
Environmental						
Conducted EMI		CISPR 15B / EN55015B				
Safety		Non-Isolated				
Ring Wave (100 kHz)						
Differential Mode (L1-L2)			2.5		kV	
Common mode (L1/L2-PE)						
Differential Surge			500		V	
Power Factor			0.94			Measured at $V_{OUT(TYP)}$, $I_{OUT(TYP)}$ and 230 VAC, 50 Hz
Harmonic Currents		EN 61000-3-2 Class D (C)				Class C specifies Class D Limits when P_{IN} <25 W
Ambient Temperature	T_{AMB}		50		°C	Free convection, sea level

3 Schematic

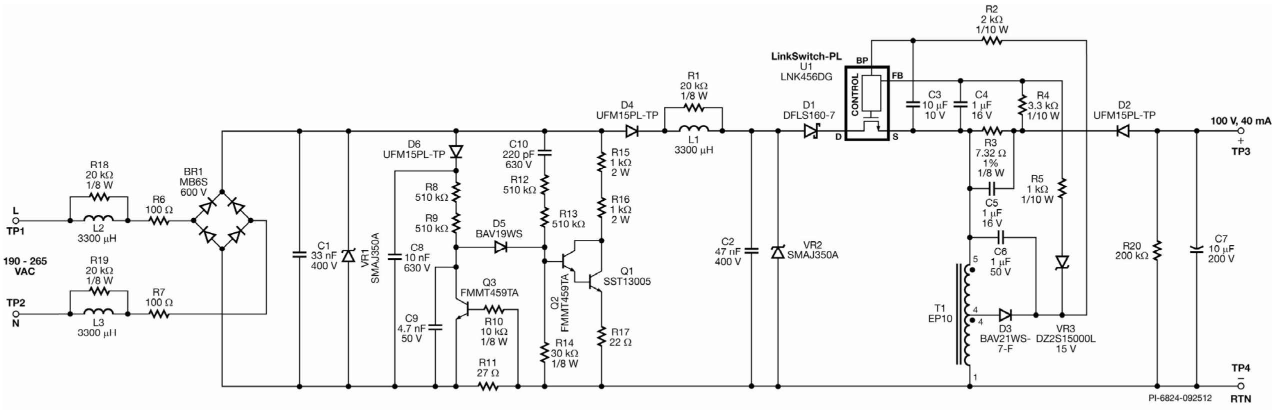

Figure 4 – Schematic Diagram.

Notes:

1) R20 was added as a post-production operation.
2) Resistor R18, L2, R19 and L3 are mounted in line to the AC input terminal of enclosure.

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4 Circuit Description

The LinkSwitch-PL (U1) is a highly integrated primary side controller designed for use in LED driver applications. The LinkSwitch-PL provides high power factor while regulating the output current across a range of input (190 VAC to 265 VAC) in a single conversion stage. The design also supports the output voltage variations typically encountered in LED driver applications. All of the control circuitry responsible for these functions plus the high-voltage power MOSFET was incorporated into the IC.

4.1 Input EMI Filtering

Resistors R6 and R7 is used as passive damper during dimming. Zener diodes VR1 and VR2 make a clamp to limit the maximum voltage during differential line surge events. These diodes were added to increase immunity to differential line surge. These diodes are needed because of the absence of input capacitance. Bridge rectifier BR1 rectifies the AC line voltage with capacitor C2 providing a low impedance path (decoupling) for the primary switching current. A low value of capacitance (sum of C1 and C2) is necessary to maintain a power factor of greater than 0.9.

EMI filtering is provided by inductors L1, L2 and L3, and capacitors C1 and C2. Resistor R1, R18 and R19 across L1, L2 and L3 damp the self-resonances of the inductors to avoid noise peaking in the conducted EMI plot at the resonant frequency of these inductors.

4.2 Power Circuit

The circuit is a buck-boost converter. Diode D2 is the rectifier diode with cathode connected to the current sense resistor R3. The DRAIN (D) pin of U1 is connected to the positive side of the DC rectified input through D1. Diode D1 is used to prevent reverse current from flowing through U1 when T1 resonates during off-time. An EP10 core size inductor is optimized for highest system efficiency.

Capacitor C3 provides local decoupling for the BYPASS (BP) pin of U1 which is the supply pin for the internal controller. During start-up, C3 is charged to 6 V from an internal high-voltage current source connected to the DRAIN pin. Once charged U1 starts switching at which point the operating supply current is also provided from the T1 inductor via R2 and C6. A bias voltage was derived from the main inductor T1 to provide supply bypass voltage during dimming operation where the supply from the drain is not available.

4.3 Output Feedback

Resistor R3 is used to sense the output current (off-time inductor current) of the buck-boost converter. Resistor R3 is selected to give an average value of 290 mV into the FEEDBACK (FB) pin when I_{OUT} nominal is flowing into it. Resistor R4 and capacitor C4 provide filtering to lower the ripple voltage feed to the FEEDBACK pin of U1 for improved regulation.

4.4 TRIAC Phase Dimming Control Compatibility

The requirements to provide output dimming with low cost, TRIAC based, leading edge and trailing edge phase dimmers introduced some trade-offs in the design.

Due to the much lower power consumed by LED based lighting, the current drawn by the overall lamp is below the holding current of the TRIAC within many dimmers. This causes undesirable behavior such as limited dimming range and/or flickering. The relatively large impedance presented to the line by the LED allows significant ringing to occur due to the inrush current charging the input capacitance when the TRIAC turns on. This effect can cause similar undesirable behavior, as the ringing may cause the TRIAC current to fall to zero and turn off.

To overcome these issues, the passive damper and active bleeder were incorporated. The drawback of these circuits is increased dissipation and therefore reduced efficiency of the driver. For non-dimming application these components can simply be omitted.

The passive damper consists of resistors R6 and R7 to dampen the input network during TRIAC dimming. Resistors R6 and R7 were also chosen to withstand the high instantaneous power during differential line surge testing.

The active bleeder circuit is comprised of two sections. Components C10, R12, R13, R14, Q1, Q2, R15, R16, and R17 are used to provide latching current and damping to keep the TRIAC conducting. This network is a replacement for a bulky passive RC bleeder. A typical passive RC bleeder with capacitance of 3 to 5 times of the total input capacitance is replaced by an active RC which dramatically reduce the space occupied by a traditional passive RC. The exponential decay characteristic is set by components C10, R12, R13 and R14. The voltage developed across R14 is translated to an amplified exponential current decay flowing into Q1. The Darlington connection of Q1 and Q2 provides a high current gain necessary to keep a higher resistance value for R12 and thus minimize the size of capacitor C10. Resistor R15 and R16 limit the maximum peak current at Q1 and also absorb most of the dissipation required by the active bleeder network. Resistor R14 is chosen such that at non-dimming (no TRIAC) condition, Q1 is off.

The other section of the active bleeder serves the purpose of maintaining a holding current drawn by the converter from the input to keep the TRIAC conducting. The current drawn by the converter is sensed through R11. A minimum current of Vbe_{Q3}/R11 is maintained by regulating the collector voltage of Q3. If the input current drawn by the LED driver is less than the holding current setting, Q3 collector goes high and D5 is forward biased to keep the input current above the holding current of the TRIAC. If the input current drawn by the driver is greater than the set holding current, D5 anode is pulled down by Q3.

The active bleeder function of maintaining the input current above a specified threshold (set holding current) keeps the TRIAC conducting. The drawback is increased input

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power due to the power dissipated by the active bleeder. This power is shared by R15, R16 and Q1. Power dissipation of this network increases with line voltage, and decreasing output power.

Worst case active bleeder dissipation occurs during maximum input line fault condition such as OVP and short-circuit. During these fault conditions, the LED driver draws a small amount of power from the line since U1 forced the converter to operate into cycle skipping mode. The active bleeder however still does its function by keeping the input current above the holding current and dissipates all the power necessary to keep the TRIAC conducting.

As shown, Q1, R15 and R16 are not designated to operate under prolonged fault conditions (either shorted or disconnected LED load) and will overheat.

5 PCB Layout

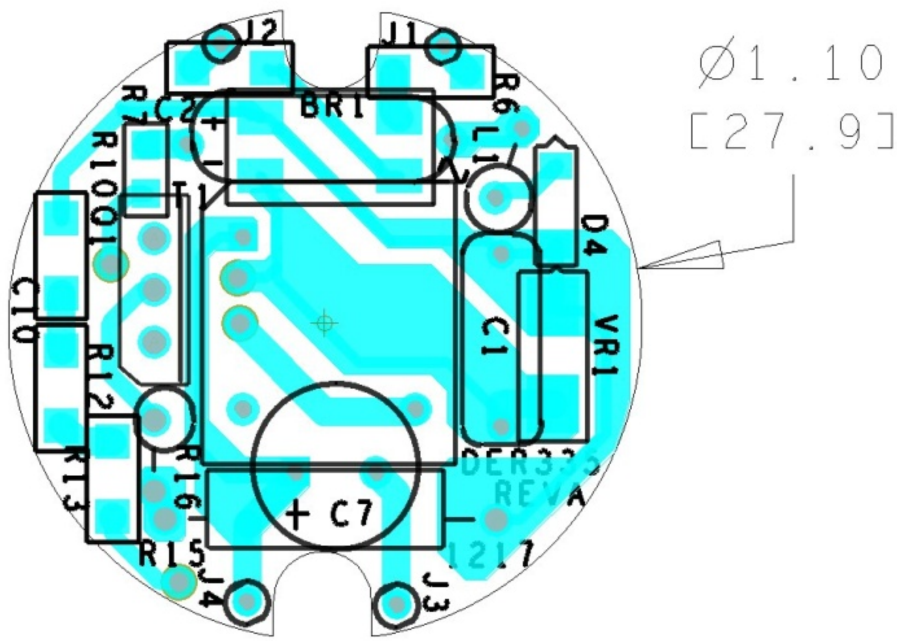

Figure 5 – Top Side.

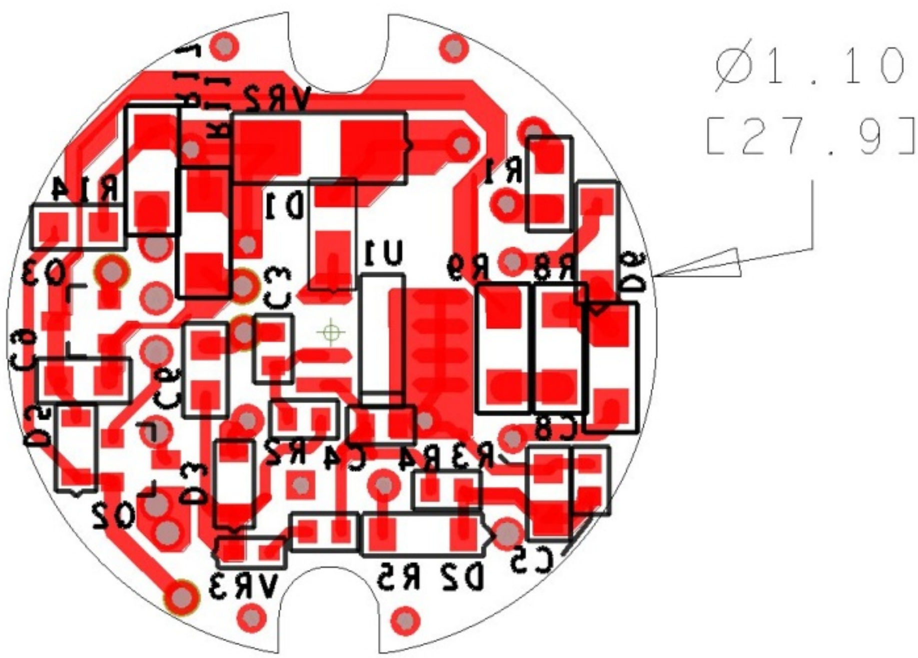

Figure 6 – Bottom Side.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 0.5 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	MB6S-TP	Micro Commercial Co
2	1	C1	33 nF, 400 V, Film	ECQ-E4333KF	Panasonic
3	1	C2	47 nF, 400 V, Film	ECQ-E4473KF	Panasonic
4	1	C3	10 μF, 10 V, Ceramic, X5R, 0603	C1608X5R1A106M	TDK
5	2	C4 C5	1 μF, 16 V, Ceramic, X5R, 0603	GRM188R61C105KA93D	Murata
6	1	C6	1 μF, 50 V, Ceramic, X7R, 0805	C2012X7R1H105M	TDK
7	1	C7	10 μF, 200 V, Electrolytic, (8 x 11)	SMQ200VB10RM8X11LL	Nippon Chemi-Con
8	1	C8	10 nF, 630 V, Ceramic, X7R, 1206	C1206C103KBRACTU	Kemet
9	1	C9	4.7 nF, 50 V, Ceramic, X7R, 0805	08055C472KAT2A	AVX
10	1	C10	220 pF, 630 V, Ceramic, NPO, 1206	C3216C0G2J221J	TDK
11	1	D1	60 V, 1 A, Diode Schottky, PWRDI 123	DFLS160-7	Diodes, Inc.
12	3	D2 D4 D6	600 V, 1 A, Ultrafast Recovery, 75 ns, SOD-123	UFM15PL-TP	Micro Commercial
13	1	D3	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
14	1	D5	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
15	3	L1 L2 L3	3300 μH, 62 mA, 59.5 Ω, Axial Ferrite Inductor	B78108S1335J	Epcos
16	1	Q1	NPN, NPN Fast SW BIPO SOT-32, TO-126-3	STT13005	ST Micro
17	2	Q2 Q3	NPN, Small Signal BJT, 450 V, 0.5 A, 150 MA, SOT-23	FMMT459TA	Diodes, Inc.
18	1	R1	20 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ203V	Panasonic
19	1	R2	2 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ202V	Panasonic
20	1	R3	7.32 Ω, 1%, 1/8 W, Thick Film, 0805	RC0805FR-077R32L	Yageo
21	1	R4	3.3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ332V	Panasonic
22	1	R5	1 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
23	2	R6 R7	100 Ω, 5%, 1/4 W, Pulse Proof, Thick Film, 1206	SR1206JR-07100RL	Yageo
24	4	R8 R9 R12 R13	510 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ514V	Panasonic
25	1	R10	10 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
26	1	R11	27 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ270V	Panasonic
27	1	R14	30 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ303V	Panasonic
28	2	R15 R16	1.0 kΩ, 5%, 2 W, Metal Oxide	RSMF2JT1K00	Stackpole
29	1	R17	22 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ220V	Panasonic
30	2	R18 R19	20 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-20K	Yageo
31	1	R20	200 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ204V	Panasonic
32	1	T1	Bobbin, EP10, Horizontal, 8 pins Transformer	 SNX-R1685	Phillips Santronics USA
33	1	U1	LinkSwitch-PL, SO-8C	LNK456DG	Power Integrations
34	2	VR1 VR2	350 V, 400 W, 5%, DO214AC (SMA)	SMAJ350A	LittleFuse
35	1	VR3	15 V, 5%, 150 mW, SSMINI-2	DZ2S15000L	Panasonic

7 Inductor Specification

7.1 Electrical Diagram

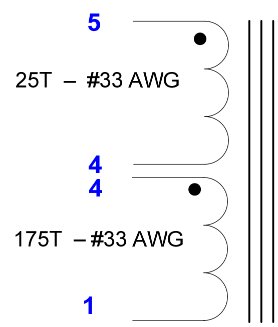

Figure 7 – Inductor Electrical Diagram.

7.2 Electrical Specifications

Primary Inductance	Pins 1-5, all other windings open, measured at 66 kHz, 0.4 V_{RMS}	1160 μH ±7%
Resonant Frequency	Pins 1-5, all other windings open	1.5 MHz (Min.)

7.3 Materials

Item	Description
[1]	Core: EP10-3F3 or equivalent.
[2]	Bobbin: CSH-EP10-1S-8P.
[3]	Tape, Polyester film, 3M 1350F-1 or equivalent, 5.6 mm wide.
[4]	Magnet Wire, #33 AWG, solderable double coated.

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7.4 Inductor Build Diagram

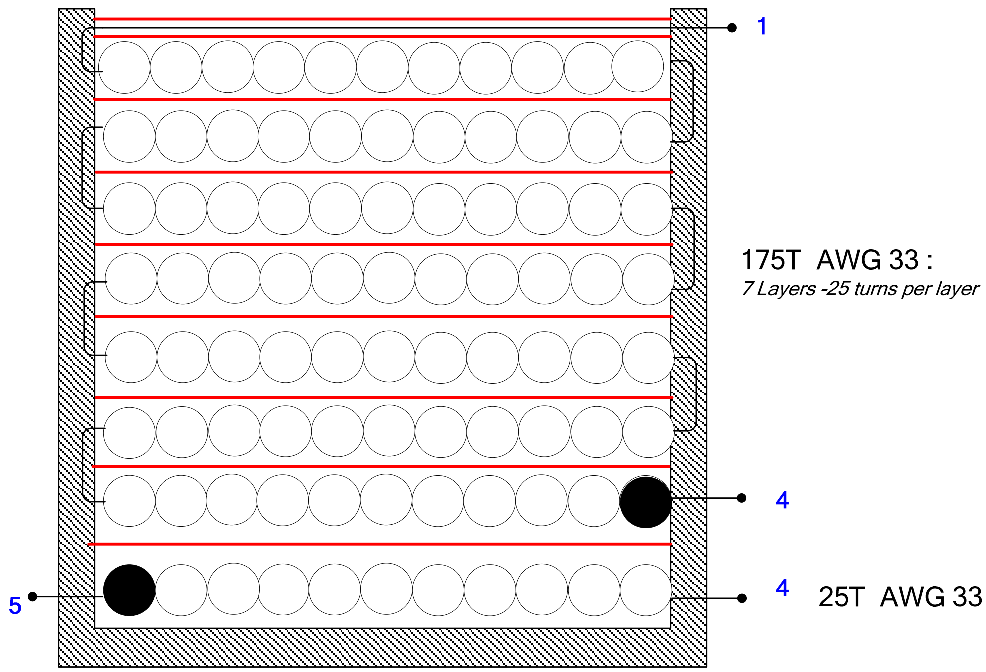

Figure 8 – Inductor Build Diagram.

7.5 Inductor Construction

General Note	For the purpose of these instructions, bobbin is oriented on winder such that pin 1 side is on the right.
WD1	Start at pin 5. Wind 25 turns of item [3] as shown in Figure 2. Terminate at pin 4.
WD2	Start at pin 4. Wind 175 turns of item [3] and terminate the other end at pin 1. Add 1 layer of tape per layer (7 layers, 25T per layer).
Finish	Grind the core to get the specified inductance. Apply tape to secure both cores. Cut pins 2, 3, 6, 7, and 8.

8 Inductor Design Spreadsheet

ACDC_LinkSwitch-PL-Buck-Boost_120211; Rev.1.1; Copyright Power Integrations 2011	INPUT	OUTPUT	UNIT	LinkSwitch-PL Buck-Boost Design Spreadsheet
ENTER APPLICATION VARIABLES				
VACMIN	190	190	V	Minimum AC input voltage
VACNOM	230	230	V	Nominal AC input voltage
VACMAX	265	265	V	Maximum AC input voltage
FL		50	Hz	Minimum line frequency
VO_MIN	95.00	95.0	V	Minimum output voltage tolerance
VO_NOM	100.00	100.00	V	Nominal Output Voltage
VO_MAX	105.00	105.00	V	Maximum output voltage tolerance
IO	0.040	0.040	A	Average output current specification
n	0.89	0.890	%/100	Total power supply efficiency
Z		0.5		Loss allocation factor
Enclosure	Retrofit Lamp	Retrofit Lamp		Enclosure selections determines thermal conditions and maximum power
PO	4	4.00	W	Total output power
VD	0.70	0.7	V	Output diode forward voltage drop
LinkSwitch-PL DESIGN VARIABLES				
Device	LNK456	LNK456		Chosen LinkSwitch-PL Device
TON		1.56	us	Expected on-time of MOSFET at low line and PO
FSW		77.1	kHz	Expected switching frequency at nominal line and PO
Duty Cycle		12.0	%	Expected operating duty cycle at nominal line and PO
VDRAIN		500	V	Estimated worst case drain voltage at VACMAX and VO_MAX
IRMS		0.062	A	Nominal RMS current through the switch
IPK		0.509	A	Worst Case Peak current
ILIM_MIN		0.510	A	Minimum device current limit
KDP		2.27		Ratio between off-time of switch and reset time of core at VACNOM
LinkSwitch-PL EXTERNAL COMPONENT CALCULATIONS				
RSENSE		7.250	Ohms	Output current sense resistor
Standard RSENSE		7.32	Ohms	Closest 1% value for RSENSE
PSENSE		11.6	mW	Power dissipated by RSENSE
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES				
Core Type		EP10		Core Type
Core Part Number	**EP10**			If custom core is used - Enter part number here
Bobbin Part Number		Custom		Bobbin Part Number (if available)
AE	11.30	11.30	mm^2	Core Effective Cross Sectional Area
LE	19.30	19.30	mm	Core Effective Path Length
AL	790	790	nH/T^2	Ungapped Core Effective Inductance
BW	5.60	5.6	mm	Bobbin Physical Winding Width
L	8	8		Number of winding layers
TRANSFORMER PRIMARY DESIGN PARAMETERS				
LP	1160.00	1160.0	uH	Typical inductance (Includes inductance of input and output winding)
LP Tolerance	5.00	7	%	Tolerance of Primary Inductance
N	200	200	Turns	Number of Turns
ALG		29	nH/T^2	Gapped Core Effective Inductance
BM		2611	Gauss	Operating Flux Density
BAC		1305	Gauss	Worst case AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
BP		3570	Gauss	Calculated Worst Case Peak Flux Density (BP <

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				3600 G)
LG		0.490	mm	Gap Length (Lg > 0.1 mm)
BWE		44.8	mm	Effective Bobbin Width
L_IRMS		0.134	A	RMS Curren through the inductor
OD		0.22	mm	Maximum Primary Wire Diameter including insulation
INS		0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.18	mm	Bare conductor diameter
AWG		34	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		40	Cmils	Bare conductor effective area in circular mils
CMA		300	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
Current Density (J)		6.68	A/mm^2	Inductor Winding Current density (3.8 < J < 9.75 A/mm^2)
Output Parameters				
IRIPPLE?				Maximum Capacitor Ripple Current
IO		0.040	A	Expected Output Current
PIVS		528.5	V	Peak Inverse Voltage at VO_MAX on output diode

9 Dimming Configuration Performance Data

All measurements performed at room temperature using an LED load. The following data were measured using 3 sets of loads to represent the load range of 97 V to 103 V output voltage. Refer to the table on Section 9.6 for the complete set of test data values.

9.1 Efficiency

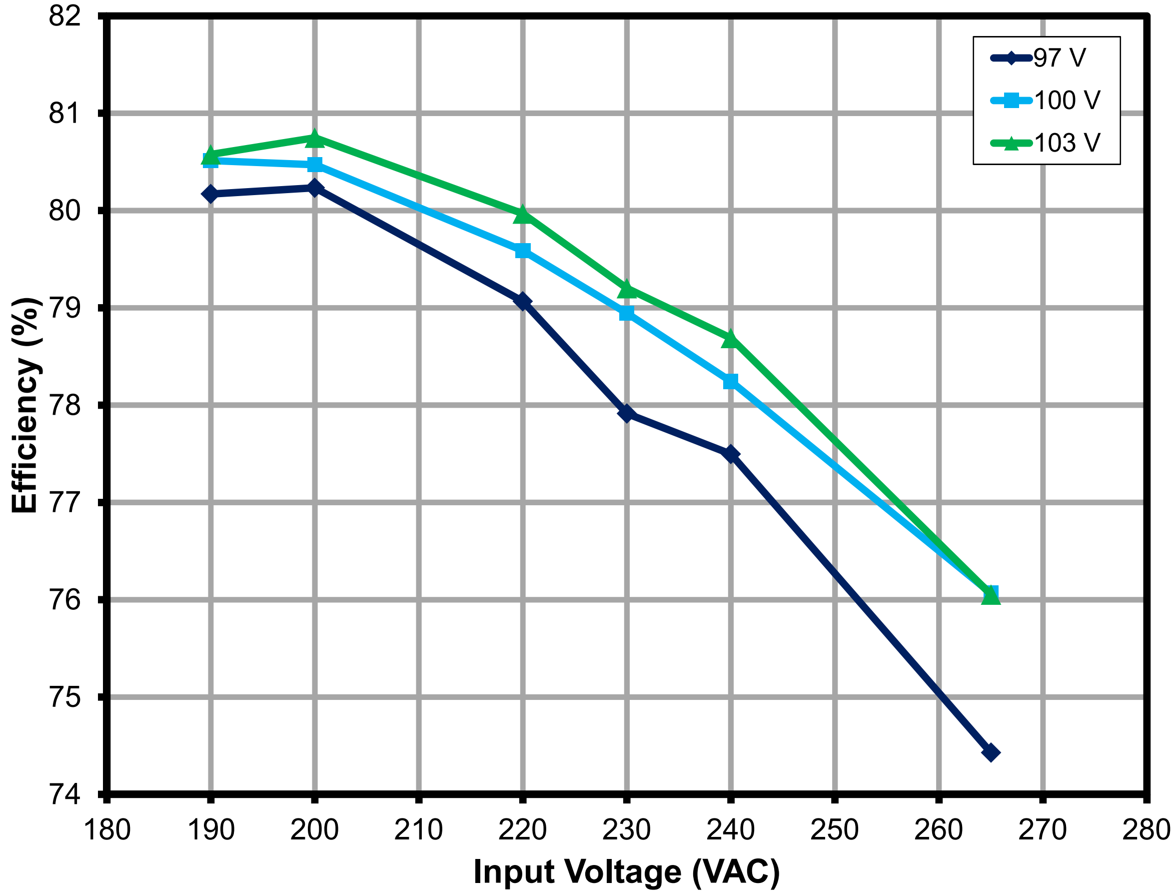

Figure 9 – Efficiency vs. Line and Load.

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9.2 Line and Load Regulation

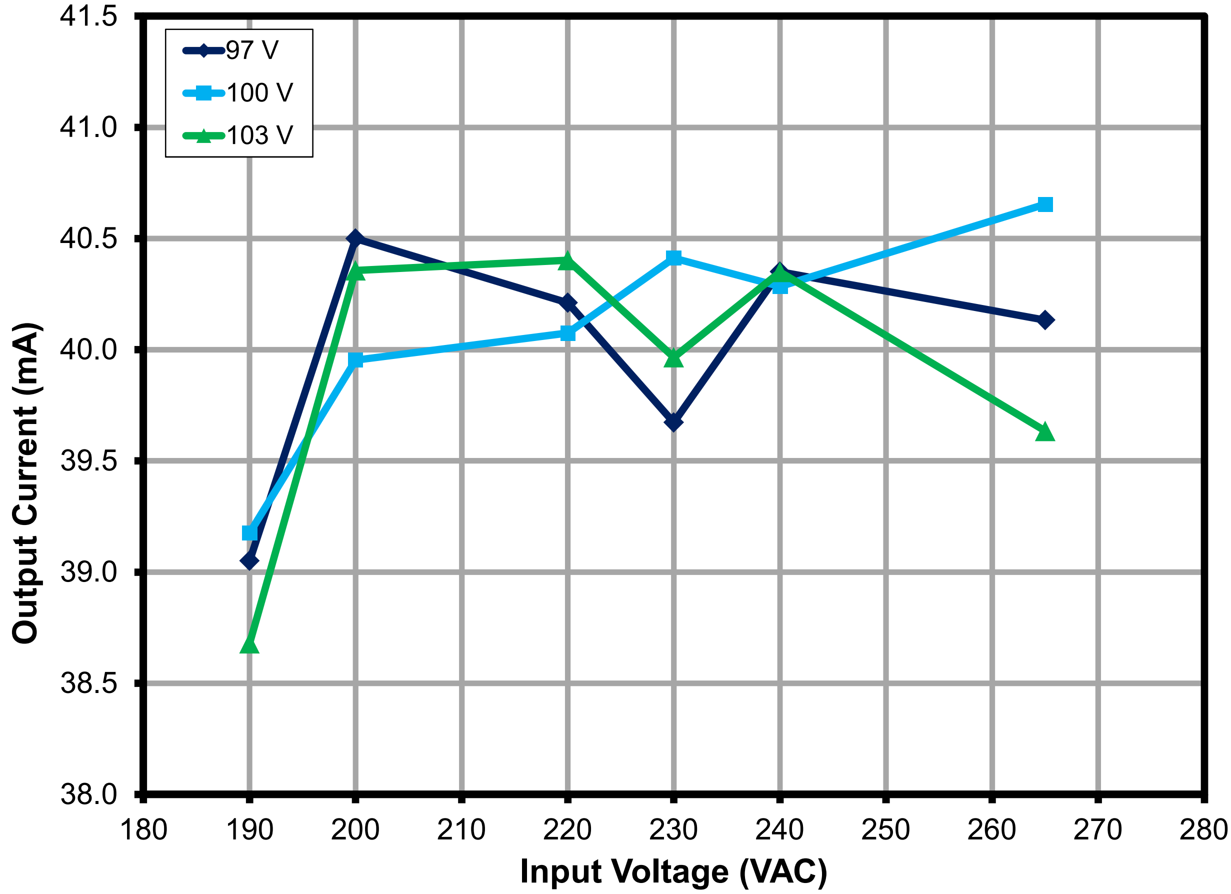

Figure 10 – Regulation vs. Line and Load

9.3 Power Factor

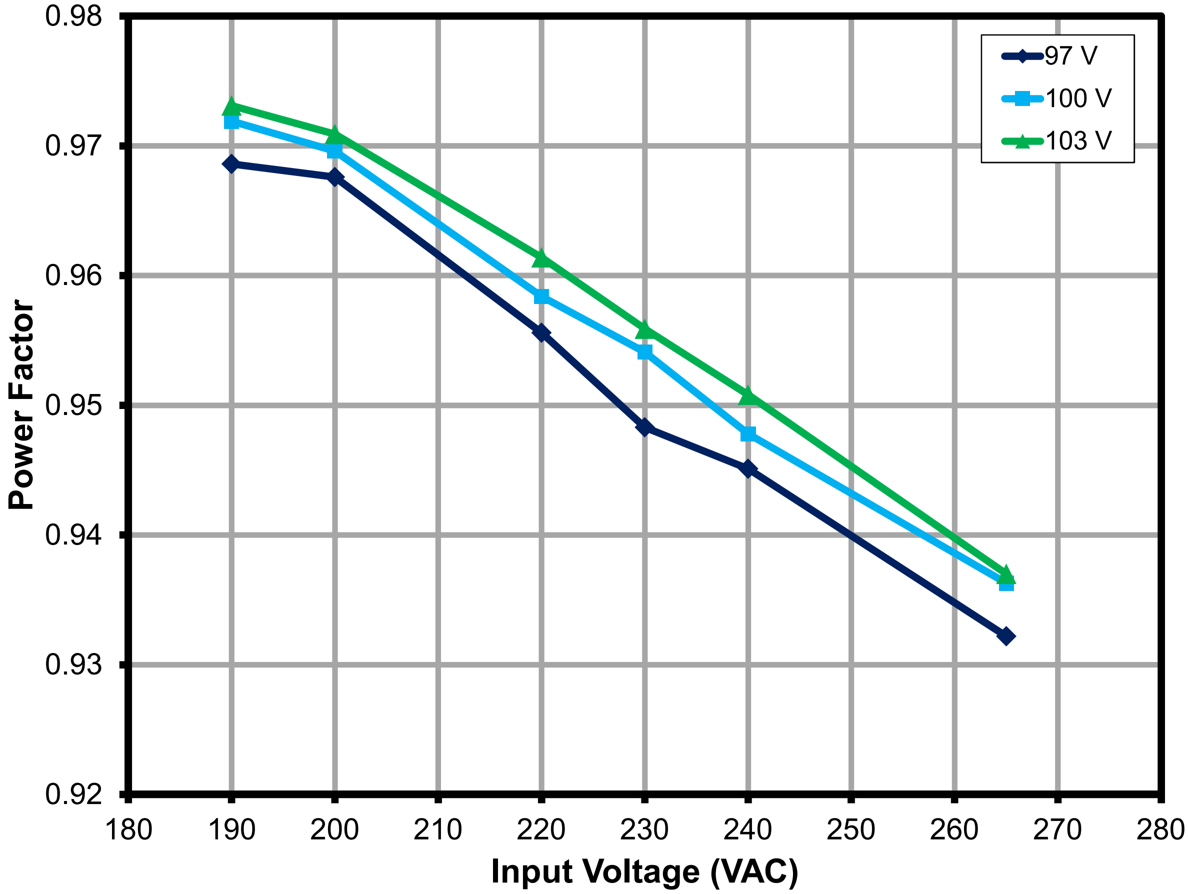

Figure 11 – Power Factor vs. Line and Load

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9.4 A-THD

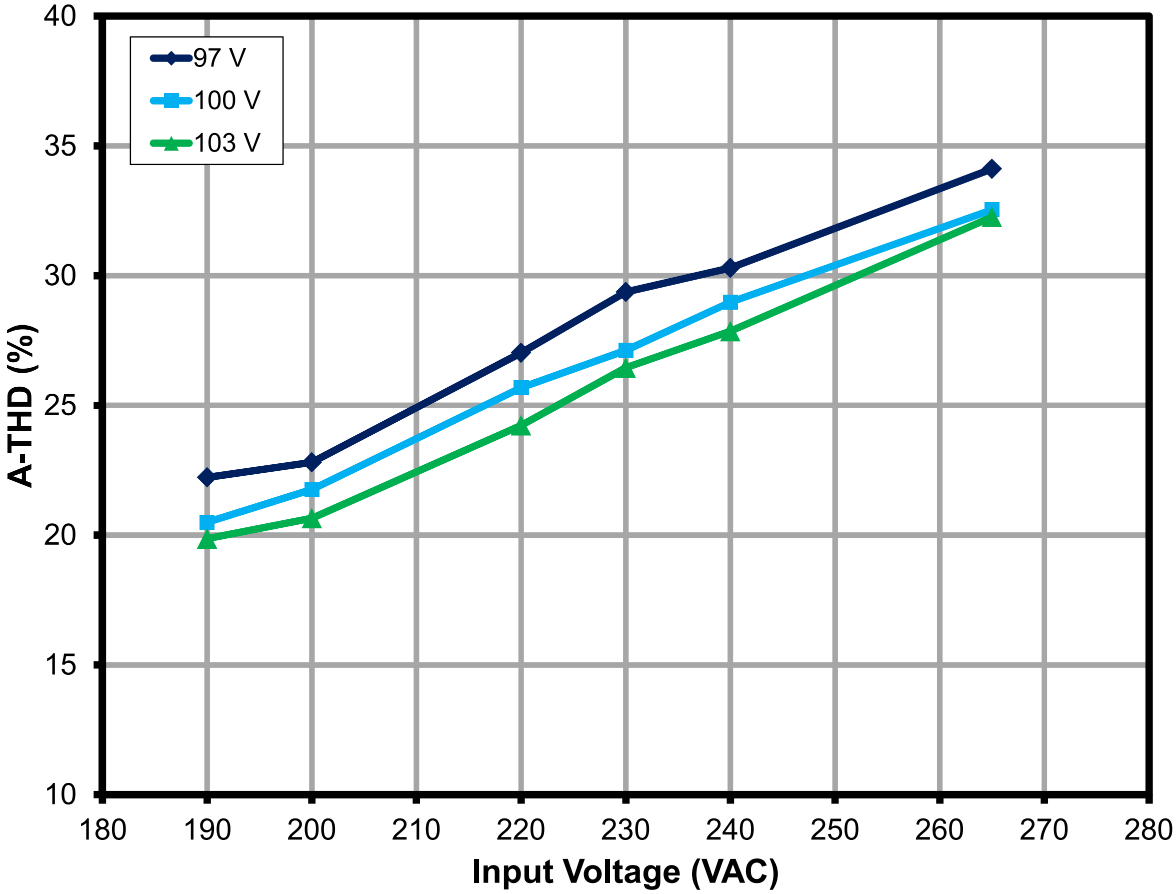

Figure 12 – A-THD vs. Line and Load.

9.5 Harmonics

The design met the limits for Class C equipment for an active input power of <25 W. In this case IEC61000-3-2 specifies that harmonic currents shall not exceed the limits of Class D equipment[1]. Therefore the limits shown in the charts below are Class D limits which must not be exceeded to meet Class C compliance.

9.5.1 97 V LED Load

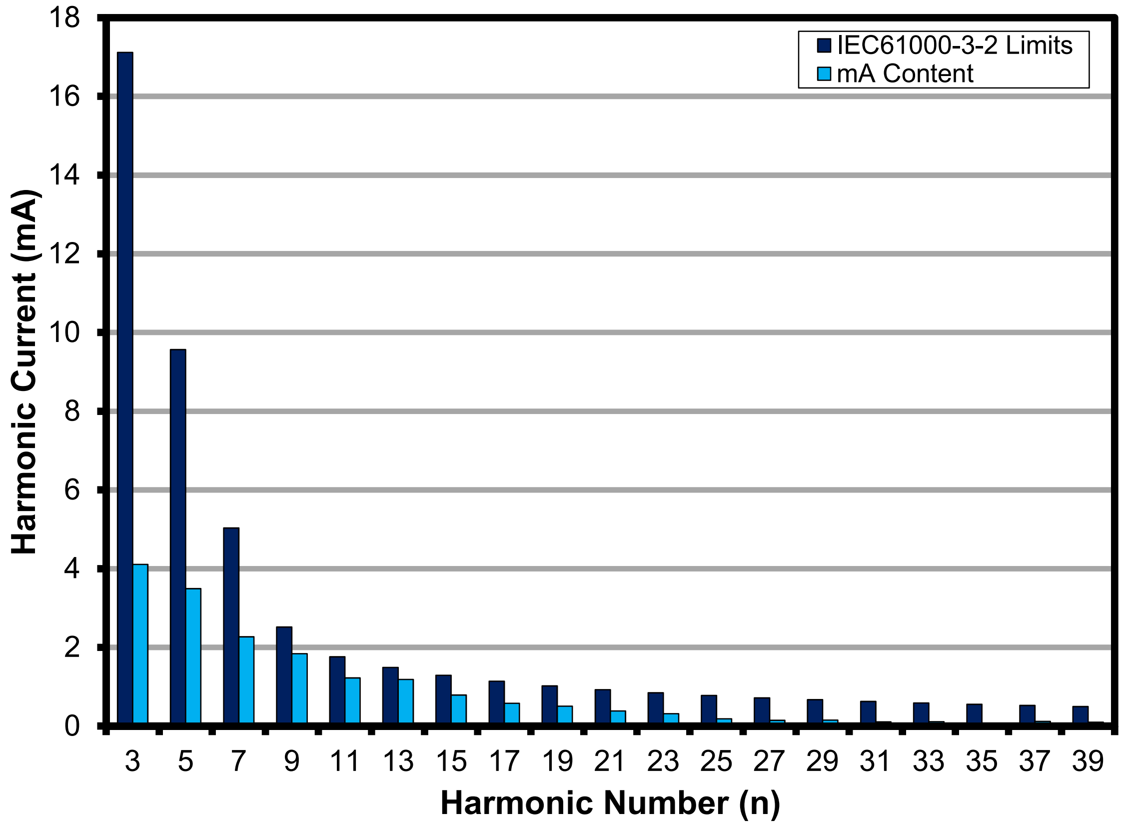

Figure 13 – 97 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

[1] IEC6000-3-2 Section 7.3, table 2, column 2.

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9.5.2 100 V LED Load

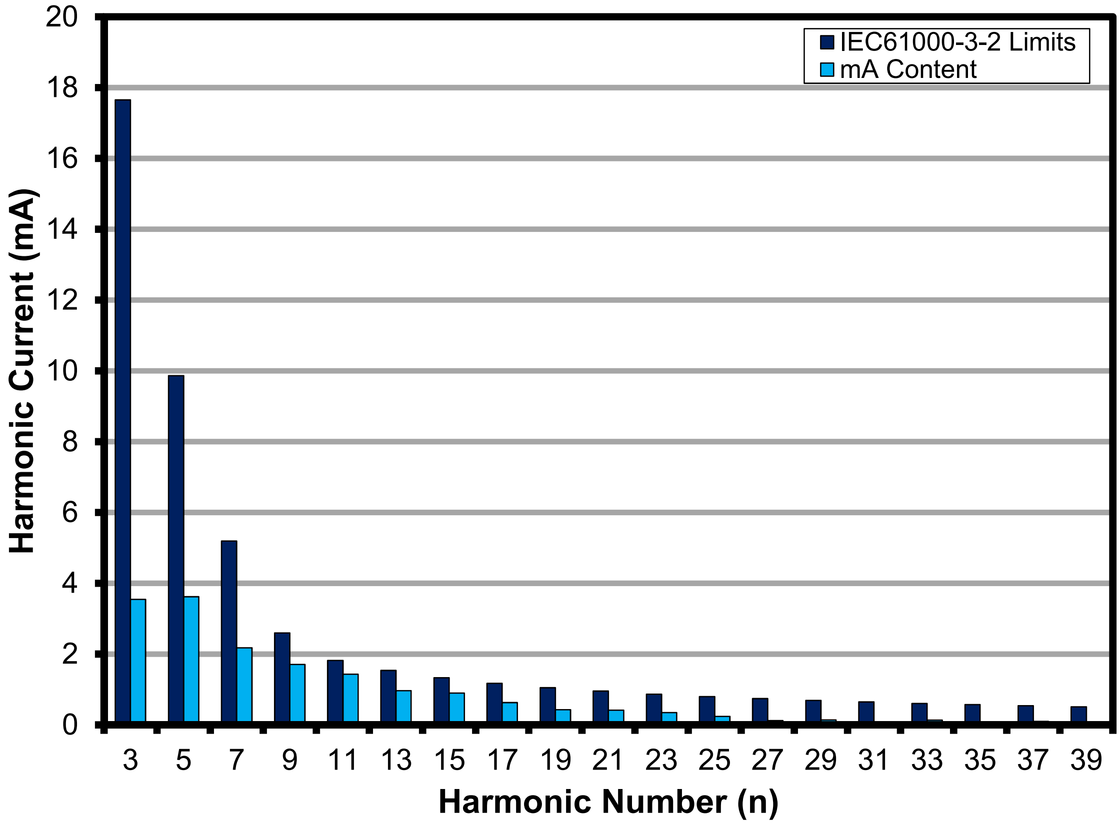

Figure 14 – 100 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

9.5.3 103 V LED Load

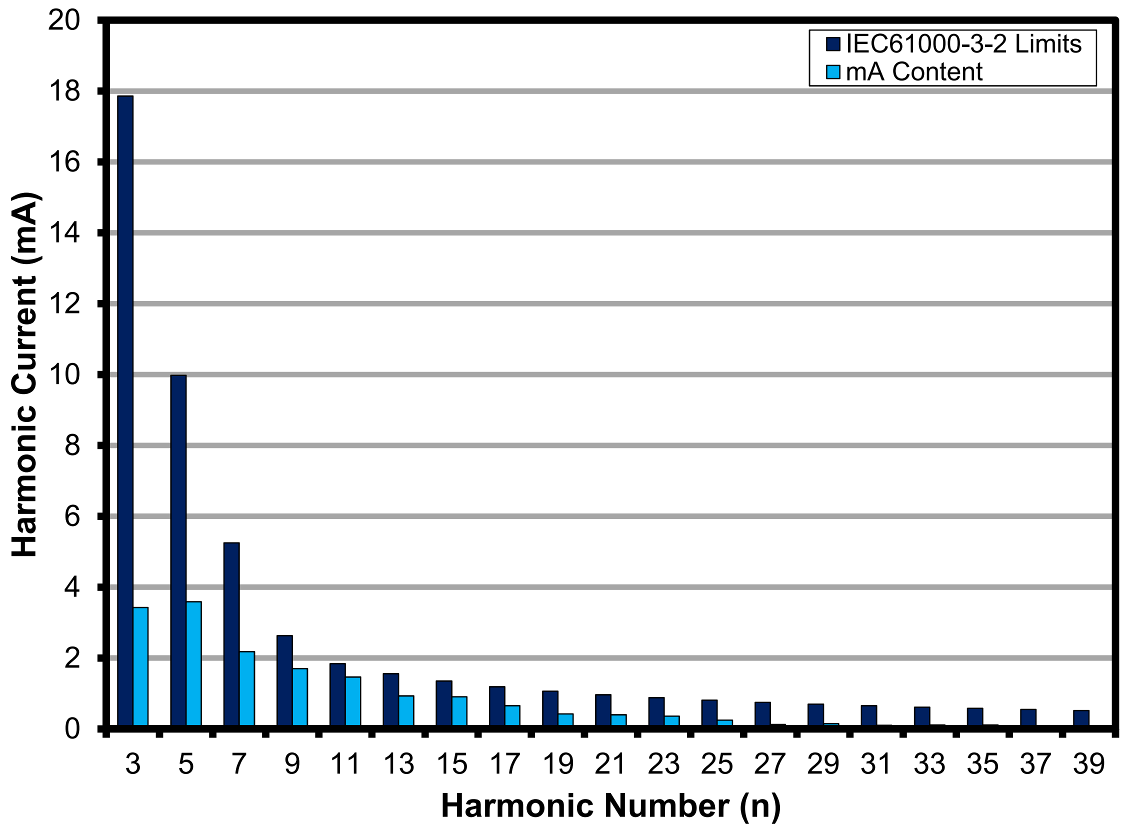

Figure 15 – 103 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

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9.6 Test Data

All measurements were taken with the board at open frame, 25 ºC ambient, and 50 Hz line frequency

9.6.1 Test Data, 97 V LED Load

Input Measurement					Load Measurement			Calculation		
V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
190.08	26.21	4.825	0.969	22.22	97.62	39.05	3.87	3.81	80.17	0.96
200.06	25.87	5.007	0.968	22.81	97.65	40.50	4.02	3.95	80.23	0.99
220.08	23.95	5.036	0.956	27.03	97.50	40.21	3.98	3.92	79.07	1.05
230.13	23.07	5.034	0.948	29.37	97.39	39.67	3.92	3.86	77.91	1.11
240.10	22.69	5.150	0.945	30.3	97.40	40.35	3.99	3.93	77.50	1.16
265.13	21.57	5.330	0.932	34.12	97.33	40.13	3.97	3.91	74.43	1.36

9.6.2 Test Data, 100 V LED Load

Input Measurement					Load Measurement			Calculation		
V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
190.13	26.69	4.932	0.972	20.5	99.93	39.18	3.97	3.91	80.51	0.96
200.11	25.97	5.038	0.970	21.76	99.96	39.95	4.05	3.99	80.47	0.98
220.13	24.20	5.106	0.958	25.68	99.92	40.08	4.06	4.00	79.59	1.04
230.19	23.65	5.193	0.954	27.12	99.91	40.41	4.10	4.04	78.95	1.09
240.15	22.92	5.218	0.948	28.98	99.87	40.29	4.08	4.02	78.25	1.14
265.18	21.83	5.419	0.936	32.54	99.88	40.65	4.12	4.06	76.07	1.30

9.6.3 Test Data, 103 V LED Load

Input Measurement					Load Measurement			Calculation		
V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
190.15	26.98	4.992	0.973	19.86	102.58	38.68	4.02	3.97	80.58	0.97
200.13	26.80	5.208	0.971	20.65	102.73	40.36	4.21	4.15	80.75	1.00
220.15	24.86	5.262	0.961	24.23	102.67	40.40	4.21	4.15	79.97	1.05
230.21	23.87	5.253	0.956	26.45	102.58	39.97	4.16	4.10	79.20	1.09
240.17	23.38	5.338	0.951	27.86	102.61	40.35	4.20	4.14	78.69	1.14
265.20	21.81	5.420	0.937	32.26	102.51	39.64	4.12	4.06	76.05	1.30

10 Non-Dimming Configuration Performance Data

The following data was taken with the board configured for non-dimming application. To convert the board for non-dimming application, R6, R7, D4 and R11 were replaced by 0 Ω 1206 jumper resistor and C8, C9, D5, D6, R8, R9, R10, R12, R13, R14, R15, R16, Q1, and Q2 were removed from the board.

All measurements performed at room temperature using an LED load. The following data were measured using 3 sets of loads to represent the load range of 97 V to 103 V output voltage). Refer to the table on Section 10.6 for the complete set of test data values.

10.1 Efficiency

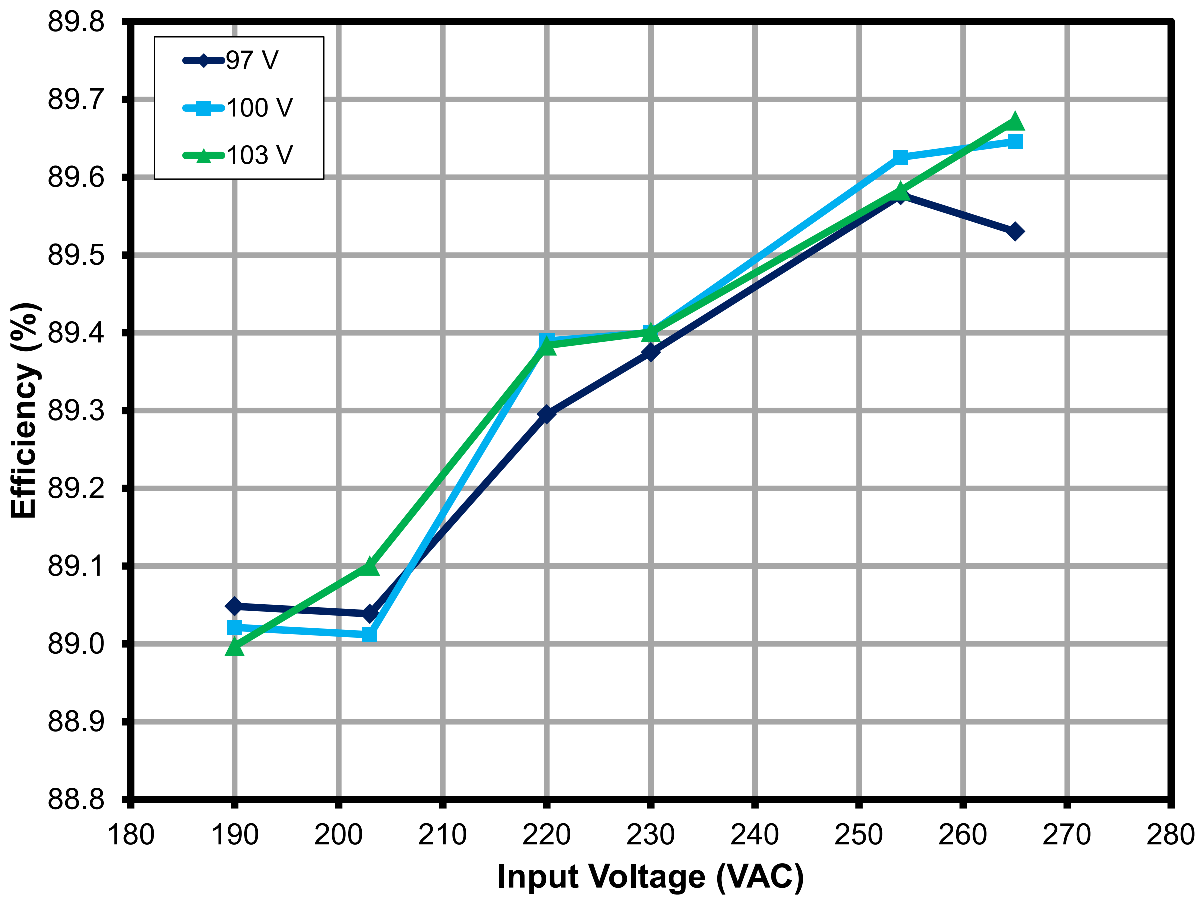

Figure 16 – Non-Dimming Configuration Efficiency vs. Line and Load.

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10.2 Line and Load Regulation

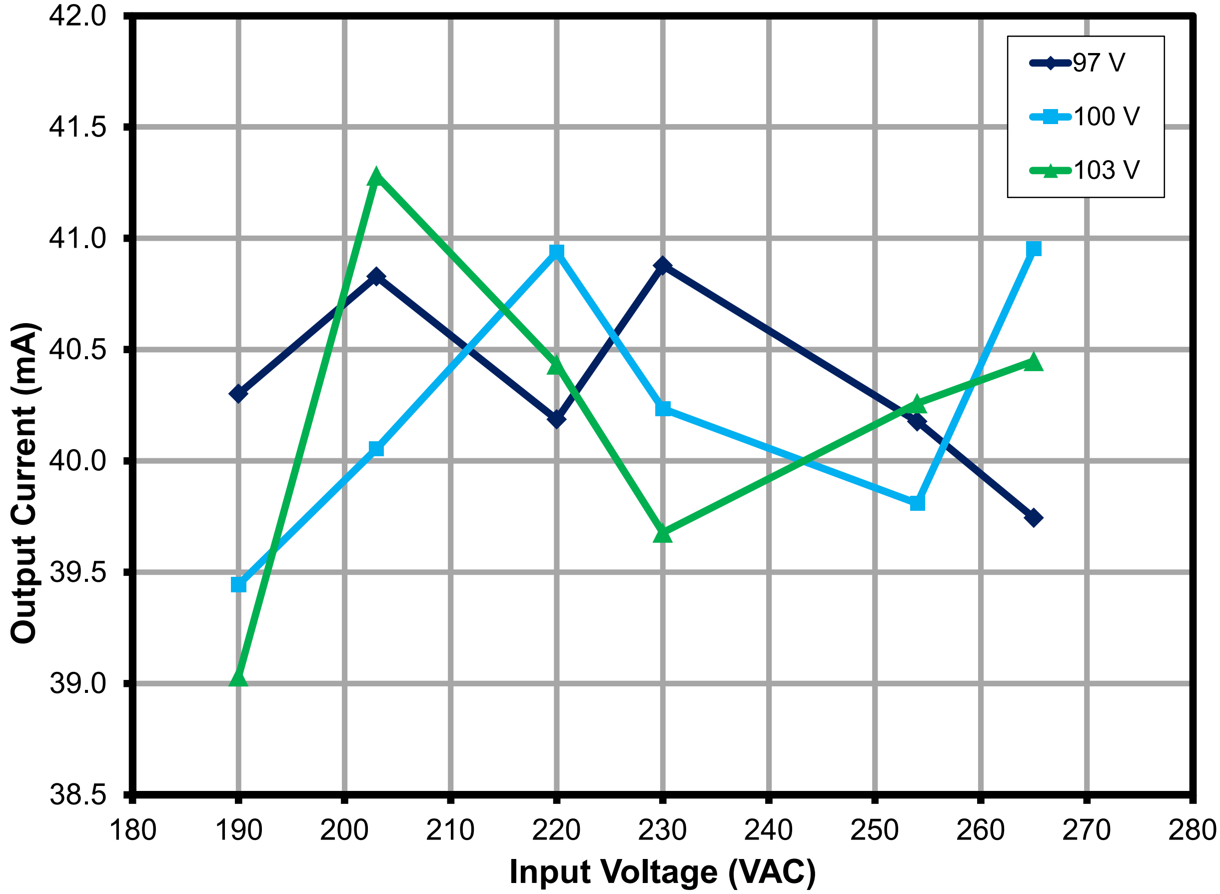

Figure 17 – Non-Dimming Configuration Regulation vs. Line and Load.

10.3 Power Factor

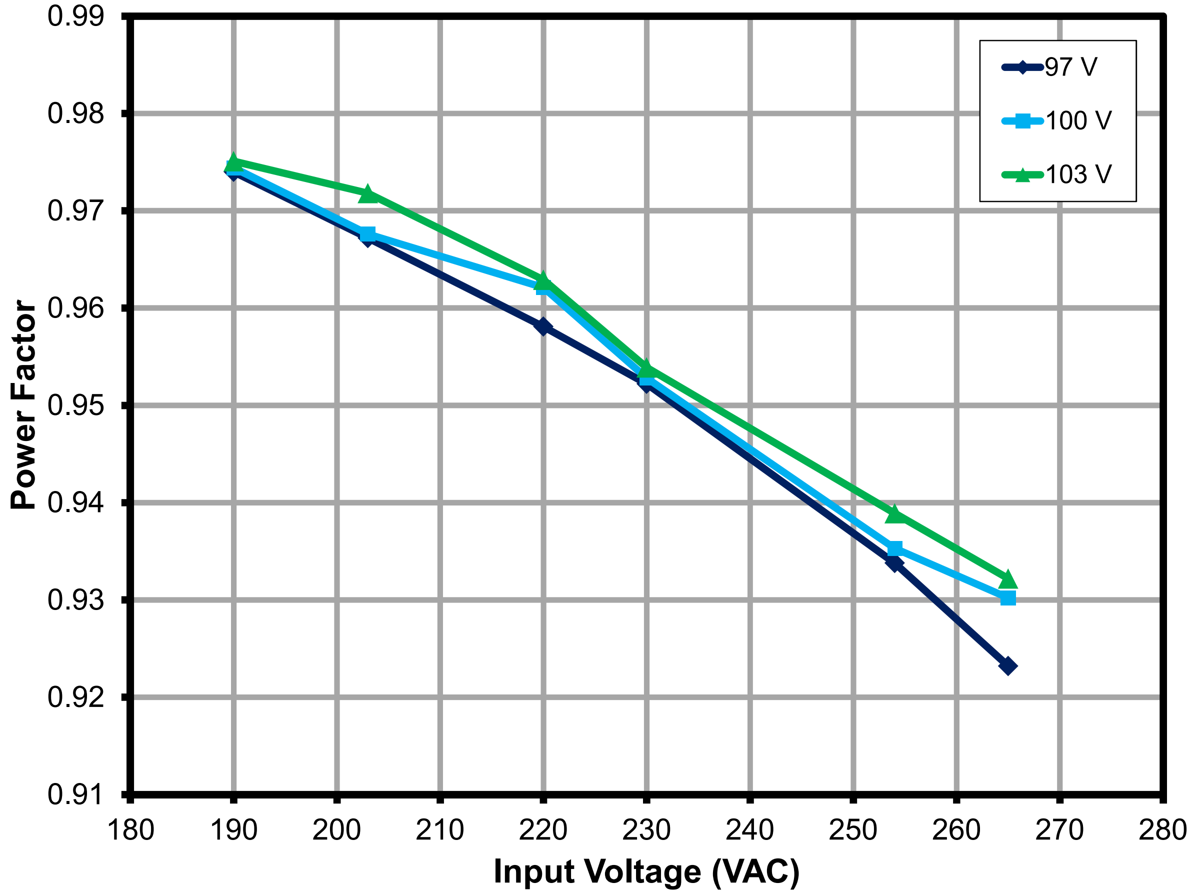

Figure 18 – Non-Dimming Configuration Power Factor vs. Line and Load.

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10.4 A-THD

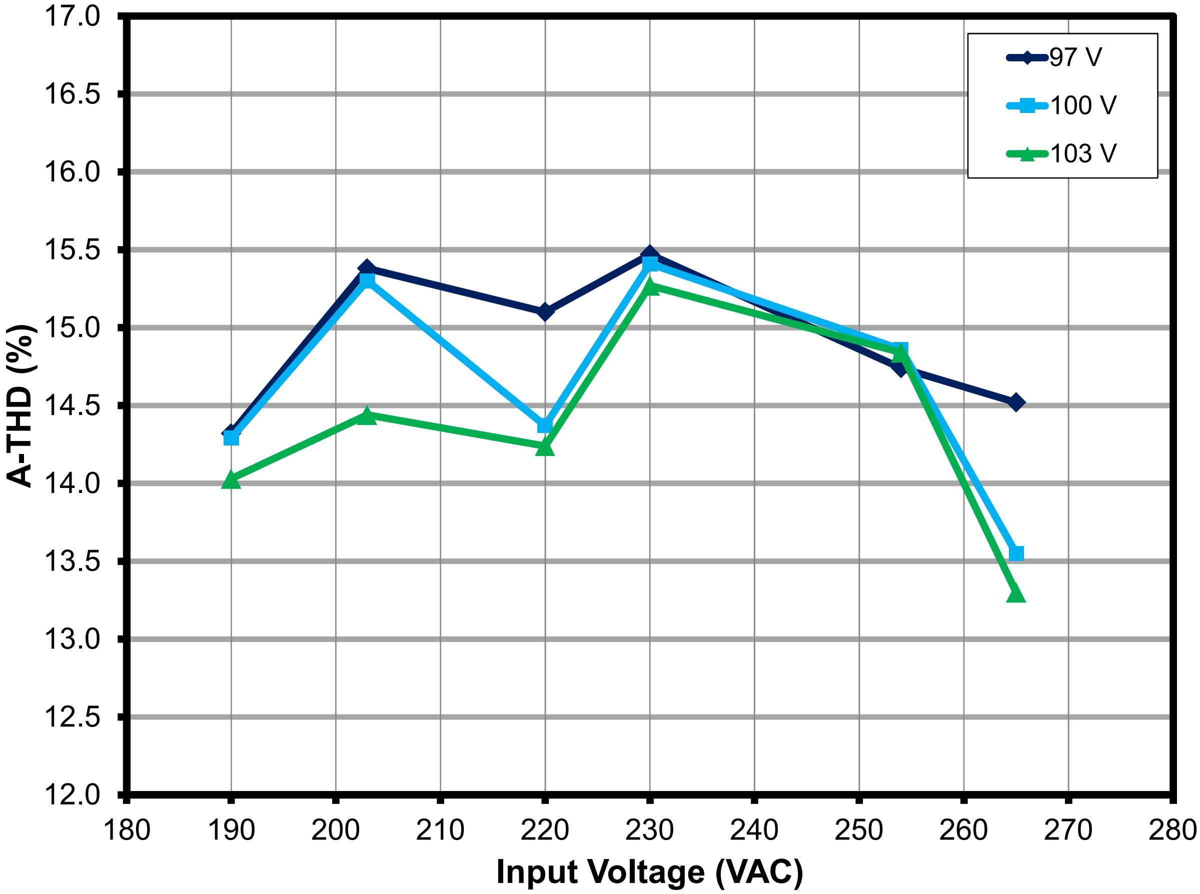

Figure 19 – Non-Dimming Configuration A-THD vs. Line and Load.

10.5 Harmonics

10.5.1 97 V LED Load

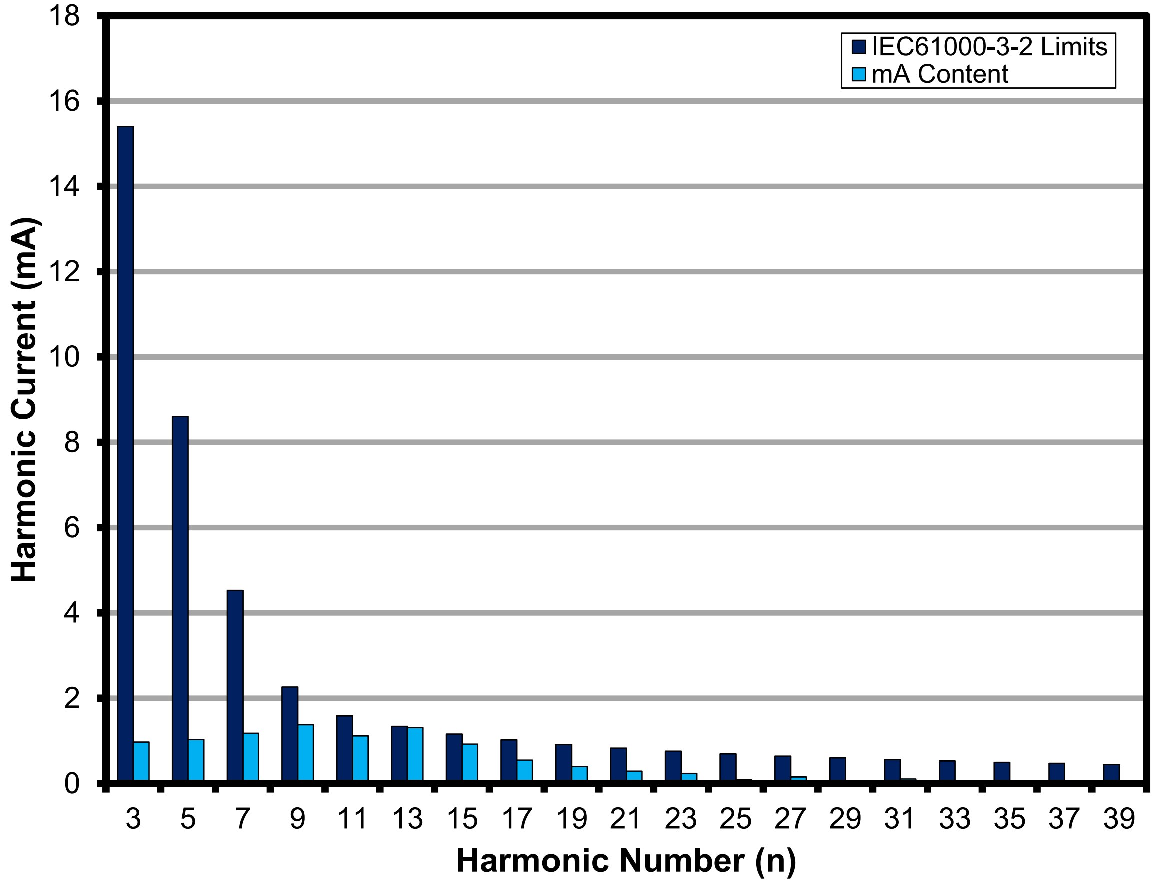

Figure 20 – 97 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

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10.5.2 100 V LED Load

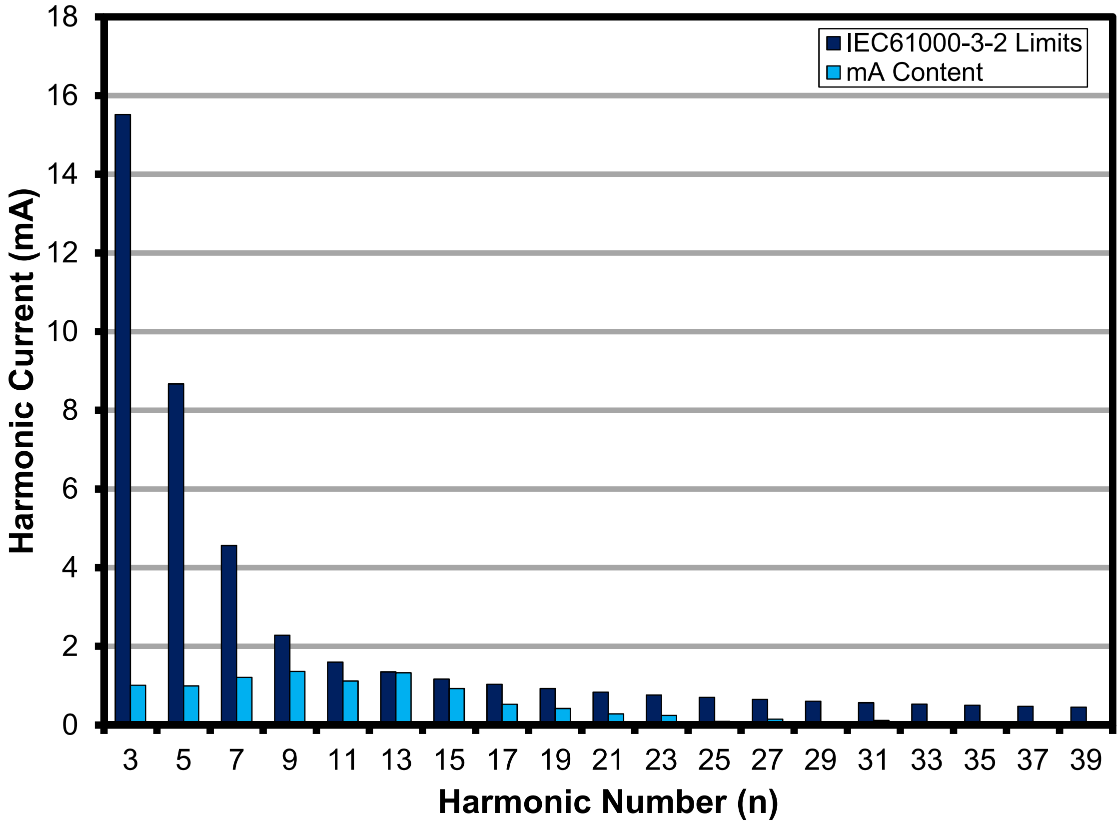

Figure 21 – 100 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

10.5.3 103 V LED Load

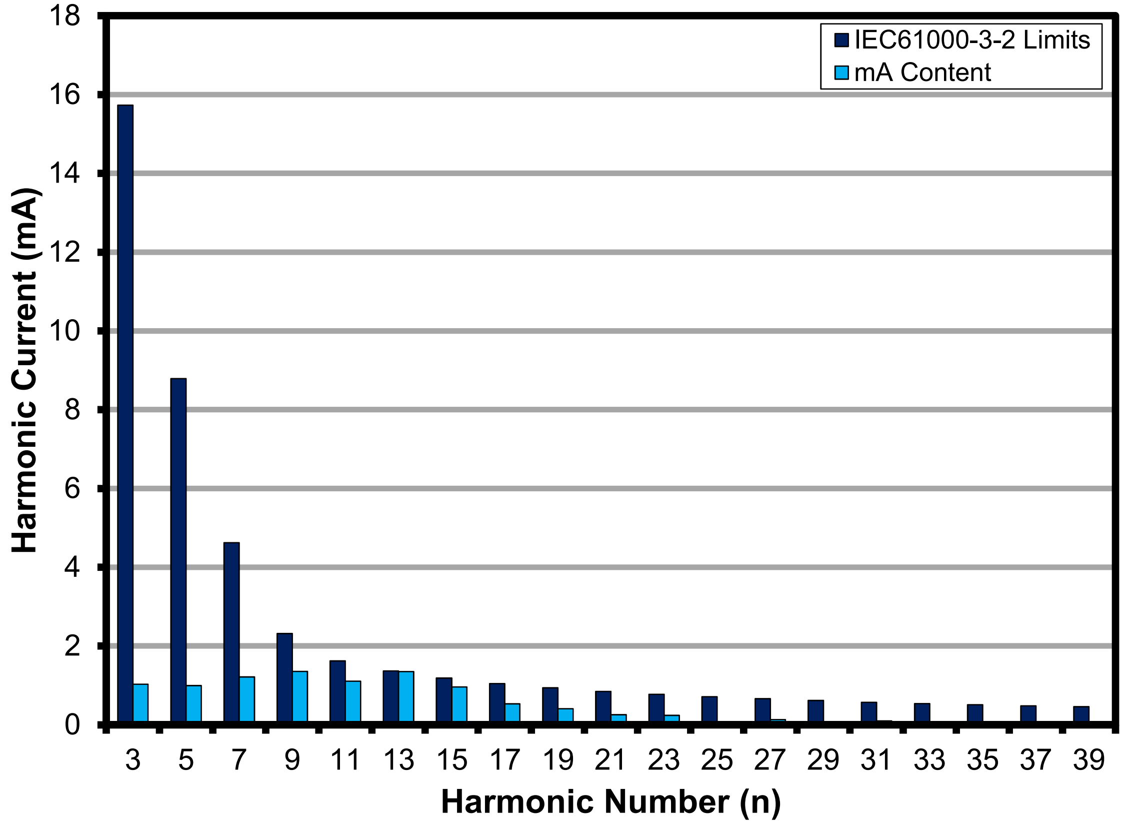

Figure 22 – 103 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

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10.6 Non-Dimming Configuration Test Data

All measurements were taken with the board at open frame, 25 ºC ambient, and 50 Hz line frequency

10.6.1 Test Data, 97 V LED Load

Input Measurement					Load Measurement			Calculation		
V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
190.14	24.24	4.490	0.974	14.32	97.7800	40.301	3.998	3.94	89.05	0.49
203.13	23.15	4.548	0.967	15.38	97.7600	40.828	4.049	3.99	89.04	0.50
220.14	21.13	4.457	0.958	15.1	97.6100	40.186	3.980	3.92	89.30	0.48
230.20	20.67	4.531	0.952	15.47	97.6600	40.877	4.049	3.99	89.37	0.48
254.18	18.69	4.436	0.934	14.74	97.5100	40.177	3.974	3.92	89.58	0.46
265.19	17.91	4.386	0.923	14.52	97.4400	39.744	3.927	3.87	89.53	0.46

10.6.2 Test Data, 100 V LED Load

Input Measurement					Load Measurement			Calculation		
V_{IN} (V_{RMS})	I_{IN} (mArms)	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
190.14	24.29	4.500	0.974	14.29	100.1400	39.444	4.006	3.95	89.02	0.49
203.13	23.24	4.569	0.968	15.3	100.1400	40.054	4.067	4.01	89.01	0.50
220.14	21.97	4.653	0.962	14.37	100.1500	40.937	4.159	4.10	89.39	0.49
230.20	20.81	4.563	0.953	15.41	100.0200	40.234	4.080	4.02	89.40	0.48
254.17	18.93	4.501	0.935	14.86	99.9500	39.809	4.034	3.98	89.63	0.47
265.19	18.79	4.636	0.930	13.55	100.0400	40.953	4.156	4.10	89.65	0.48

10.6.3 Test Data, 103 V LED Load

Input Measurement					Load Measurement			Calculation		
V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
190.15	24.67	4.574	0.975	14.03	102.9000	39.032	4.071	4.02	89.00	0.50
203.13	24.54	4.844	0.972	14.44	103.0800	41.281	4.316	4.26	89.10	0.53
220.15	22.27	4.721	0.963	14.24	102.9300	40.433	4.220	4.16	89.38	0.50
230.20	21.07	4.626	0.954	15.27	102.8700	39.678	4.136	4.08	89.40	0.49
254.18	19.64	4.688	0.939	14.84	102.9300	40.259	4.199	4.14	89.58	0.49
265.19	19.04	4.707	0.932	13.3	102.9300	40.449	4.221	4.16	89.67	0.49

11 Dimming Performance Data

TRIAC Dimming Results were taken with input voltage of 230 VAC, 50 Hz line frequency, room temperature, and nominal 100 V LED load.

11.1 Dimming Curve with Leading Edge Type Dimmer

Taken using a programmable AC source providing the leading edge chopped AC input.

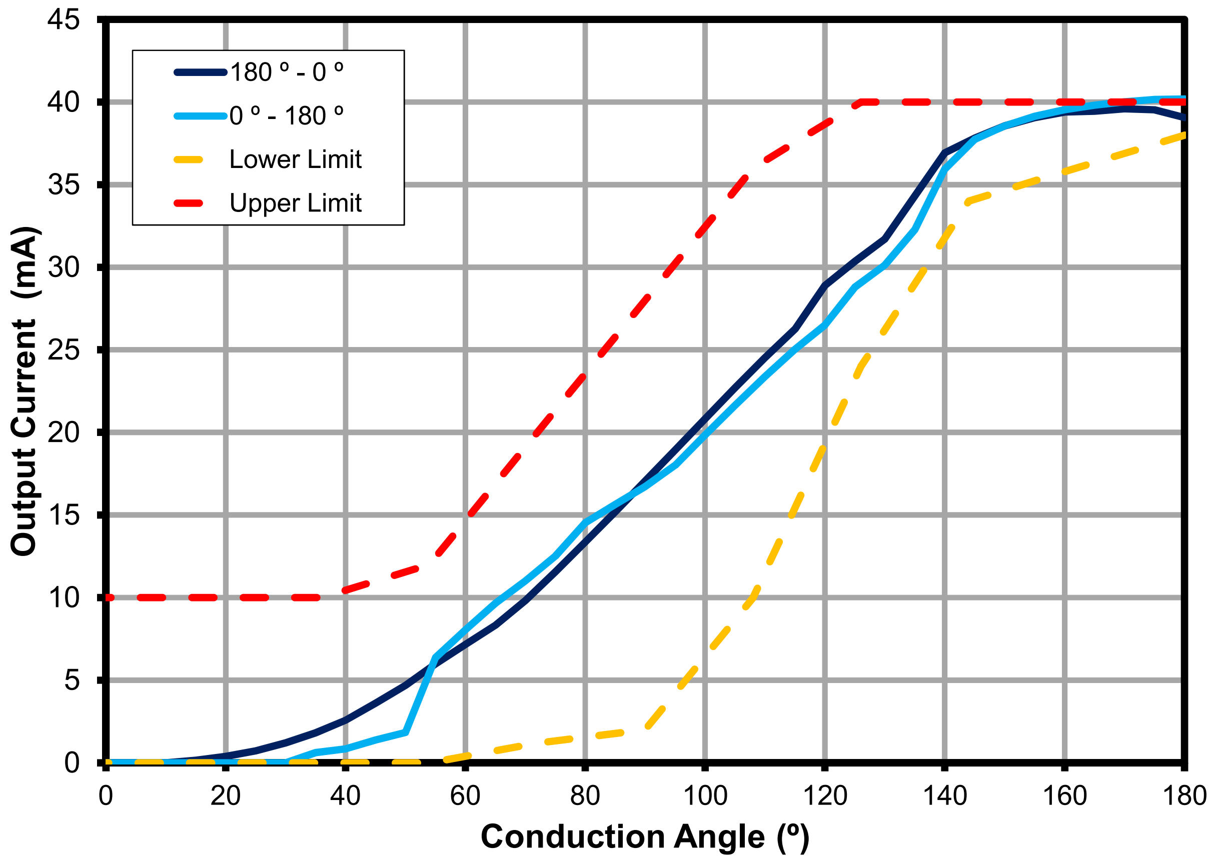

Figure 23 – Leading Edge Dimming Characteristics.

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11.2 Dimming Curve with Trailing Edge Type Dimmer

Measured using a programmable AC source providing the trailing edge chopped AC input.

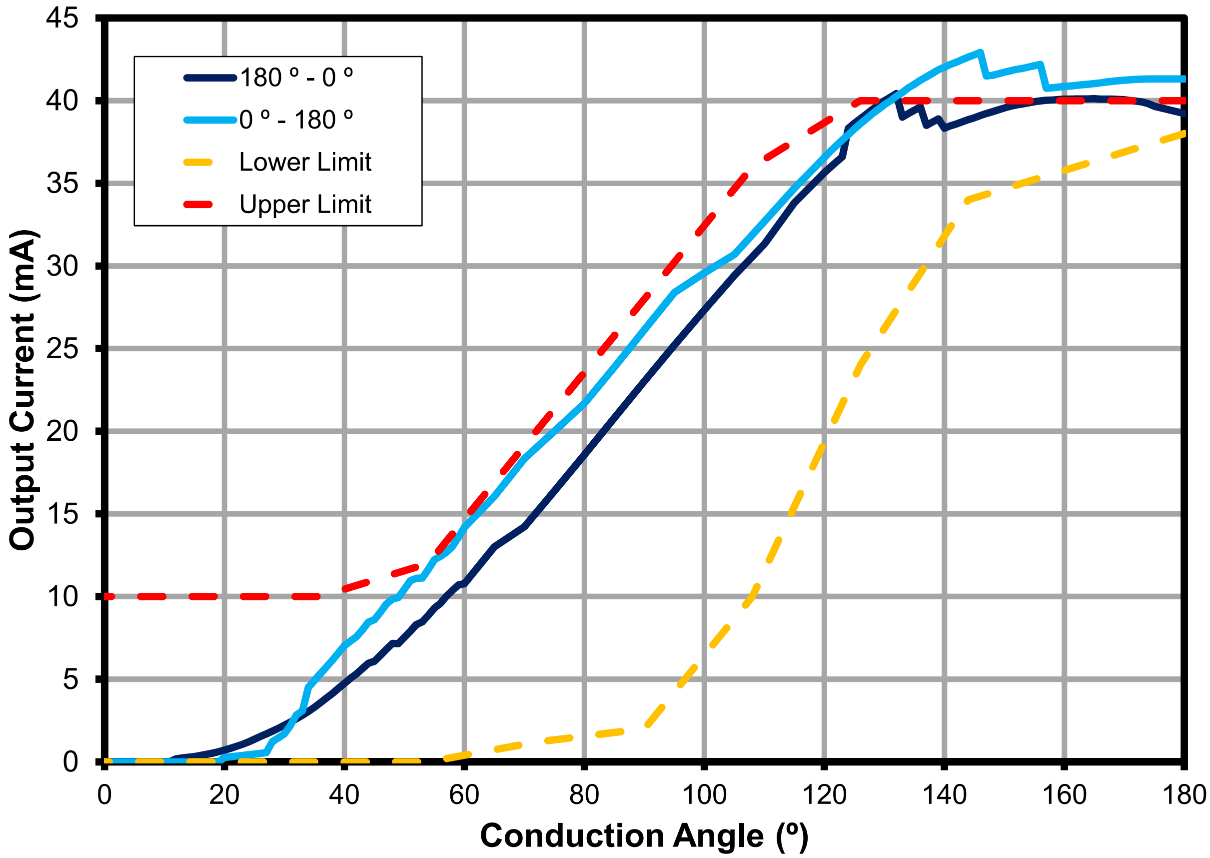

Figure 24 – Trailing Edge Dimming Characteristics.

11.3 Dimmer Compatibility List

The unit was tested with the following high-line dimmers at 230 VAC, 50 Hz input and 100 V LED load.

Dimmer	Minimum Conduction Angle (º)	Minimum I_{OUT} (mA)	Maximum Conduction Angle (º)	Maximum I_{OUT} (mA)	Dim Ratio	Type
REV 300	13.50	0.41	149.94	38.85	94.76	LE
BUSCH 2250	42.30	4.97	150.48	40.18	8.08	LE
MERTEN 572499	37.62	4.87	159.66	39.77	8.17	LE
BERKER 2875	47.88	5.50	149.94	38.15	6.94	LE
BUSCH 6513	41.40	14.80	144.90	41.63	2.81	TE
PEHA 433HAB oA	45.18	8.17	123.84	38.40	4.70	TE
PEHA 433HAB	55.80	11.70	136.08	41.50	3.55	TE
BUSCH 6513 U-102	42.84	14.90	144.90	40.24	2.70	TE
ATD315	24.30	2.19	135.90	41.60	19.00	TE
32E450TM	43.20	8.00	144.00	41.80	5.23	TE
32E450UDM	48.60	8.43	145.80	42.00	4.98	TE
SEN BO LANG 300 W	60.48	8.15	167.58	40.20	4.93	LE
EBA HUANG	15.66	0.45	167.58	38.50	85.56	LE
MYONGBO	59.58	9.35	169.56	39.00	4.17	LE
CLIPMEI	43.74	5.78	167.04	41.15	7.12	LE
MANK 200 W	69.30	11.79	168.12	38.80	3.29	LE

Figure 25 – List of Dimmers with Good Compatibility with the LED Driver.

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12 Thermal Performance

Images captured after running for more than 30 minutes at room temperature (25 °C), open frame for the conditions specified.

12.1 No Dimmer Connected; V_{IN} = 190 VAC, 50 Hz, 100 V LED Load

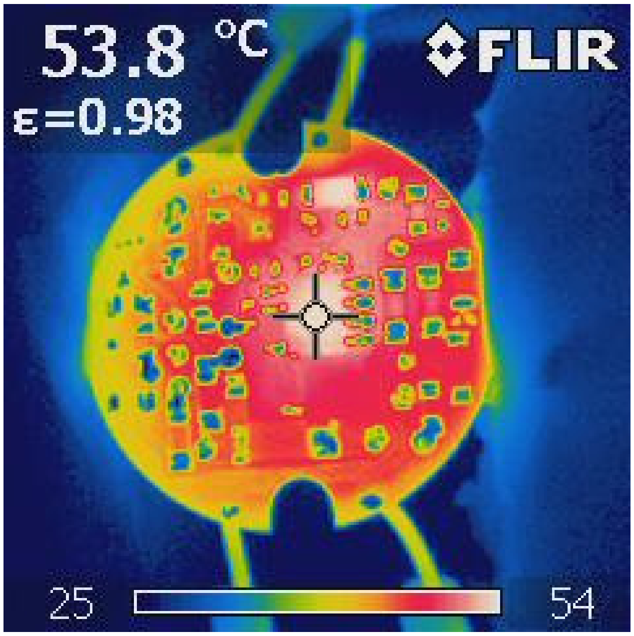

Figure 26 – Bottom Side.
U1-LNK456DG: 53.8 ºC.

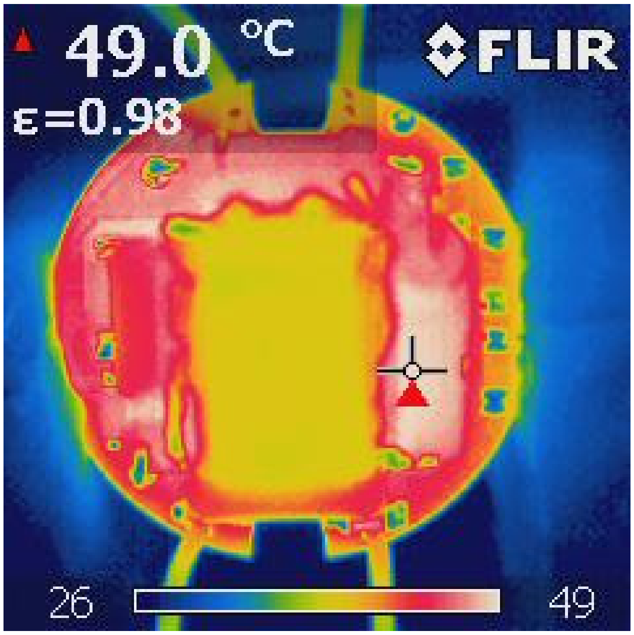

Figure 27 – Top Side.
Q1-STT13005: 49 ºC.

12.2 No Dimmer Connected: V_{IN} = 265 VAC, 50 Hz, 100 V LED Load

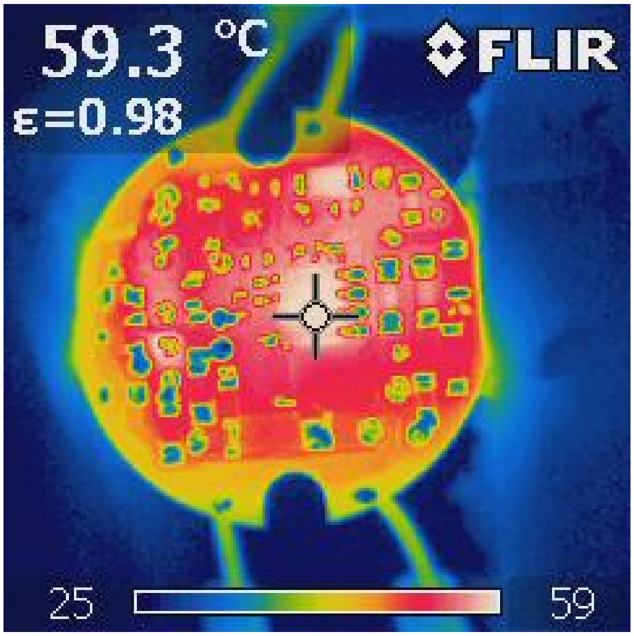

Figure 28 – Bottom Side.
U1-LNK456DG: 59.3 ºC.

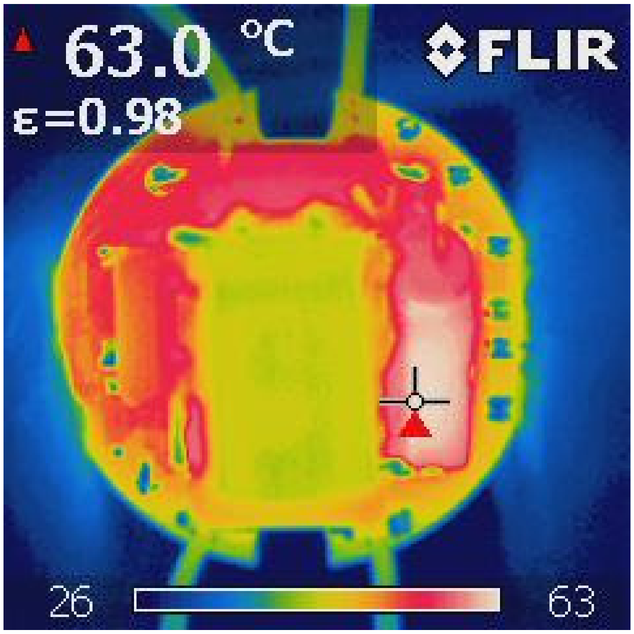

Figure 29 – Top Side.
Q1-STT13005: 63 ºC.

12.3 Dimming V_{IN} = 230 VAC 50 Hz, 90º Conduction Angle, 100 V LED Load

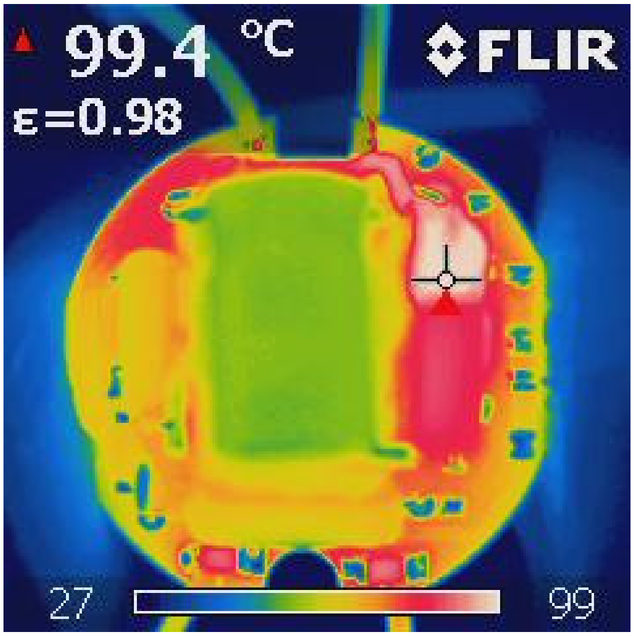

Figure 30 – Top Side.
R16-Bleeder Resistor: 99.4 ºC

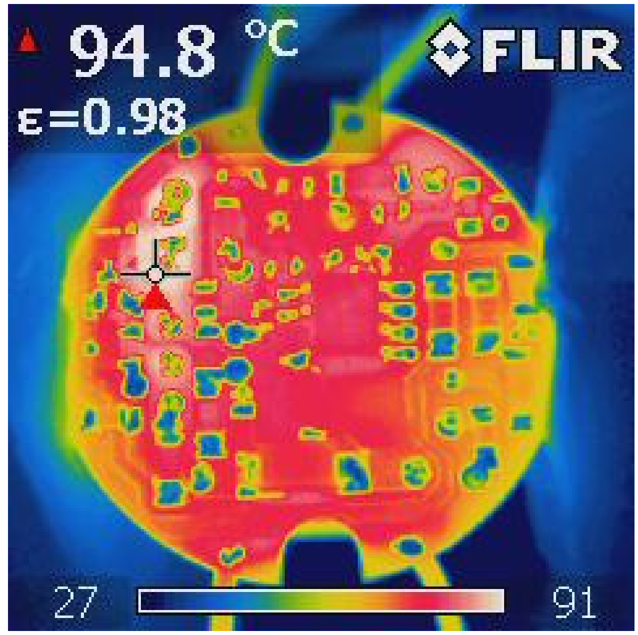

Figure 31 – Bottom Side.
PCB: 94.8 ºC.

13 Non-Dimming (No Dimmer Connected) Waveforms

13.1 Input Voltage and Input Current Waveforms

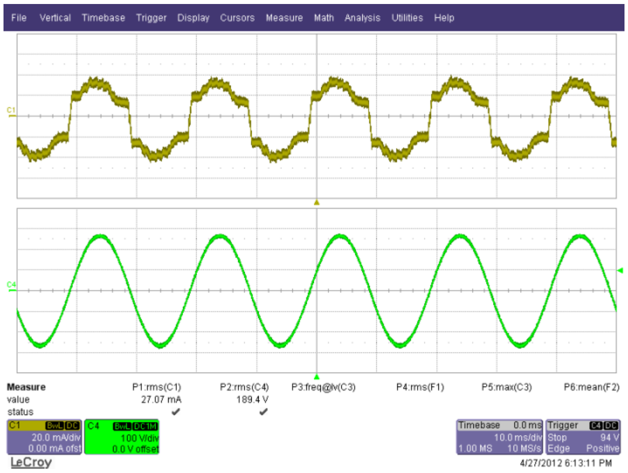

Figure 32 – 190 VAC, Full Load.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 10 ms / div.

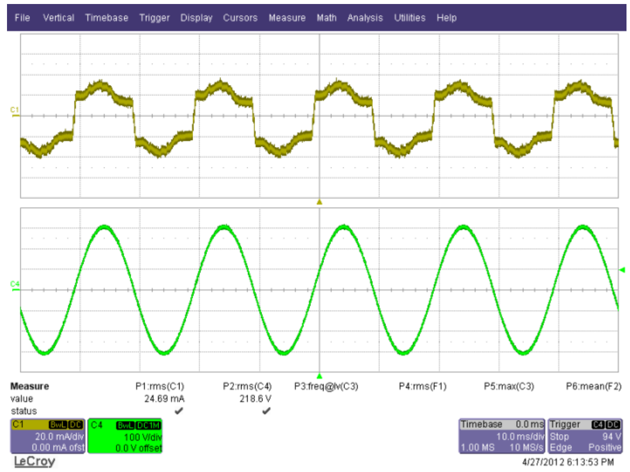

Figure 33 – 220 VAC, Full Load.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 10 ms / div.

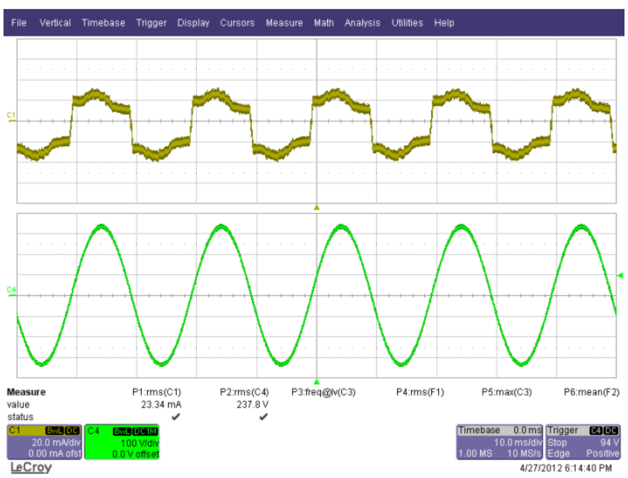

Figure 34 – 240 VAC, Full Load.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 10 ms / div.

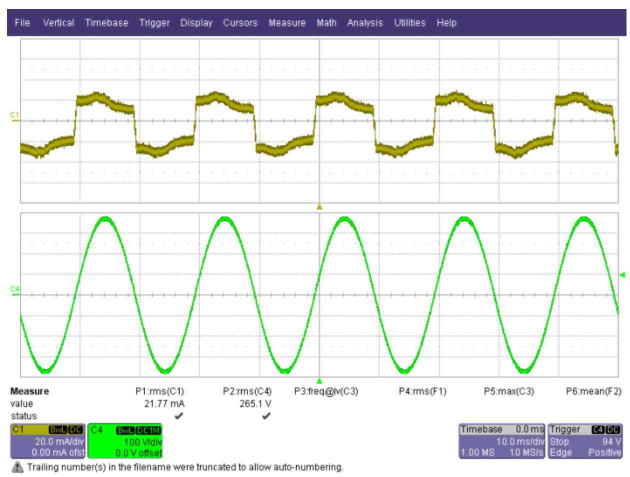

Figure 35 – 265 VAC, Full Load.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 10 ms / div.

13.2 Output Current and Output Voltage at Normal Operation

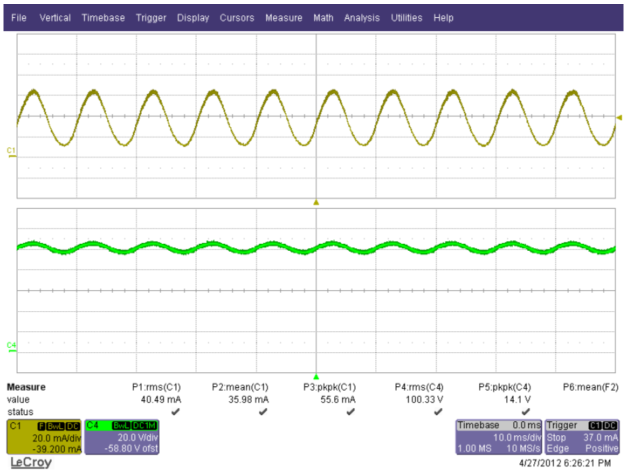

Figure 36 – 190 VAC, 50 Hz Full Load.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 20 V, 10 ms / div.

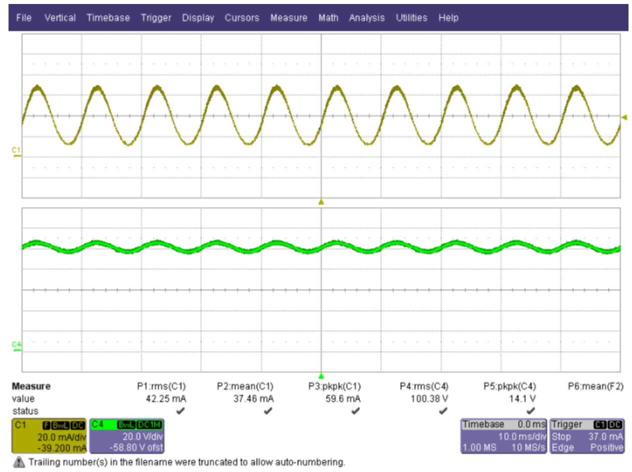

Figure 37 – 220 VAC, 50 Hz Full Load.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 20 V, 10 ms / div.

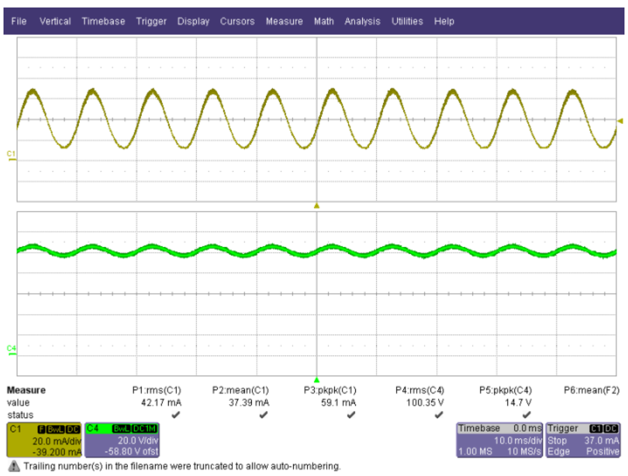

Figure 38 – 240 VAC, 50 Hz Full Load.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 20 V, 10 ms / div.

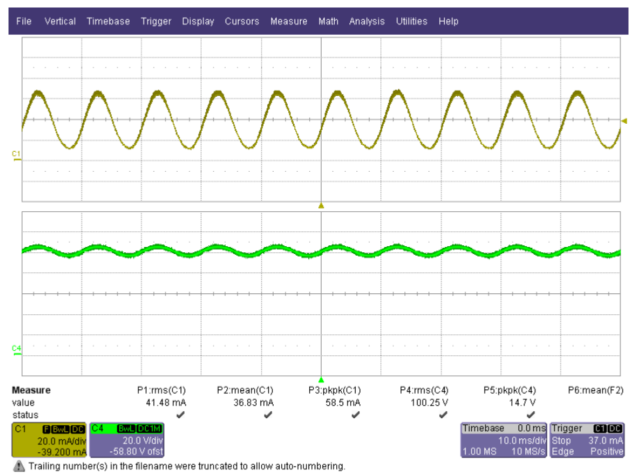

Figure 39 – 265 VAC, 50 Hz Full Load.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 20 V, 10 ms / div.

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13.3 Output Current/Voltage Rise and Fall

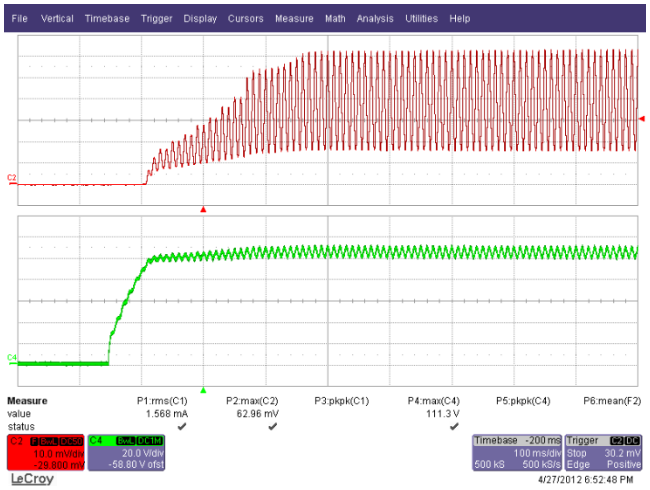

Figure 40 – 190 VAC Output Rise.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{OUT}, 20 V, 100 ms / div.

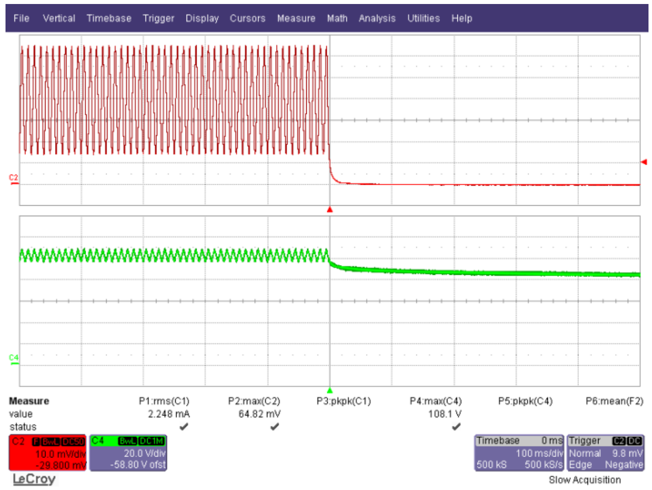

Figure 41 – 190 VAC Output Fall.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{OUT}, 20 V, 100 ms / div.

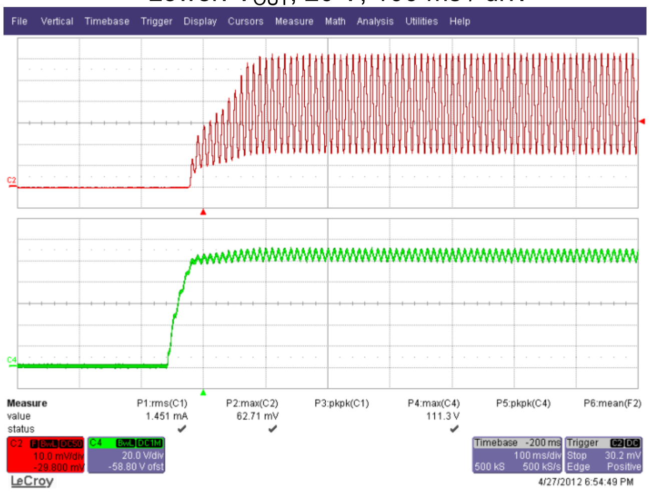

Figure 42 – 265 VAC Output Rise.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{OUT}, 20 V, 100 ms / div.

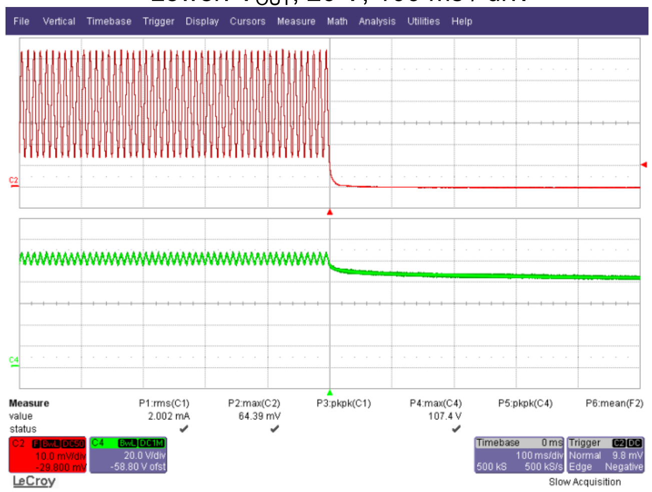

Figure 43 – 265 VAC Output Fall.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{OUT}, 20 V, 100 ms / div.

13.4 Input Voltage and Output Current Waveform at Start-up

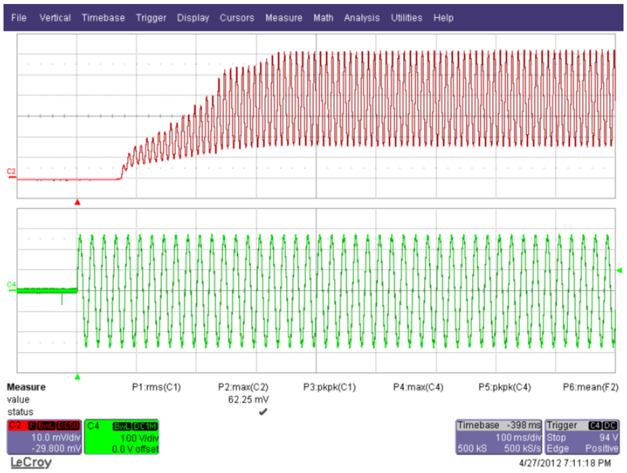

Figure 44 – 190 VAC, 50 Hz.
Upper: I_{OUT}, 10m A / div.
Lower: V_{IN}, 100 V, 100 ms / div.

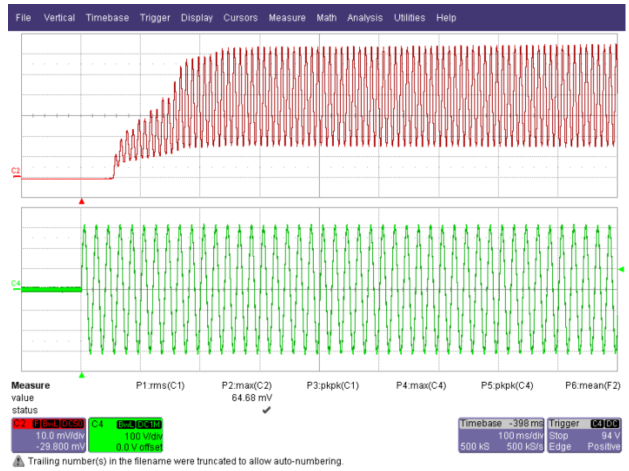

Figure 45 – 220 VAC, 50 Hz.
Upper: I_{OUT}, 10m A / div.
Lower: V_{IN}, 100 V, 100 ms / div.

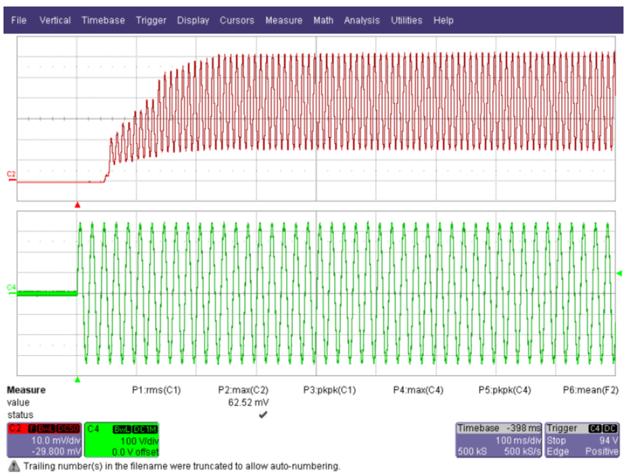

Figure 46 – 240 VAC, 50 Hz.
Upper: I_{OUT}, 10m A / div.
Lower: V_{IN}, 100 V, 100 ms / div.

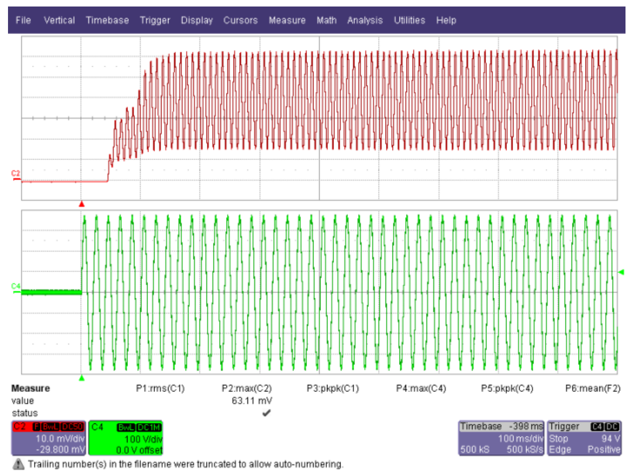

Figure 47 – 265 VAC, 50 Hz.
Upper: I_{OUT}, 10m A / div.
Lower: V_{IN}, 100 V, 100 ms / div.

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13.5 Drain Voltage and Current at Normal Operation

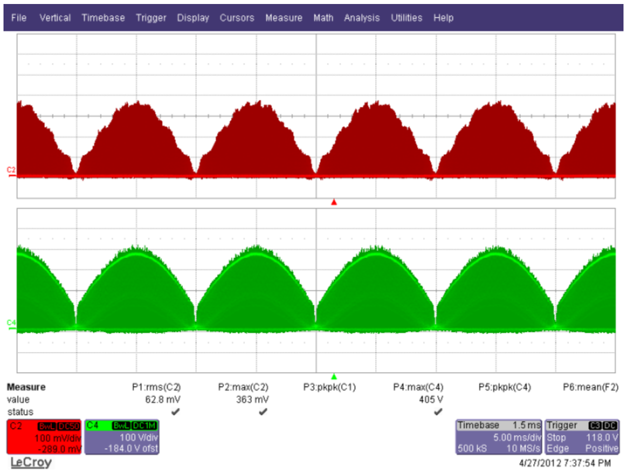

Figure 48 – 190 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V, 5 ms / div.

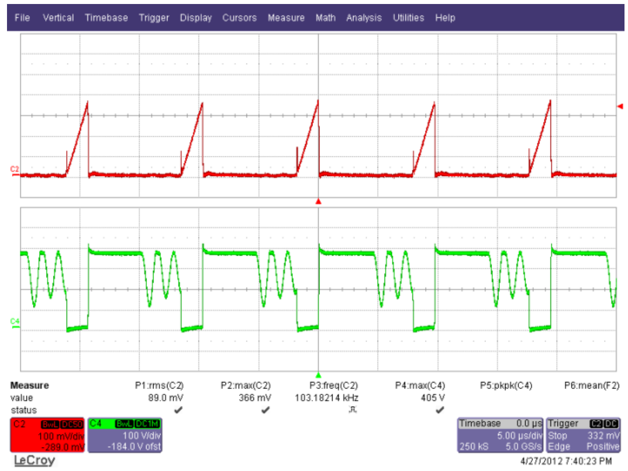

Figure 49 – 190 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V / div., 10 μs / div.

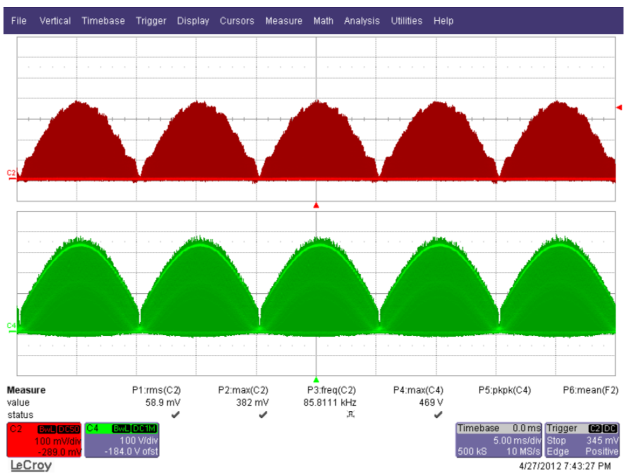

Figure 50 – 230 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V, 5 ms / div.

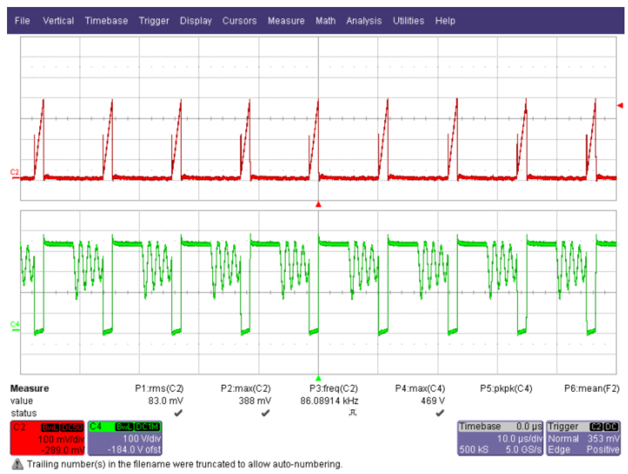

Figure 51 – 230 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V / div., 10 μs / div.

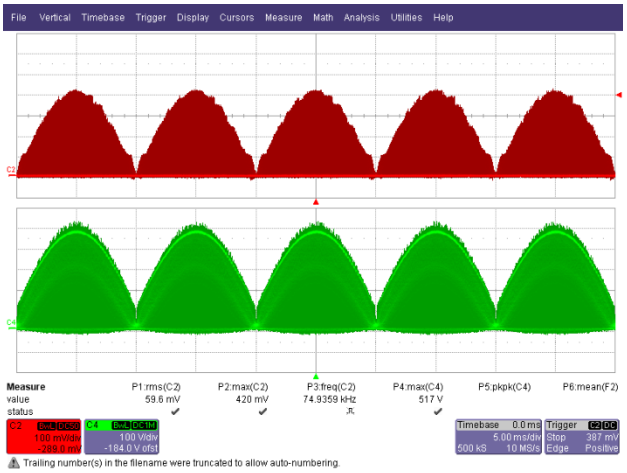

Figure 52 – 265 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V, 5 ms / div.

Figure 53 – 265 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V / div., 10 µs / div.

13.6 Start-up Drain Voltage and Current

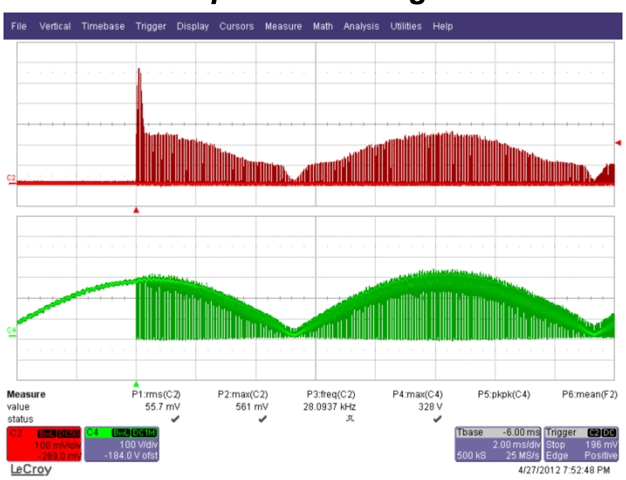

Figure 54 – 190 VAC, 50 Hz Start-up.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 100 V, 2 ms / div.

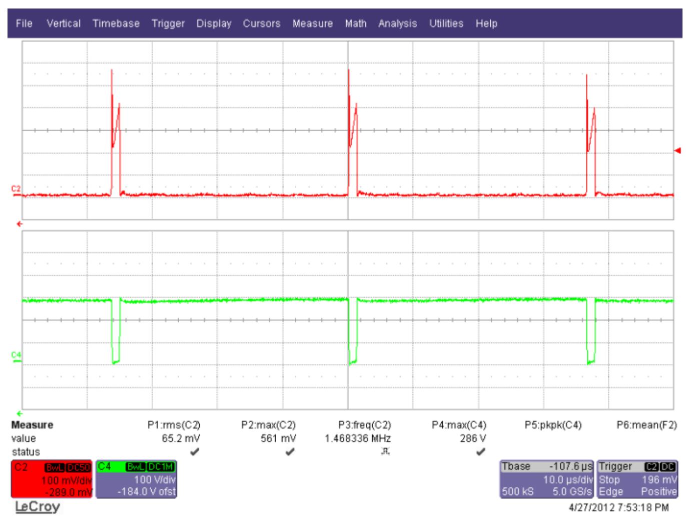

Figure 55 – 190 VAC, 50 Hz Start-up.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 100 V, 10 µs / div.

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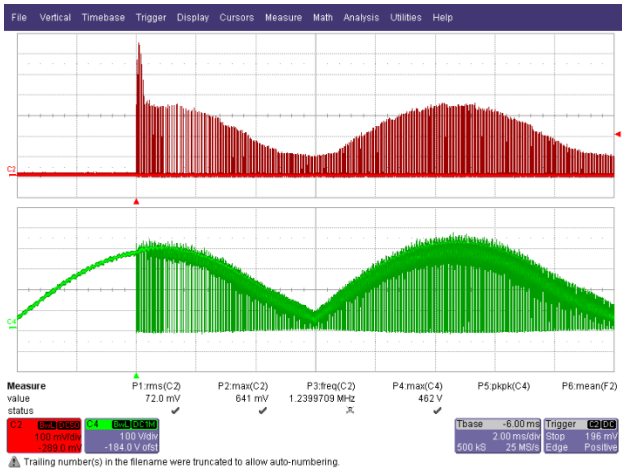

Figure 56 – 265 VAC, 50 Hz Start-up.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 100 V, 2 ms / div.

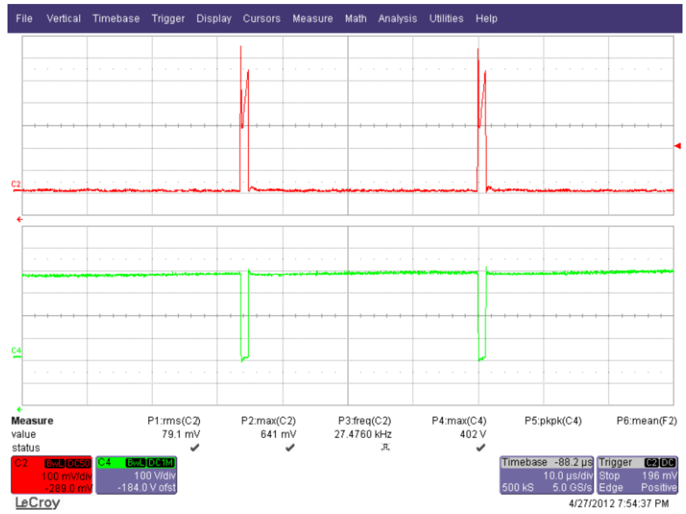

Figure 57 – 265 VAC, 50 Hz Start-up.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 100 V, 10 µs / div.

13.7 Drain Current and Drain Voltage During Output Short Condition

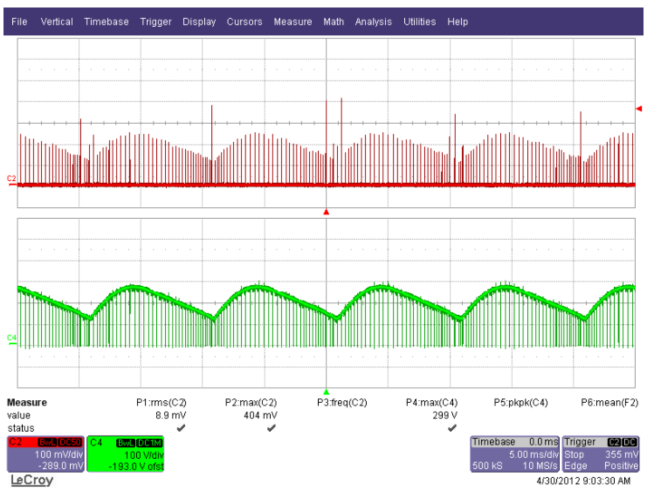

Figure 58 – 190 VAC, 50 Hz Output Short Condition.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 100 V, 5ms / div.

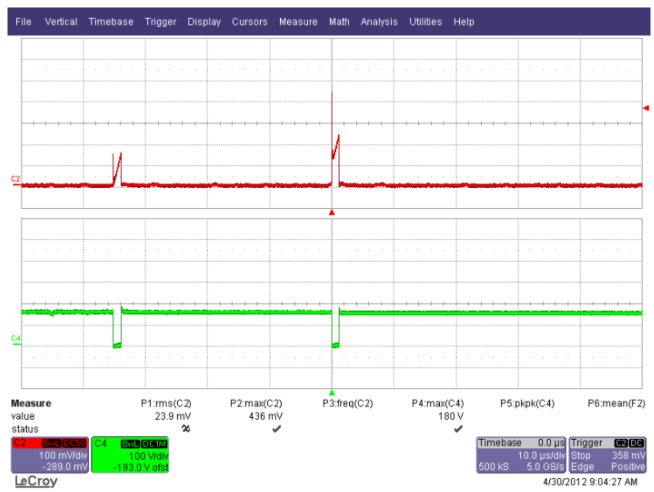

Figure 59 – 190 VAC, 50 Hz Output Short Condition.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 100 V, 10 µs / div.

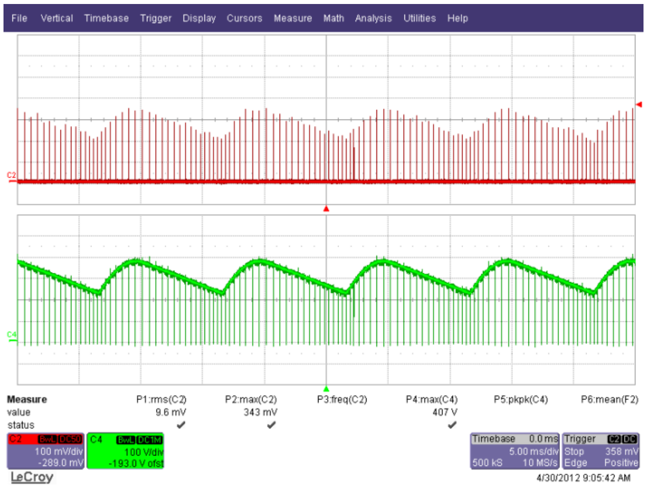

Figure 60 – 265 VAC, 50 Hz Output Short Condition.
Upper: I_{DRAIN}, 100 mA / div.
Lower: $V_{DRAIN,}$ 100 V, 5ms / div.

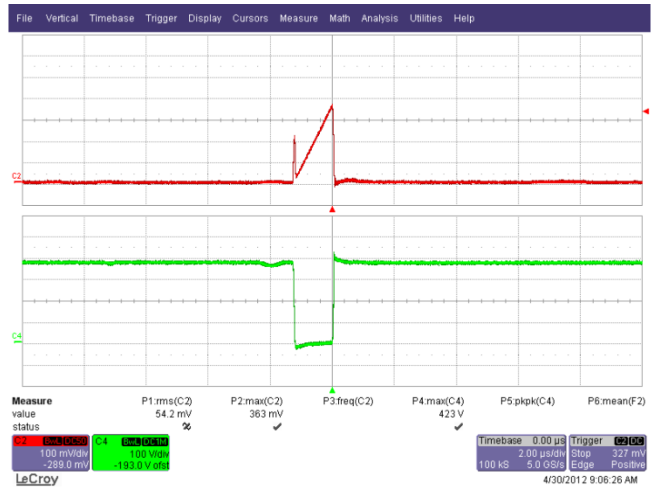

Figure 61 – 265 VAC, 50 Hz Output Short Condition.
Upper: I_{DRAIN}, 100 mA / div.
Lower: $V_{DRAIN,}$ 100 V, 2 µs / div.

13.8 Open Load Characteristic

Maximum Drain Voltage and Output voltage were within the rated specification of U1 and C7.

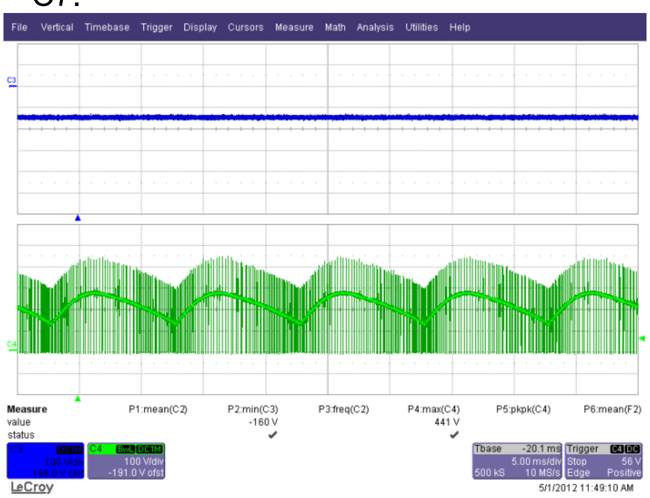

Figure 62 – 190 VAC, 50 Hz Open Load Characteristic.
Upper: V_{OUT}, 100 V / div.
Lower: V_{DRAIN}, 100 V / div., 5ms / div.

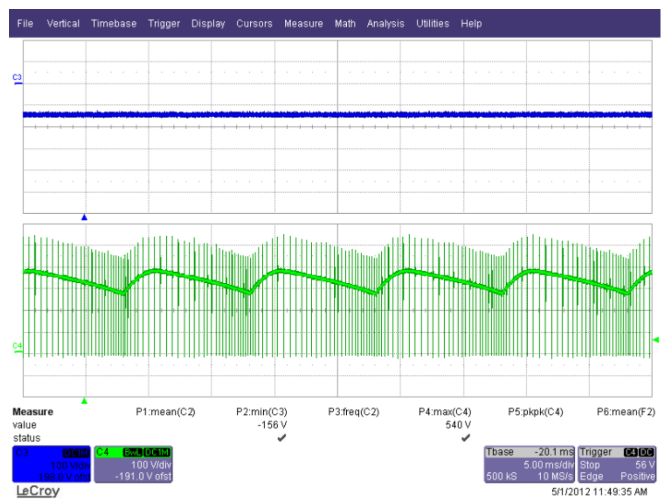

Figure 63 – 265 VAC, 50 Hz Open Load Characteristic.
Upper: V_{OUT}, 100 V / div.
Lower: V_{DRAIN}, 100 V / div., 5ms / div.

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13.9 Short Circuit: Output Diode PIV

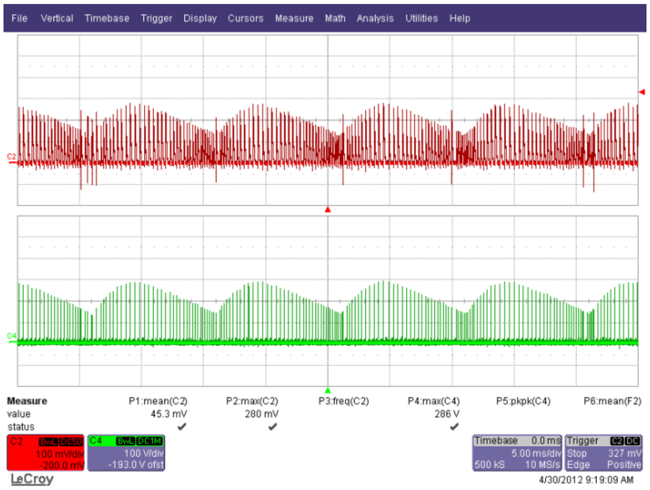

Figure 64 – 190 VAC, 50 Hz Output Short Characteristic.
Upper: I_{OUT}, 100 mA / div.
Lower: $V_{PIV\ D2}$, 100 V / div., 5 ms / div.

Figure 65 – 265 VAC, 50 Hz Output Short Characteristic.
Upper: I_{OUT}, 100 mA / div.
Lower: $V_{PIV\ D2}$, 100 V / div., 5 ms / div.

14 Dimming Waveforms

14.1 Input Voltage and Input Current Waveforms – Leading Edge Dimmer

Input: 230 VAC, 50 Hz
Output: 100 V LED Load
Dimmer: REV300

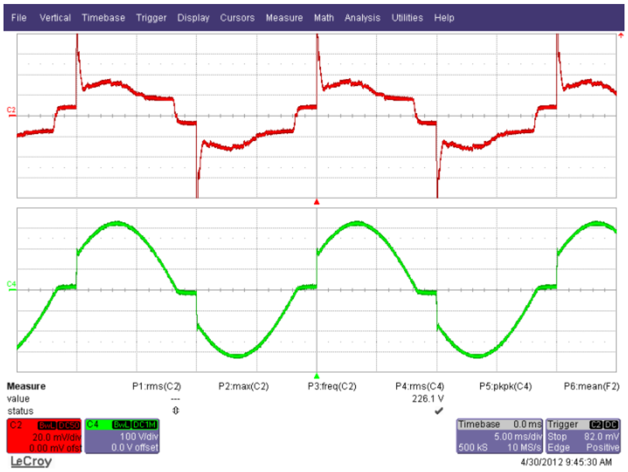

Figure 66 – 151º Conduction Angle.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

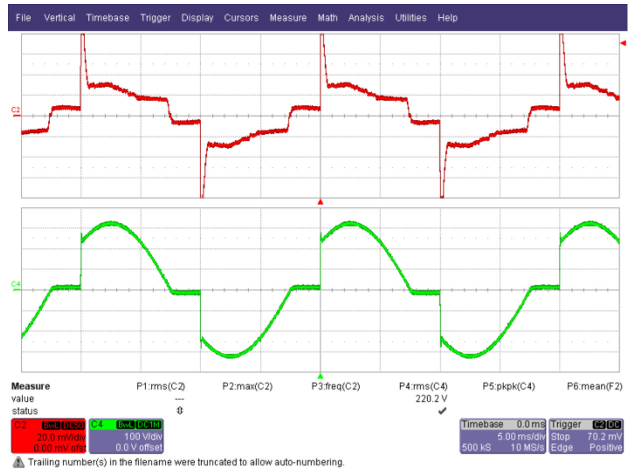

Figure 67 – 135º Conduction Angle.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

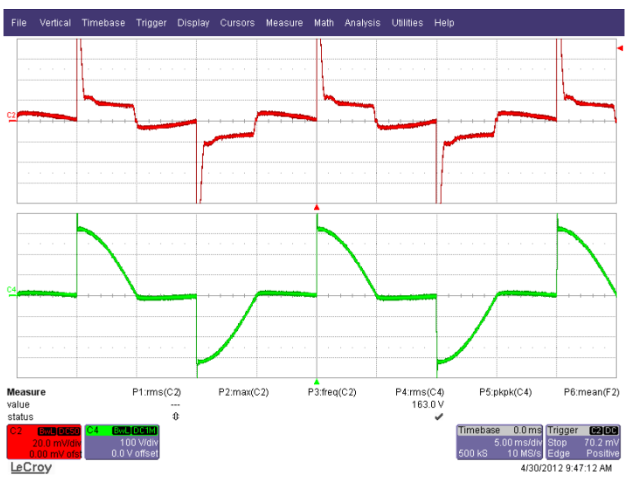

Figure 68 – 90º Conduction Angle.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

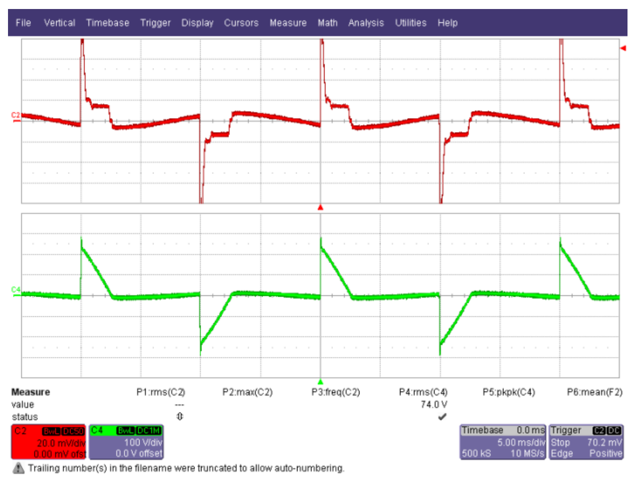

Figure 69 – 45º Conduction Angle.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

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14.2 Output Current Waveforms – Leading Edge Dimmer

Input: 230 VAC, 50 Hz
Output: 100 V LED Load
Dimmer: REV300

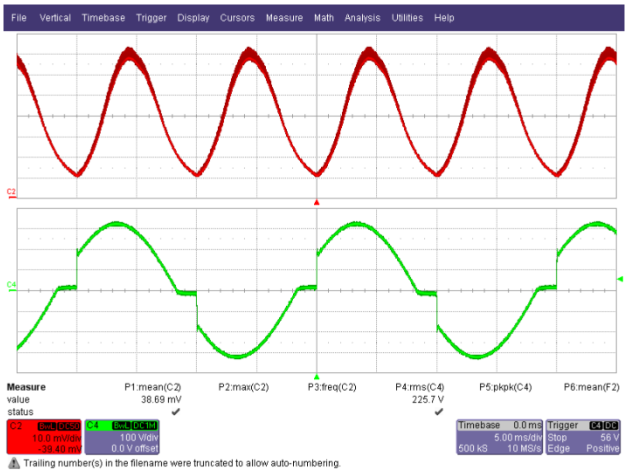

Figure 70 – 151° Conduction Angle.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

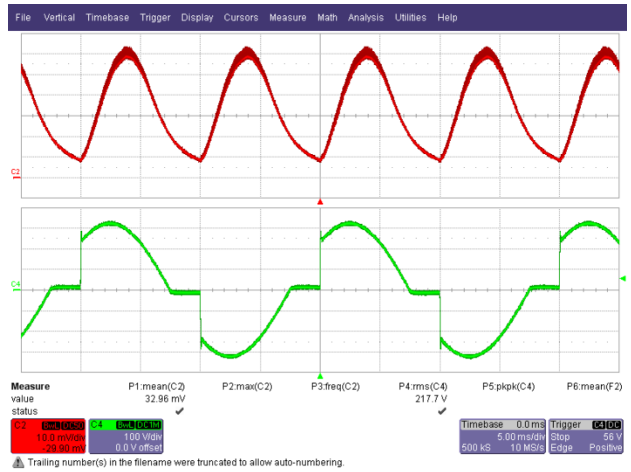

Figure 71 – 135° Conduction Angle.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

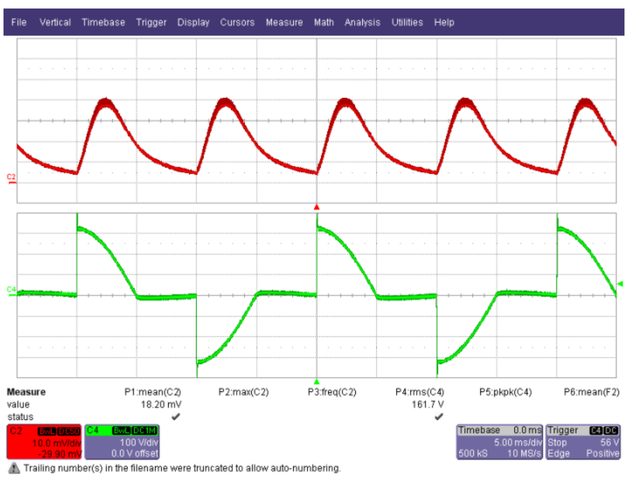

Figure 72 – 90° Conduction Angle.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

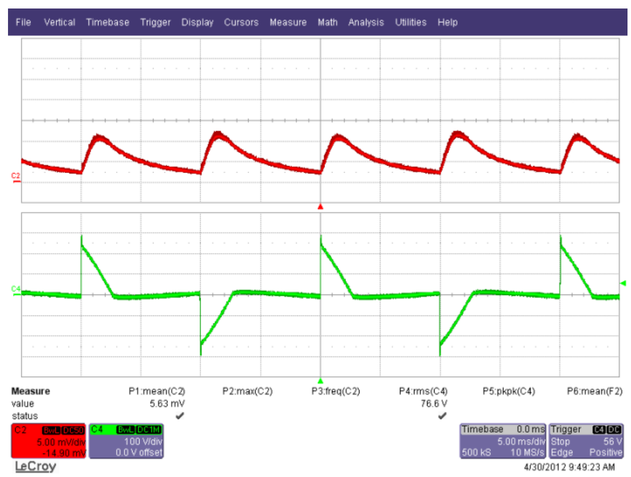

Figure 73 – 45° Conduction Angle.
Upper: I_{OUT}, 5 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

14.3 Input Voltage and Input Current Waveforms – Trailing Edge Dimmer

Input: 230 VAC, 50 Hz
Output: 100 V LED Load
Dimmer: ATD315

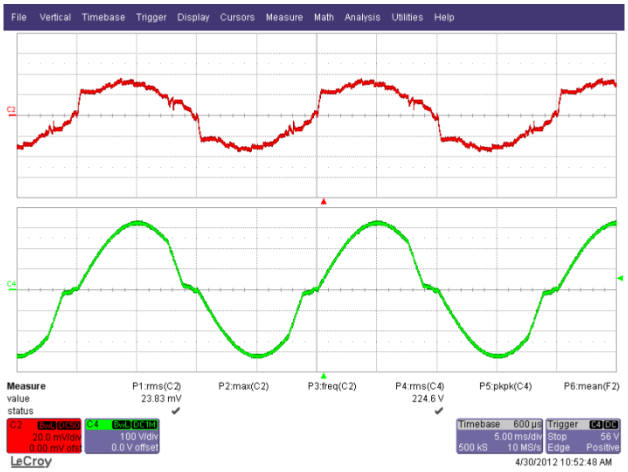

Figure 74 – 137º Conduction Angle.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

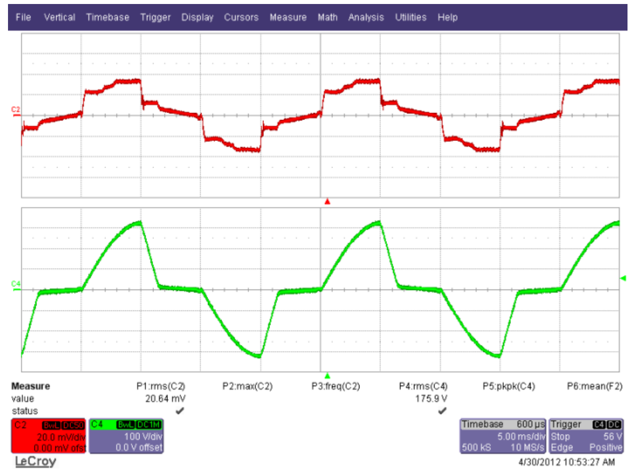

Figure 75 – 90º Conduction Angle.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

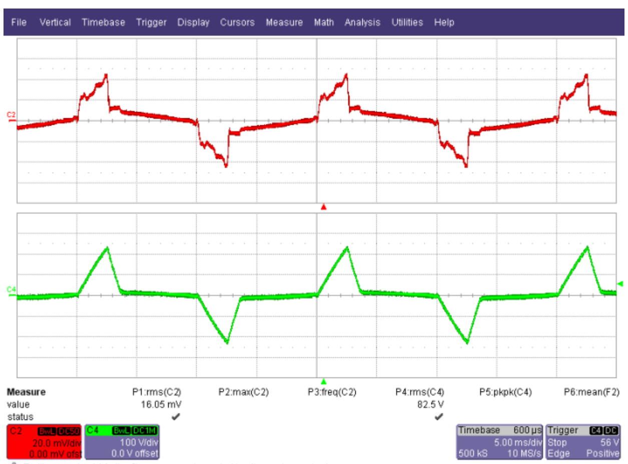

Figure 76 – 45º Conduction Angle.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

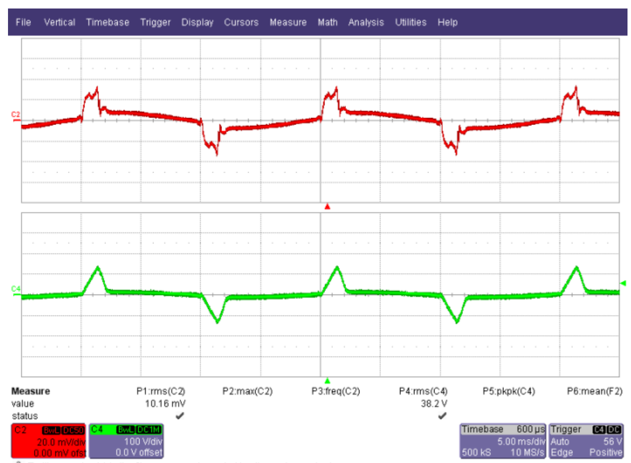

Figure 77 – 25º Conduction Angle.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

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14.4 Output Current Waveforms – Trailing Edge Dimmer

Input: 230 VAC, 50 Hz
Output: 100 V LED Load
Dimmer: ATD315

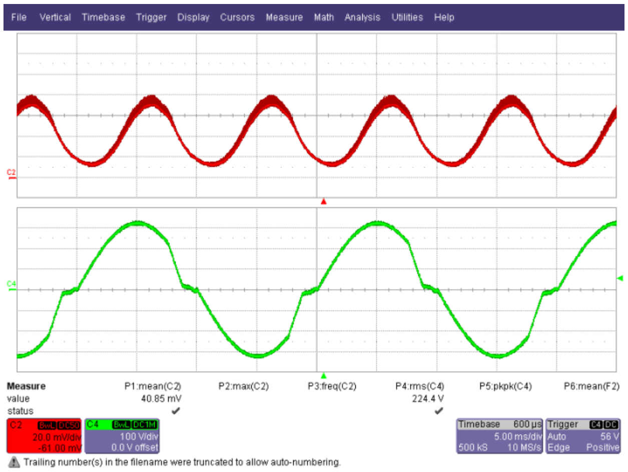

Figure 78 – 137º Conduction Angle.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

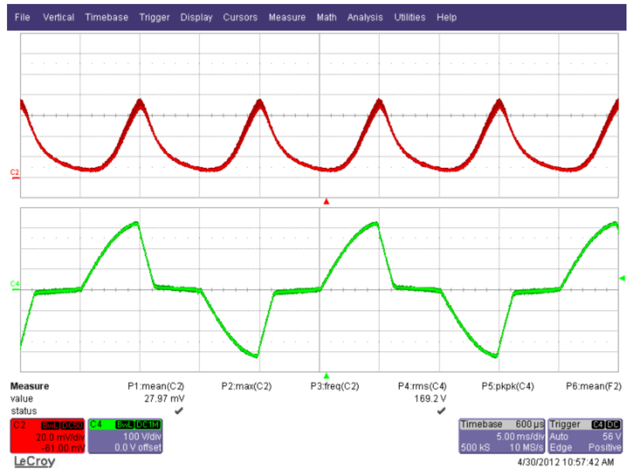

Figure 79 – 90º Conduction Angle.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

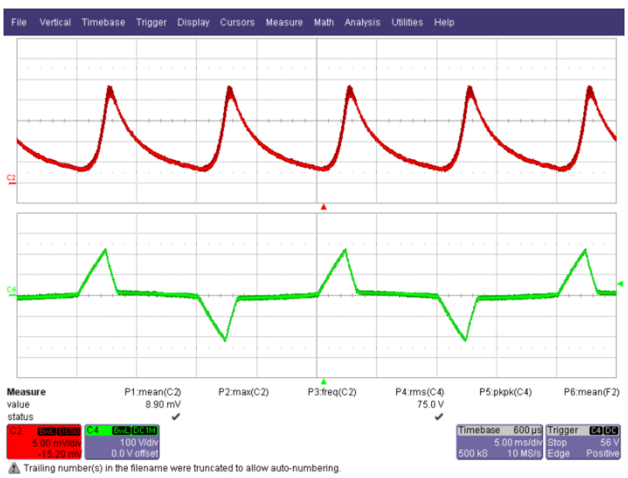

Figure 80 – 45º Conduction Angle.
Upper: I_{OUT}, 5 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

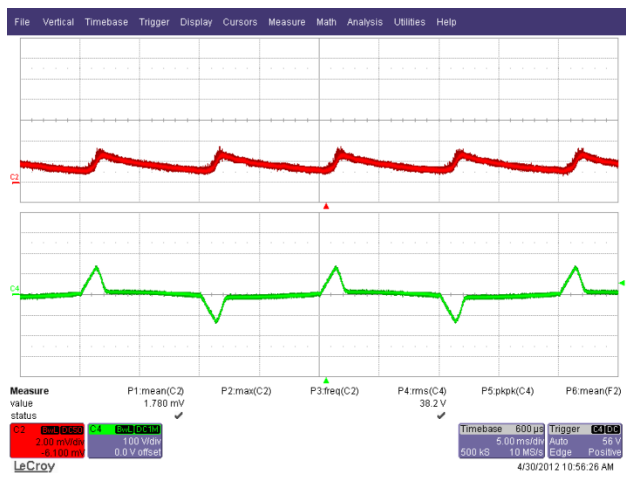

Figure 81 – 25º Conduction Angle.
Upper: I_{OUT}, 2 mA / div.
Lower: V_{IN}, 100 V, 5 ms / div.

15 Conducted EMI

15.1 Test Set-up

The unit was tested using LED load (100 V V_{OUT}) with input voltage of 230 VAC, 60 Hz at room temperature.

Figure 82 – EMI Test Set-up with the Unit and LED Load Placed Inside the Cone.

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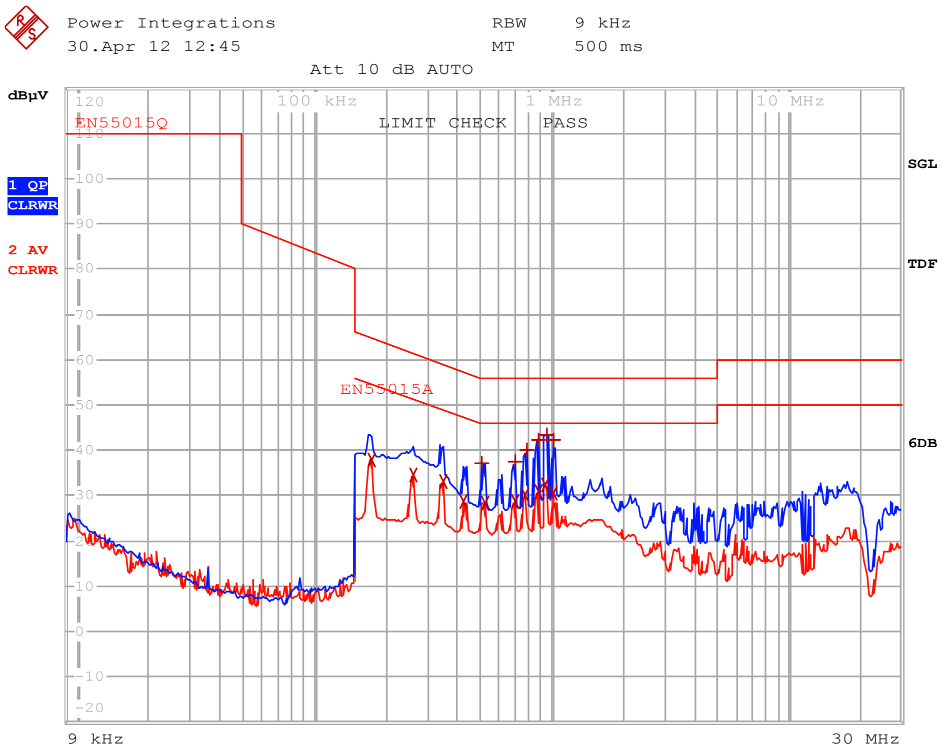
13.2 Test Result



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	172.421131986 kHz	38.01	L1 gnd	-16.82
2	Average	259.278686021 kHz	34.47	L1 gnd	-16.98
2	Average	346.008411606 kHz	32.92	L1 gnd	-16.13
2	Average	426.417977756 kHz	28.86	L1 gnd	-18.46
1	Quasi Peak	510.05878768 kHz	37.21	L1 gnd	-18.78
2	Average	520.310969312 kHz	28.19	L1 gnd	-17.80
1	Quasi Peak	701.300575623 kHz	37.47	L1 gnd	-18.52
2	Average	701.300575623 kHz	28.53	L1 gnd	-17.47
2	Average	767.002111284 kHz	30.07	L1 gnd	-15.92
1	Quasi Peak	782.418853721 kHz	40.11	L1 gnd	-15.88
1	Quasi Peak	872.919948931 kHz	42.43	L1 gnd	-13.56
2	Average	872.919948931 kHz	30.94	L1 gnd	-15.05
2	Average	935.888336808 kHz	32.51	L1 gnd	-13.48
1	Quasi Peak	954.699692378 kHz	43.46	L1 gnd	-12.53
1	Quasi Peak	1.01343296123 MHz	42.13	L1 gnd	-13.87
2	Average	1.01343296123 MHz	30.51	L1 gnd	-15.48

Figure 83 – Conducted EMI, 100 V LED Load, 230 VAC, 60 Hz, and EN55015 B Limits.

16 Line Surge

The unit was subjected to ±2500 V 100 kHz ring wave and ±500 V differential surge at 230 VAC using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring supply repair or recycling of input voltage.

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+2500	230	L1, L2	0	100kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	0	100kHz Ring Wave (500 A)	Pass
+2500	230	L1, L2	90	100kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	90	100kHz Ring Wave (500 A)	Pass

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+500	230	L1, L2	0	Surge (2Ω)	Pass
-500	230	L1, L2	0	Surge (2Ω)	Pass
+500	230	L1, L2	90	Surge (2Ω)	Pass
-500	230	L1, L2	90	Surge (2Ω)	Pass

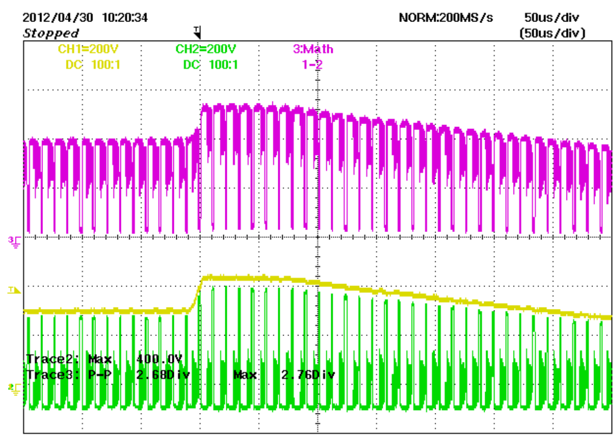


Figure 84 – +500 V (90º Injection Phase) Differential Surge VDS Waveforms.
C3: U1 VDS maximum voltage of <600 V.
C1: U1 Drain Voltage Reference to Output Return.
C2: U1 Source Voltage Reference to Output Return.

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17 Revision History

Date	Author	Revision	Description and Changes	Reviewed
11-Dec-12	CA	1.0	Initial Release	Apps & Mktg

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